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INTEGRATED CIRCUITS

UNITRODE

LINEAR INTEGRATED CIRCUITS DATA AND APPLICATIONS HANDBOOK

IC600

UNITRODE IC DATA HANDBOOK

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INTRODUCTION

Unitrode Integrated Circuits (U.I.C.C.) is a recognized leader in the design and manufacture of high-performance power management integrated circuits for use in the control for switching power supplies and small electronic motors, and for various interface functions.

The key to our success has been our ability to anticipate trends in carefully selected industrial, computer, and military market segments, and to develop products which respond to their needs.

To do this, U.I.C.C. takes a totally integrated approach to definition, development and production. Design and process engineers work together, often directly with customers, so that users can participate to the fullest in product development.

U.I.C.C. is also one of the few power management IC vendors to offer military versions of its new products. Our products are thus generally of higher quality than those offered by competitors who do not compete in the more demanding military/aerospace market.

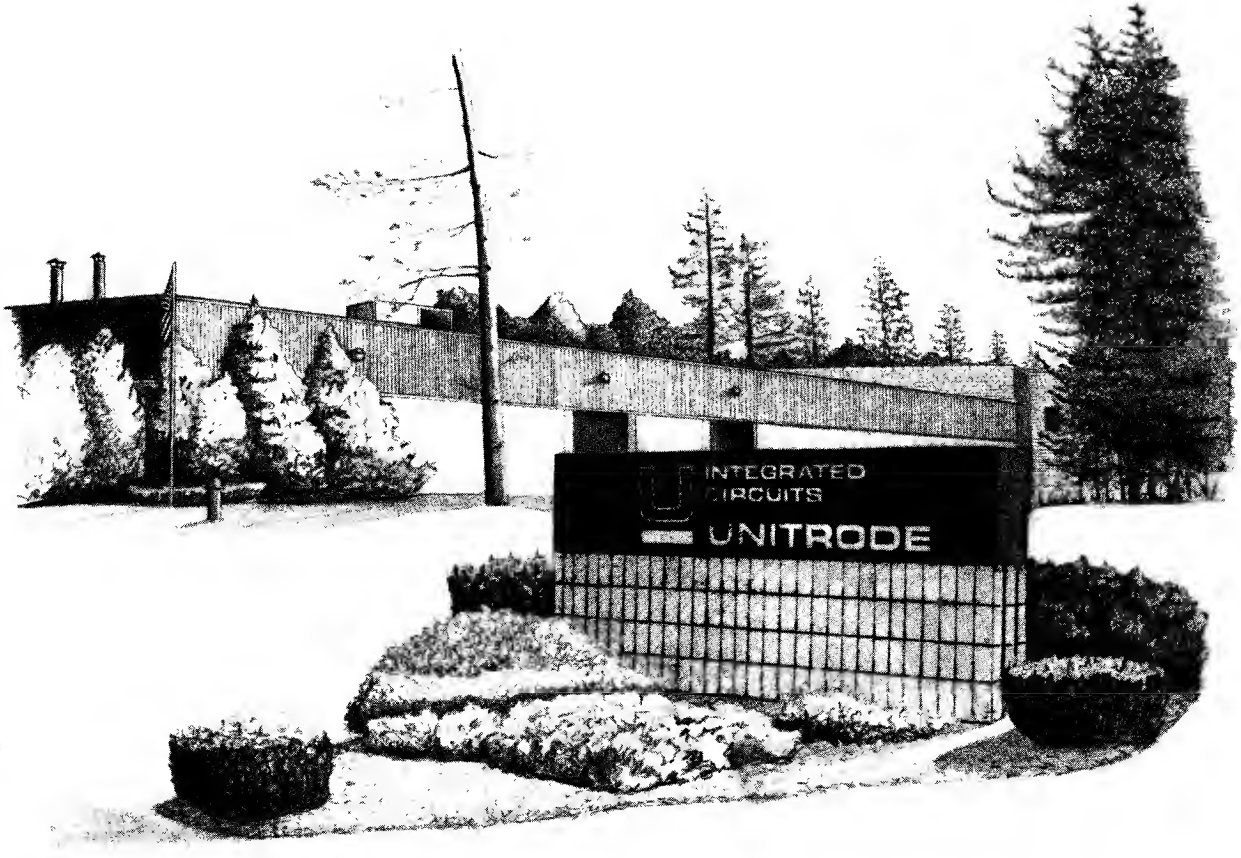
Our modern 85,000 square foot Merrimack, N.H. facility is fully JAN certified to MIL-M-38510, Class B. Many devices have been qualified with additional QPL items expected in the near term. U.I.C.C. is also servicing many OEM customers to produce and screen devices to their Class S needs.

U.I.C.C. has also made a major commitment to support the Singapore and Far East marketplace with upgrades in it's own 10,000 square foot test facility along with direct customer sales/support capability.

Another of our distinguishing features is the high degree of application and engineering support we provide. Our design-oriented engineering staff has created many custom ICs for very demanding customers, and the extraordinary size of our support staff reflects our commitment to unmatched customer support services.

We have earned our leadership position with our unique ability to innovate while adhering to the most stringent quality standards and highest levels of customer support. We will maintain this leadership by continuing to excel in all we do.

This data book describes U.I.C.C.'s current and new products along with detailed applications materials. We welcome your inquiries about our products, and the opportunity to develop new ones to meet your needs.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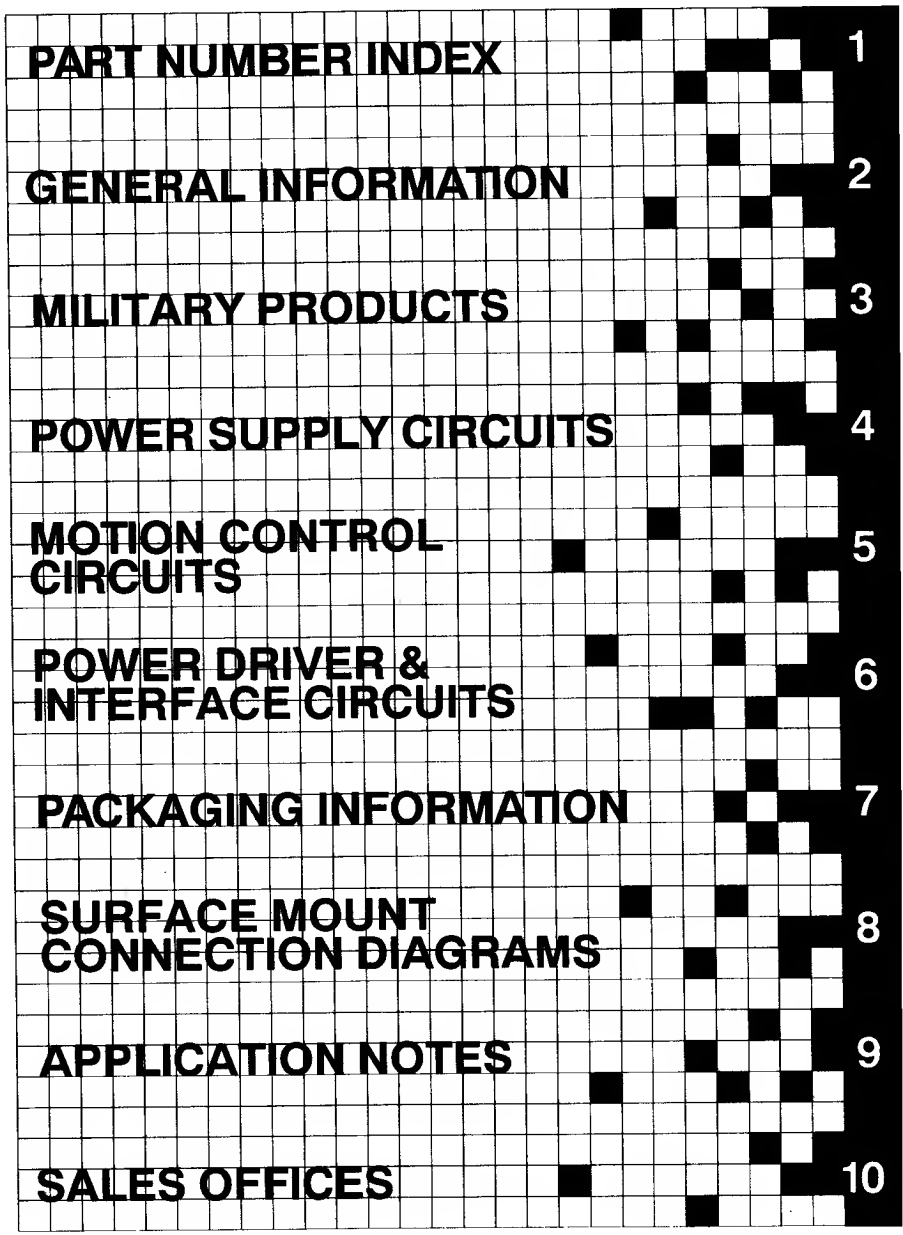
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4–132	UC3834J	HIgh Efficiency Linear Regulator: Ceramic DIL
4–132	UC3834N	HIgh Efficiency Linear Regulator; Plastic DIL
4–136	UC3835J	Low Cost, High Efficiency Regulator Ceramic DIL
4–136	UC3835N	Low Cost , High Efficiency Regulator Plastic DIL
4–136	UC3836J	Adjustable High Efficiency Regulator; Ceramic
4–136	UC3836N	Adjustable High Efficiency Regulator; Plastic DIL
4–141	UC3838AJ	Magnetic Amplifier Control Circuit Ceramic DIL
4–141	UC3838AN	Magnetic Amplifier Control Circuit
4–144	UC3840J	40V; 200mA; PWM Controller; Ceramic DIL
4–144	UC3840N	40V; 200mA; PWM Controller; Plastic DIL
4–152	UC3841J	Programmable, Off-Line PWM; Ceramic DIL
4–152	UC3841N	Programmable, Off-Line PWM, Plastic DIL
4–160	UC3842J	Low Cost Current Mode PWM; Ceramic DIL
4–160	UC3842N	Low Cost Current Mode PWM; Plastic DIL
4–166	UC3842AN	Adv. Low Cost PWM Plastic DIL
4–160	UC3843J	Low Cost Current Mode PWM; Ceramic DIL
4–160	UC3843N	Low Cost Current Mode PWM; Plastic DIL
4–166	UC3843AN	Adv. Low Cost PWM Plastic DIL
4–160	UC3844J	Low Cost Current Mode PWM; Ceramic DIL
4–160	UC3844N	Low Cost Current Mode PWM; Plastic DIL
4–166	UC3844AN	Adv. Low Cost PWM Plastic DIL
4–160	UC3845J	Low Cost Current Mode PWM; Ceramic DIL
4–160	UC3845N	Low Cost Current Mode PWM; Plastic DIL
4–166	UC3845AN	Adv. Low Cost PWM Plastic DIL
4–172	UC3846J	Current Mode PWM; Ceramic DIL
4–172	UC3846N	Current Mode PWM; Plastic DIL
4–179	UC3846AN	Adv. Current Mode PWM Plastic DIL

*Available in JAN/38510 Versions — See Military Versions

**Also Available in Isolated Tab Versions, "IG" Suffix

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
4–172	UC3847J	Current Mode PWM; Ceramic DIL
4–172	UC3847N	Current Mode PWM; Plastic DIL
4–180	UC3851N	Program. Off-Line PWM Plastic DIL
4–186	UC3854N	Power Factor Control Plastic DIL
4–192	UC3860J	Resonant Mode Control Ceramic DIL
4–192	UC3860N	Resonant Mode Control Plastic DIL
4–192	UC3860Q	Resonant Mode Ctonrol 28 Pin PLCC
4–200	UC3861N	Z.V.S. Resonant Mode Plastic DIL
4–200	UC3861Q	Z.V.S. Resonant Mode 20 Pin PLCC
4–200	UC3864N	Z.V.S. Resonant Mode Plastic DIL
4–200	UC3864Q	Z.V.S. Resonant Mode 20 Pin PLCC
4–200	UC3865N	Z.V.S. Resonant Mode Plastic DIL
4–200	UC3865Q	Z.V.S. Resonant Mode 20 Pin PLCC
4–208	UC3901J	Isolated Feedback Generator; Ceramic DIL
4–208	UC3901N	Isolated Feedback Generator; Plastic DIL
4–212	UC3903J	Quad Voltage and Line Monitor; Ceramic DIL
4–212	UC3903N	Quad Voltage and Line Monitor: Plastic DIL
4–16	LAS3905K	8A, Pos. TO-3 Reg.
4–16	LAS39U	8A, Adj. TO-3 Reg.
4–219	UC3906J	Lead Acid Battery Charger; Ceramic
4–219	UC3906N	Lead Acid Battery Charger; Plastic
6–72	UC5170CN	Octal Single Ended Driver; Plastic DIL
6–72	UC5170CQ	Octal Single Ended Driver; PLCC
6–76	UC5180CN	Octal Line Receiver; Plastic DIL
6–76	UC5180CQ	Octal Line Receiver; PLCC
4–24	LAS6350	5A, TO-3 Reg.
4–24	LAS6350P1	5A; Plastic SIP
4–24	LAS6351	5A, Adj. TO-3 Reg.
4–24	LAS6350P1	5A, Adj. Plastic SIP
4–29	LAS6380	8A, TO-3 Reg.
4–29	LAS6380P1	8A, Adj. Plastic SIP
4–29	LAS6381	8A, Adj. TO-3 Reg.
4–29	LAS6381P1	8A, Adj. Plastic SIP
4–230	UC7805ACK	1A; +5V; TO-3; Precision Fixed Reg.
4–230	UC7805ACT	1A; +5V; TO-220 Precision Fixed Reg.
4–230	UC7805AK	1A; +5V; TO-3; Precision Fixed Reg.
4–226	UC7805CK	1A; +5V; TO-3; Fixed Reg.
4–226	*UC7805K	1A; +5V; TO-3; Fixed Reg.
4–226	**UC7805G	1A; +5V; TO-257; Fixed Reg.
4–230	UC7812ACK	1A; +12V; TO-3; Precision Fixed Reg.
4–230	UC7812ACT	1A; +12V; TO-220; Precision Fixed Reg.
4–230	UC7812AK	1A; +12V; TO-3; Precision Fixed Reg.
4–230	**UC7812AG	1A; +12V; TO-257 Fixed Reg.
4–226	UC7812CK	1A; +12V; TO-3; Fixed Reg.
4–226	*UC7812CT	1A; +12V; TO-220; Fixed Reg.
4–226	*UC7812K	1A; +12V; TO-3; Fixed Reg.
4–226	**UC7812G	1A; +12V; TO-257 Fixed Reg.
4–234	**UC7815AG	1A; +12V; TO-257; Fixed Reg.
4–230	UC7815ACK	1A; +15V; TO-3; Precision Fixed Reg.
4–230	UC7815ACT	1A; +15V; TO-220; Precision Fixed Reg.
4–230	UC7815AK	1A; +15V; TO-3;
4–226	**UC7815G	Precision Fixed Reg.
4–226	UC7815CK	1A; +15V; TO-3; Fixed Reg.
4–226	UC7815CT	1A; +15V; TO-220; Fixed Reg.
4–226	*UC7815K	1A; +15V; TO-3; Fixed Reg.
4–226	**UC7815G	1A; +15V; TO-257; Fixed Reg.
4–238	UC7905ACK	1A; –5V; TO-3; Precision Fixed Reg.
4–238	UC7905ACT	1A; –5V; TO-220; Precision Fixed Reg.
4–238	UC7905AK	1A; –5V; TO-3;
4–238	**UC7905AG	Precision Fixed Reg.
4–234	UC7905CK	1A; –5V; TO-3; Fixed Reg.
4–234	UC7905CT	1A; –5V; TO-220; Fixed Reg.
4–234	*UC7905K	1A; –5V; TO-3; Fixed Reg.
4–234	**UC7905G	1A; –5V; TO-257; Fixed Reg.
4–238	UC7912ACK	1A; –12V; TO-3; Precision Fixed Reg.
4–238	UC7912ACT	1A; –12V; TO-220; Precision Fixed Reg.
4–238	UC7912AK	1A; –12V; TO-3;
4–238	**UC7912AG	Precision Fixed Reg.

*Available in JAN/38510 Versions — See Military Versions

**Also Available in Isolated Tab Versions, "IG" Suffix

PAGE	PART NUMBER	DESCRIPTION
4–234	UC7912CK	1A; –12V; TO-3; Fixed Reg.
4–234	UC7912CT	1A; –12V; TO-220 Fixed Reg.
4–234	*UC7912K	1A; –12V; TO-3; Fixed Reg.
4–234	**UC7912G	1A; –12V; TO-257; Fixed Reg.
4–238	UC7915ACK	1A; –15V; TO-3; Precision Fixed Reg.
4–238	UC7915ACT	1A; –15V; TO-220; Precision Fixed Reg.

PAGE	PART NUMBER	DESCRIPTION
4–238	UC7915AK	1A; –15V; TO-3; Precision Fixed Reg.
4–238	**UC7915AG	
4–234	UC7915CK	1A; –15V; TO-3; Fixed Reg.
4–234	UC7915CT	1A; –15V; TO-220; Fixed Reg.
4–234	*UC7915K	1A; –15V; TO-3; Fixed Reg.
4–234	**UC7915G	1A; –15V; TO-220; Fixed Reg.

1

*Available in JAN/38510 Versions — See Military Versions **Also Available in Isolated Tab Versions, "IG" Suffix

GENERAL INFORMATION 2

ABOUT THIS DATABOOK

PRODUCT CLASSIFICATION STATUS

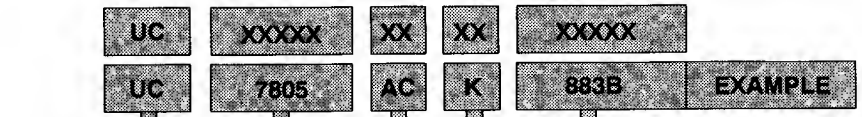
The following definitions apply to describe U.I.C.C.'s current product production status. U.I.C.C. also reserves the right to make changes without further notice in order to improve design performance, reliability, or manufacturability.

CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheet	First Production	Supplementary data may be published at a later date. U.I.C.C. reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product in Full Production

This databook contains complete data and applications information about Unitrode Linear Integrated Circuits for industrial and military applications. It includes all our latest new products including products that will be introduced throughout the year 1990. Also featured, are several new Power Packages and a totally new section dedicated to the description of our Military/Aerospace capabilities.

For more information about any new products or any of U.I.C.C. service capabilities, please call, write or fax.

PART NUMBER DESIGNATORS



PREFIX

"UC" Linear Integrated Circuits

PART NUMBER

•Generic P/N's
(See Data Sheets For Descriptions)
•5 Digit In-House Number
To Spec. Control Drawings

OPTIONAL GRADES

A - Improved Version
C - "Commercial" Temp Range

SCREEN/PROCESSING OPTIONS

883 - MIL-STD-883 Class B
JAN - MIL-M-38510 (Integrated Circuits)
SMD - STD Military Drawing (DESC)

PACKAGE OPTIONS

Letter Designator	Package Type
N	Plastic Molded Dip
J	Glass-Sealed Ceramic DIP
S	Side-Braized Ceramic DIP
D	14 Pin Narrow Body SO (150 mL)
DW	16/20 Pin Wide Body SO Surface Mount (300 mL)
L	Ceramic Leadless Chip Carrier
Q	Plastic Molded Quad PLCC
V	Multiwatt® Vertical Mount
VH	Multiwatt® Horizontal Mount
H	TO-39 Metal Can
K	TO-3 Steel-Base Power
T	TO-220 Plastic Power
JP	Ceramic Power
G	TO-257 Hermetic (TO-220 Style)
IG	TO-257 Hermetic Isolated Tab

For More Information See Packaging Section

QUALITY STATEMENT

Since its founding, Unitrode Integrated Circuits Corp. (U.I.C.C.) has structured its development to fully respond to customer requirements in areas of quality and overall product assurance, with particular emphasis on enhanced design and reliability.

As part of its total quality planning, U.I.C.C. has progressed through the traditional techniques of control by appraisal to a more mutually satisfying statistically based process monitoring. However, area's of accute variability would still require the use of universally accepted sampling plans, such as those reference in MIL-STD-105 and MIL-M-38510.

MIL-STD-105D

TABLE I
Sample size code letters

Lot or Batch Size	General Inspection Levels I	II	III
2 to 8	A	A	B
9 to 15	A	B	C
16 to 25	B	C	D
26 to 50	C	D	E
51 to 90	C	E	F
91 to 150	D	F	G
151 to 280	E	G	H
281 to 500	F	H	J
501 to 1200	G	J	K
1201 to 3200	H	K	L
3201 to 10000	J	L	M
10001 to 35000	K	M	N
35001 to 150000	L	N	P
150001 to 500000	M	P	Q
			R

TABLE II-A
Single sampling plans for normal inspection (Master table)

Sample Size Code Letter	Sample Size	Acceptable Quality Levels (normal inspection) 0.010 Ac Re	0.015 Ac Re	0.025 Ac Re	0.040 Ac Re	0.065 Ac Re	0.10 Ac Re	0.15 Ac Re	0.25 Ac Re	0.40 Ac Re	0.65 Ac Re	1.0 Ac Re	1.5 Ac Re	2.5 Ac Re	4.0 Ac Re	6.5 Ac Re	10 Ac Re	15 Ac Re
A	2														0 1	0		
B	3													0 1				
C	5												0 1					
D	8											0 1						
E	13										0 1							
F	20									0 1								
G	32								0 1									
H	50							0 1										
J	80						0 1											
K	125					0 1												
L	200				0 1													
M	315			0 1														
N	500		0 1															
P	800	0																
Q																		
R	1250																	

MIL-M-38510F
APPENDIX B

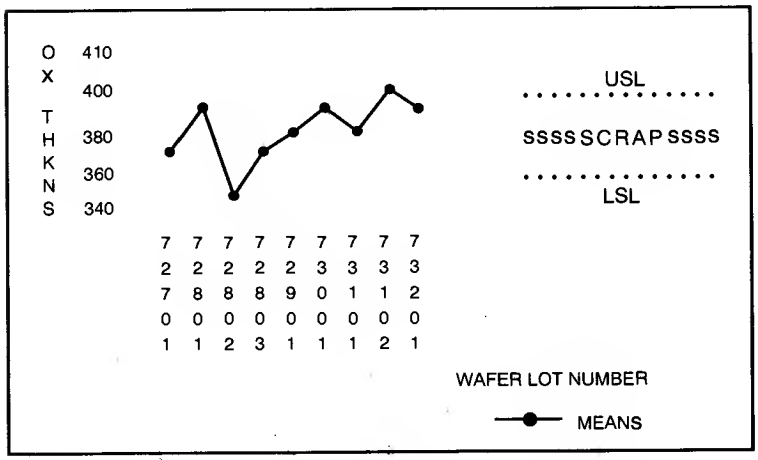
TABLE B-1. LTPD Sampling Plans 1/ 2/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample)

Max Percent Defective (LTPD) or λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiplied by 1000)														
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)

Quality

Ongoing efforts in process improvement have become an aggressive daily pursuit in manufacturing whereby meeting specification is no longer good enough.



Simply, many benefits to the customer have been realized in the form of on-time-delivery, superior quality and unprecedented levels of sustained reliability. Organizationally, a "total committment" to quality improvements have manifested themselves in the form of:

- Improved customer satisfaction
- Improved product quality
- Known process capabilities
- Increased yields
- Improved product flow
- Reduction in quality costs such as scrap and rework
- Prevention orientation and quality consciousness
- Facts vs. Opinions
- Reduction in operating costs

U.I.C.C.'s unique self auditing approach makes certain quality ownership is an intrinsic part of the manufacturing community with no one faction having full responsibility. Documentation at U.I.C.C. has been developed to truly reflect a "Real Time" status through master matrixing and planning whereas design, fabrication, assembly and test and their many detailed process steps are tied together relationally.

Reliability assurance at U.I.C.C. has specific goals to demonstrate product reliability of the various functional catagories that make up this primarily bipolar product base. It is important to note the existence of feedback to design and process engineering that ensures all products receive continuing reviews, thus enhancing even the most mature family of products.

Quality

QUAL/QCI FLOW FOR JANB, 883B
MIL-STD-883 METHOD 5005

GROUP A ELECTRICALS
–55°, +25°, +125°, +150°C

GROUP B

SUBGROUP 2
RESISTANCE TO SOLVENTS
SUBGROUP 3
SOLDERABILITY
SUBGROUP 5
BOND STRENGTH

GROUP C

SUBGROUP 1
STEADY STATE LIFE
END POINT ELECTRICALS

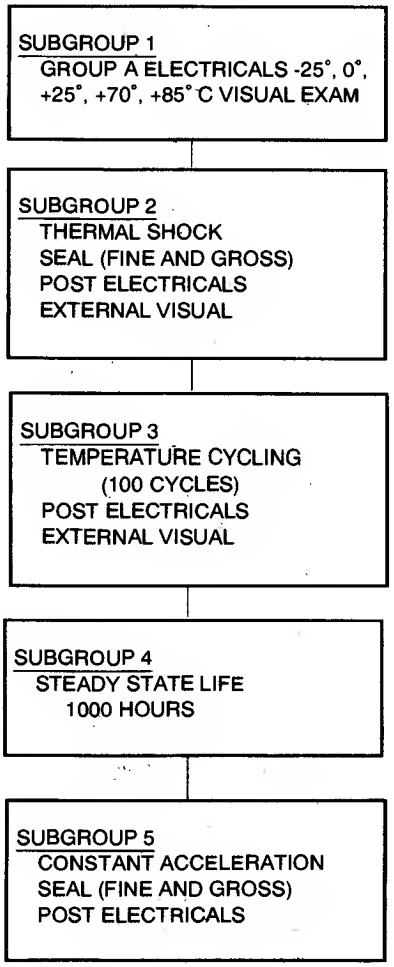
GROUP D

SUBGROUP 1
PHYSICAL DIMENSIONS
SUBGROUP 2
LEAD INTEGRITY
SEAL (FINE AND GROSS)
SUBGROUP 3
THERMAL SHOCK
TEMPERATURE CYCLING
MOISTURE RESISTANCE
SEAL (FINE AND GROSS)
VISUAL EXAMINATION
END POINT ELECTRICALS
SUBGROUP 4
MECHANICAL SHOCK
VIBRATION, VARIABLE FREQUENCY
CONSTANT ACCELERATION
SEAL (FINE AND GROSS)
VISUAL EXAMINATION
END POINT ELECTRICALS
SUBGROUP 5
SALT ATMOSPHERE
SEAL (FINE AND GROSS)
VISUAL EXAMINATION
SUBGROUP 6
INTERNAL WATER VAPOR CONTENT
SUBGROUP 7
ADHESION OF LEAD FINISH
SUBGROUP 8
LID TORQUE

GROUP E
(RADIATION HARDNESS ASSURANCE)
(WHEN APPLICABLE)

SUBGROUP 1
NEUTRON IRRIADIATION
END POINT ELECTRICALS
SUBGROUP 2
STEADY STATE TOTAL DOSE IRRIADIATION
END POINT ELECTRICALS
SUBGROUP 3
TRANSIENT IONIZING IRRIADATION
END POINT ELECTRICALS

QUALIFICATION FLOW FOR COMMERCIAL-INDUSTRIAL DEVICES



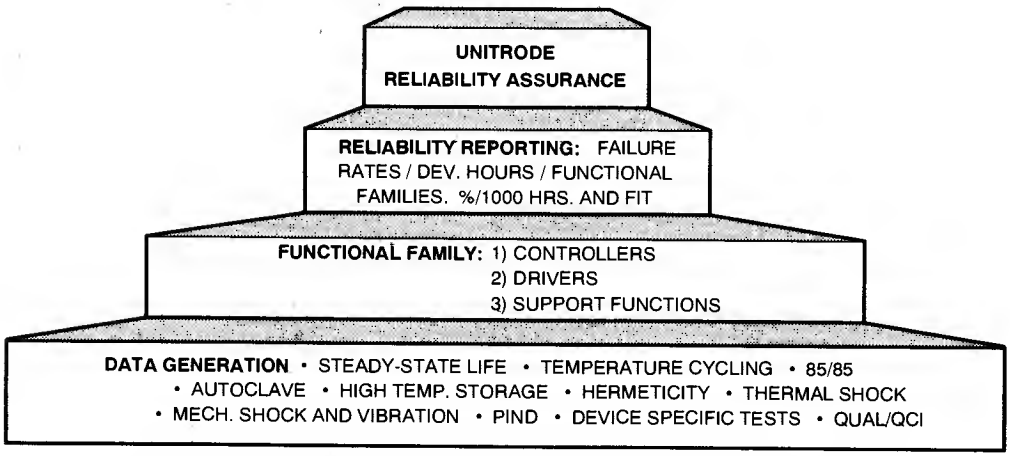
NOTE: UNITRODE INTEGRATED CIRCUITS ALSO PERFORMS TESTING TO SOURCE CONTROL DRAWINGS FOR CLASS S DEVICES IN ACCORDANCE WITH MIL-STD-883

Quality

Should failure occur either in the field or during the course of reliability testing, in-depth failure analysis is performed to identify and understand the failure mechanism(s) involved. Immediate feedback to design or process for the purpose of corrective action is systematically accomplished. Critical inventory nodes are also alerted

Levels of long-term device reliability through the accumulation of millions of hours of testing at accelerated temperatures have demonstrated 40 fit or lower failure rates on our more mature products within a functional family. With, the ever growing demand for greater system reliability, this is a major factor.

U.I.C.C. has planned and developed reliability goals for the decade of the 90's that realistically test the technology.



In summary, U.I.C.C. has a committment to supply its customers with nothing less than the quality they demand.

"A Total Quality Concept"

Quality Assurance Manager

UNITRODE SPC PROGRAM

WHAT SPC IS TO UICC:

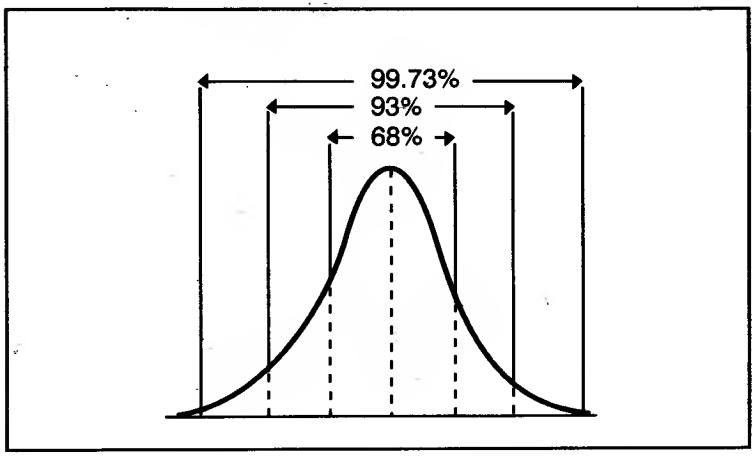
The objective of the UICC SPC program is a continual improvement in quality and increase producitvity to meet our Customer requirements.

To accomplish this objective, SPC techniques are to be applied to all processes to help reduce and eventually eliminate defects, thus improving quality and productivity and reducing the cost of our products. The specific goal is that all critical processes should be brought into statistical control and become design capable. These processes will be analyzed and controlled by the implementation of SPC, using charting techniques by the operators.

SPC techniques are used to identify and resolve both production workmanship and support problems which impact quality, productivity and cost.

Several senior staff are appointed members of the SPC Steering Committee, and are responsible for assuring that effective personnel training and implementation programs are established, maintained and managed.

All functional and support personnel who are a part of or work with those processes related to the production or support are SPC trained and provided with a SPC Facilitator/Coach to assist them in the never-ending improvement of quality and productivity.



Why U.I.C.C. decided to implement SPC:

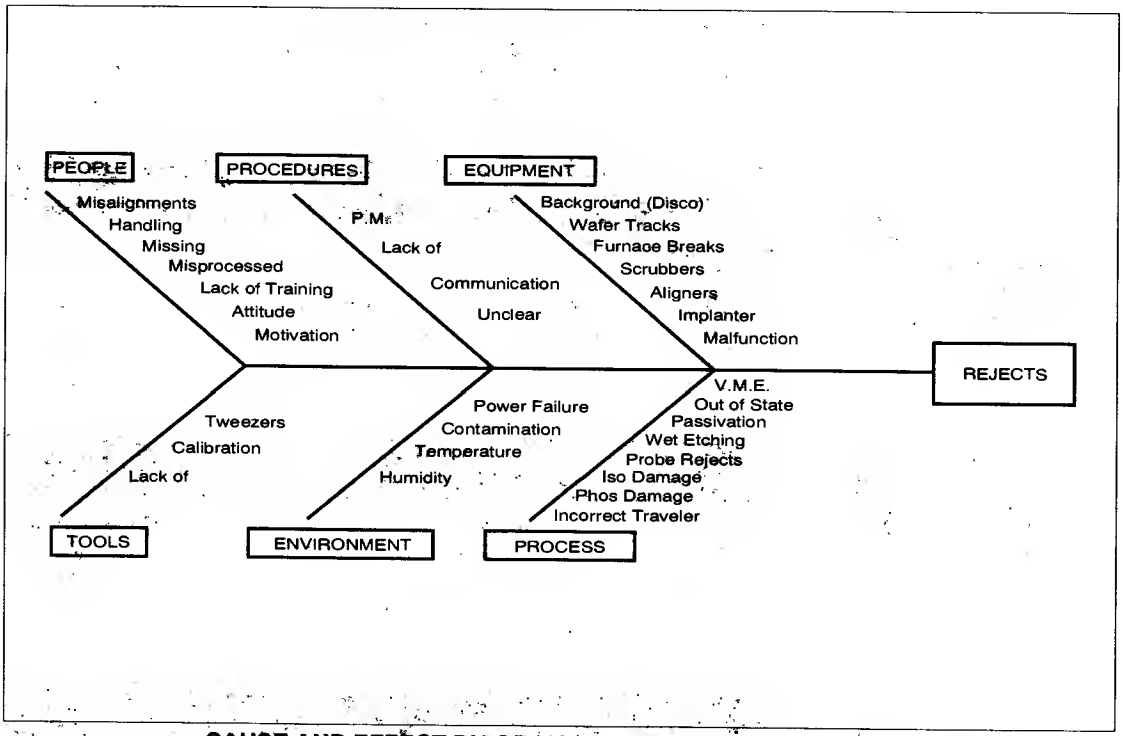
It was decided to implement SPC throughout our Facility in order to enhance quality and reduce scrap through identification of process variation, and through the reduction of this variations by means of real time corrective action. It is expected to establish the cultural environment and the organizational support required to achieve the Six-Sigma goal.

Quality

What it means to our Customers:

Statistical Process Control, or SPC, is the science of controlling manufacturing operations to insure the quality of product conformance. SPC, through the use of statistical techniques, allows for corrective action to be taken to avert possible quality problems before they occur thus reducing cost of reworking or scrapping product.

These factors enable Unitrode (U.I.C.C.) to better serve our Customers and to improve quality, delivery and cost of our products. Specifications such as JEDEC publication 19 which states the minimum requirements for SPC relative to semiconductor processing has become an intrinsic part of our day to day operation.



CAUSE AND EFFECT DIAGRAM - WAFER REJECTS

INTEGRATED CIRCUITS

UNITRODE

New Quality Products From U.I.C.C.

PULSE WIDTH MODULATORS

Part Number	Description	Page Number
UC3823A	Advanced 1MHz PWM	.4–119
UC3825A	Advanced 1MHz PWM	.4–119
UC3842A	Improved Low Cost PWM	.4–166
UC3843A	Improved Low Cost PWM	.4–166
UC3844A	Improved Low Cost PWM	.4–166
UC3845A	Improved Low Cost PWM	.4–166
UC3846A	Advanced Current Mode PWM	.4–179
UC3883	ISDN, Micro Power PWM	.4–206
UC3885	ISDN, Micro Power PWM	.4–207

RESONANT CONTROLLERS

Part Number	Description	Page Number
UC3861	ZVS Resonant Controller	.4–200
*UC3862	ZVS Resonant Controller	.4–200
*UC3863	ZVS Resonant Controller	.4–200
UC3864	ZVS Resonant Controller	.4–200
UC3865	ZVS Resonant Controller	.4–200

HIGH POWER FET DRIVERS

Part Number	Description	Page Number
UC3708	Dual Non-Inv. Driver	6–29
UC3709	Dual Fet Driver	6–33
UC3710	"Miller Killer"™ High Power Driver	6–36
UC3711	Ultra High Speed Fet Driver	6–39

POWER SUPPLY SUPPORT CIRCUITS

Part Number	Description	Page Number
UC3838A	Improved MAG-AMP Controller	.4–141
UC3854	Ave. Current Sense Power Factor	.4–186
UC1054C	Charage Pump Converter	4–72
UC3724	Isolated Drive Transmitter	6–44
UC3725	Isolated High Side Driver	6–47

NOTE: Only commercial part numbers are indicated see military section for military versions
*Products have not been announced at time of printing

New Quality Products From U.I.C.C.

LOW DROP VOLTAGE REGULATORS

Part Number	Description	Page Number
UC3832	High Performance Linear Reg.	4–127
UC3833	Low Cost Linear Reg.	4–127

3 TERMINAL VOLTAGE REGULATORS

Part Number	Description	Page Number
UC117G	1.5A; TO-257, Positive Adj. Reg.	4–46
UC117H	0.5A; TO-5, Positive Adj. Reg.	4–46
UC117HV	57V; TO-5, Positive Adj. Reg.	4–50
UC137G	1.5A; TO-257, Negative Adj. Reg.	4–54
UC7805AG	1.0A; +5V, 1%, Fixed Voltage Reg	4–230
UC7812AG	1.0A; +12V, 1% Fixed Voltage Reg	4–230
UC7815AG	1.0A; +15V, 1% Fixed Voltage Reg	4–226
UC7905AG	1.0A; – 5V, 1% Fixed Voltage Reg	4–238
UC7912AG	1.0A; –12V, 1% Fixed Voltage Reg	4–238
UC7915AG	1.0A; –15V, 1% Fixed Voltage Reg	4–238
UC1033KG	3.0A; Negative Adj. Reg. TO-3.TO-257	4–69

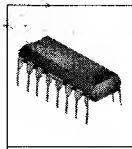
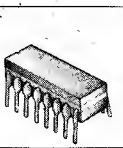
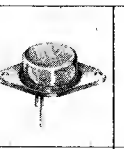
HIGH CURRENT REGULATORS

Part Number	Description	Page Number
LAS6350	5.0 Amp, Switching Reg; TO 3, Plastic Sip	4–24
LAS6380	8.0 Amp, Switching Reg; TO 3, Plastic Sip	4–29
LAS1905	5.0 Amp, +5V, Lin. Reg; TO-3	4–10
LAS1912	5.0 Amp, +12V Lin. Reg; T0-3	4–10
LLM338	5.0 Amp, Adj. Reg; To–3	4–34

MOTOR CONTROLLERS

Part Number	Description	Page Number
UC3174	.8A, Voice Coil Motor Drive	5–80
UC3175	.8A, Voice Coil Motor Drive	5–80
UC3177	2.0A, Voice Coil Motor Drive	5–85
UC3623	Low Noise 3-Phase Brushless Driver	5–94
UC3625	High Voltage 3-Phase Brushless Driver	5–39
UC3635	Phase Lock Loop Controller	5–60
UC3655	Low Sat. Linear 3-Phase Brushless	5–97
UC3770A	High Performance Stepper Motor Drive	5–110
UC3770B	HIgh Performance Stepper Motor Drive	5–110

PACKAGE CROSS-REFERENCE CHART

								
	PLASTIC DIP	**CERAMIC DIP**	**MULTIWATT**	**PLCC**	**LCC**	**SOIC**	**TO-3**	**TO-220**
UNITRODE	N	J	V	Q	L	D,DW	K	T
Linear Tech	N,NB	J,J8	—	—	L	5,58	K	T
Cherry	N	J	V	FN	L	D,DW	—	T
SGS	B,N,P	—	V	—	—	D	K	—
Silicon General	M,N	J,Y	—	Q	L	D,DW	K	P
Texas Instruments	P,N	J,JG	—	FN	FC	DW	K	KC
Signetics	N	F	—	—	—	D	—	U
National	N	J	—	—	—	—	K,KC	T
Motorola	P	U	—	FN	—	D	K,KC	T
Fairchild	T,P	D,R	—	—	L	—	K	U
Sprague	A,M,B	R	—	E	—	L	V	T

Die And Wafers

DESCRIPTION

Unitrode Integrated Circuits Corp. U.I.C.C. offers most of all its's products described in this data book in die and/or wafer form. Products include all Pulse Width Modulators (PWM's), Motor Controls, Low-Drop Regulator, fixed, and adjustable industry standard Voltage Regulators, Power Drivers and Switches, and Special Function Circuits. Most all U.I.C.C. products are designed with military temperature range operation capability.

U.I.C.C. die utilize linear bipolar technology featuring tight beta control and resistor matching techniques. Also, other enhancements used implement thin film resistor and Schottky process, as well as in-house epitaxial capability for unique voltage flexability. All products are protected by a CVD Oxide plus Nitride layers to make a sandwich passivation system that offers superior coverage over all junctions.

Die thicknesses vary by product type, however, they fall into the catagories; 12 mils ± 1 mil, or 15 mils ± 1 mil. Interconnects are an alloy of copper (2%) and aluminum (to reduce possibility of metal migration). Backside metalization is Titanium - Nickel - Silver, suitable with various common eutectic and thermal epoxy mount down techniques used today.

TESTING

All products are tested at two separate points. 1) In-Line probing and 2) Final test probing.

Final test probe utilize state-of-the-art high speed/power ATE equipment. Die are 100% tested to low power DC limits.

INSPECTION

U.I.C.C. performs visual inspections on military grade die to MIL-STD-750B, Method, 2072 and to MIL-STD-883C Method 2010, condition A or B, or to customer supplied requirements.

Die can be supplied in "waffle pack' or single wafer form. Standard wafers are 100 mils (generic 4 inch diameter).

ORDERING INFORMATION

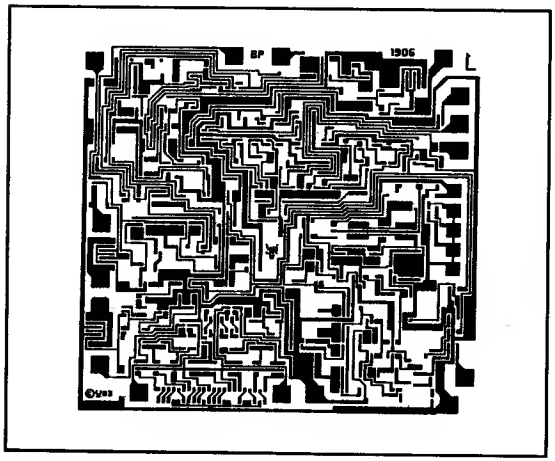
PART NUMBER = UCXXXX: CHIP WFR

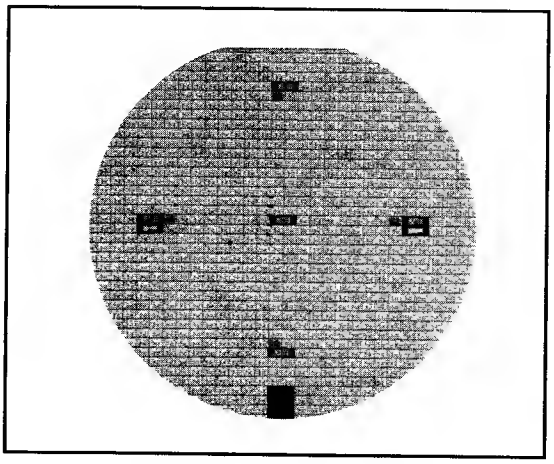
\+

CHIP ORDER

\+

WAFER ORDER





Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

MILITARY PRODUCTS 3

JAN38510 SMD 883S 883B
JAN38510 SMD 883S 883B
JAN38510 SMD 883S 883B

MILITARY/AEROSPACE PROCESSING:

Processing TO MIL-M-38510 and MIL-STD-883 is performed by a totally dedicated business unit within the linear division of U.I.C.C. to serve the power linear components requirements of our various Military/Aerospace customers. U.I.C.C. has been committed to this market for many years and intends to continue to support this key market segment.

The Military Business Unit offers several levels of processing flows as noted below. Any of the flows listed would satisfy a majority of customer requirements.

- **Jan-Level "B"** - full compliance to MIL-M-38510 Jan program and QPL listings as published by DESC.
- **Standard Military (DESC) drawing (SMD)** — conformance to Class "B" process requirements to DESC selected item drawings.
- **SCD-B** — conformance to Class "B" process requirements of MIL-STD-883 to customer temperature range and/or data sheet electricals.
- **SCD-S** — conformance to Class "S" process requirements of MIL-STD-883 to customer drawing requirements.

JAN QUALIFIED (MIL-M-38510) CLASS "B" PROGRAM:

Our Jan Program offers the customer a standard of product processing, and of quality and reliability that is well documented by U.I.C.C. and monitored by the defense electronics supply Center (DESC) of the U.S. government. The products are manufactured in the U.S. in our certified facility to the requirements of MIL-M-38510 and individual product specifications as called out in the MIL-M-38510 "Slash Sheets". The DESC certification is based on standardized documentation for design, processing, test methods, product assurance program, and personnel training. Facilities and documentation are audited by DESC prior to certification and periodically thereafter.

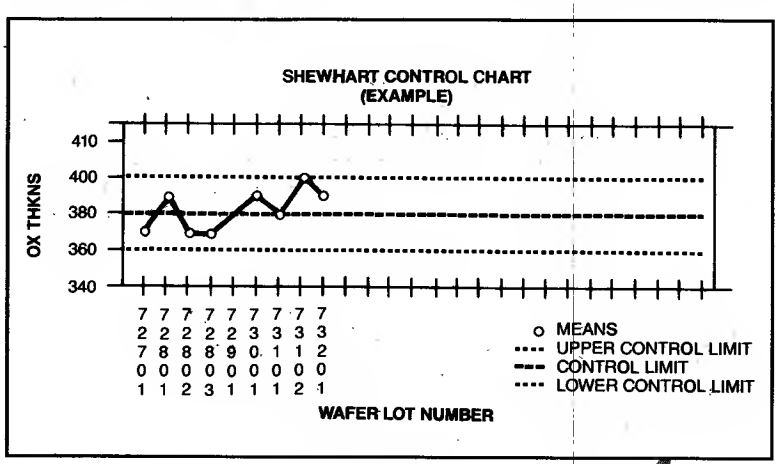
U.I.C.C. maintains a very active MIL-M-38510 qualified product list (QPL) program and has developed a key position in expanding the number of QPL's for power linear products.

DESC SELECTED ITEM DRAWINGS:

DESC selected item drawings or military drawings provide an industry standard specification in compliance with Class "B" requirements for devices that are not JAN qualified.

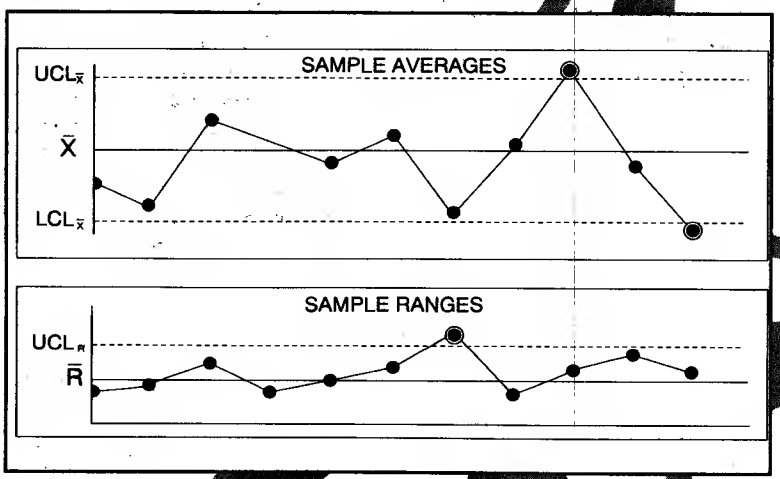
STATISTICAL PROCESS CONTROL/MILITARY

SPC Unitrode's Military Business Unit utilizes Statistical Process Control for all critical process steps. SPC has proven to enhance production capabilities and product quality in the military group. By monitoring and control of these critical process and assembly steps, U.I.C.C. will better serve our customers and improve quality, delivery and cost of our products.



Control charts are in use for those critical parameters that affect's function, safety and reliability.

Unitrode, utililizes data from control charts to identify opportunities for continually reducing variation in our process output.



NEW
MILITARY LINEAR INTEGRATED CIRCUITS

NEW POWER FACTOR CONTROLLER

UC1854 HIGH POWER FACTOR PREREGULATOR

- Fast feed-forward line regulation
- Average current-mode control for low noise sensitivity
- Limit line current distortion to <5%
- Control to .99 power factor
- World-wide voltage operation without range switching
- Available in 16 pin ceramic DIL and 20 pin surface mount military packages

NEW RAD TOLERANT FET DRIVER

UC1711 DUAL ULTRA HIGH SPEED FET DRIVER

- 25nS rise and fall times into 1000pF
- 15nS propagation delay
- 1.5 Amp source or sink output drive
- Operation with 5V to 35V supply
- Available in 8-pin ceramic DIL or 20 pin surface mount military packages

MILITARY 3Ø BRUSHLESS DC MOTOR DRIVER

UC1620 SWITCHMODE DRIVER FOR BRUSHLESS DC MOTORS

- Current mode control
- 3A peak output current
- 8V to 40V operation
- Fixed off time control
- TTL compatible Hall inputs
- Available in new 25W power ceramic 24 pin DIL package (see "J" under package section)

MILITARY RESONANT MODE CONTROL

UC1860 ZCS VERSITILE RESONANT MODE CONTROLLER

- 3 MHz VFO linear over 100:1 range
- 5 MHz error amplifier with controlled output swing
- Programmable one-shot timer — down to 100NS
- Dual 2A peak totem pole outputs with programmable sequence capability
- Programmable UVLO
- Very low start up current
- Programmable fault management & restart delay
- Uncommitted comparator
- Two military packages — 24-Pin DIL and 28-Pin LCCC

NEW
MILITARY LINEAR INTEGRATED CIRCUITS

1832/1833 PECISION LOW DROP LINEAR CONTROLLERS

- Precision 1% reference
- Over-current sense thersold accurate to 5%
- Programmable duty-ratio over current protection

Additional features of 1832

- Adjustable current limit to current sense ratio
- Seperate + V_{IN} terminal
- Programmable driver current limit
- Access to V_{REF} and E/A(+)
- Logic-Level disable input
- Available in 8,14-PIN ceramic DIL packages

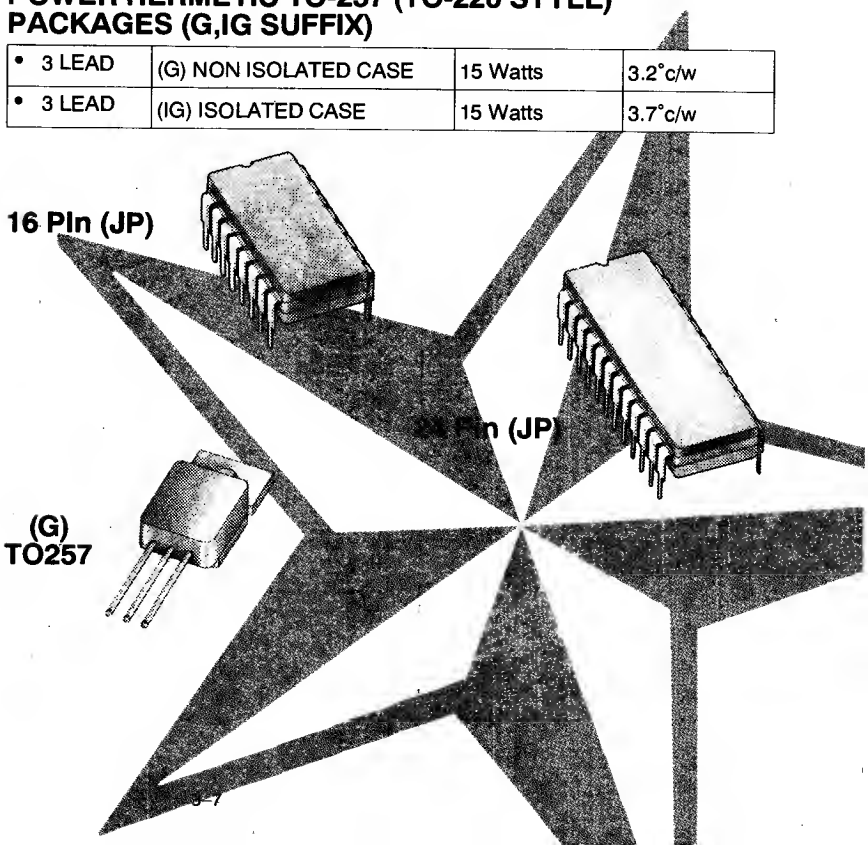
NEW POWER MILITARY PACKAGES

POWER HERMETIC DUAL-IN-LINE PACKAGES (JP SUFIX)

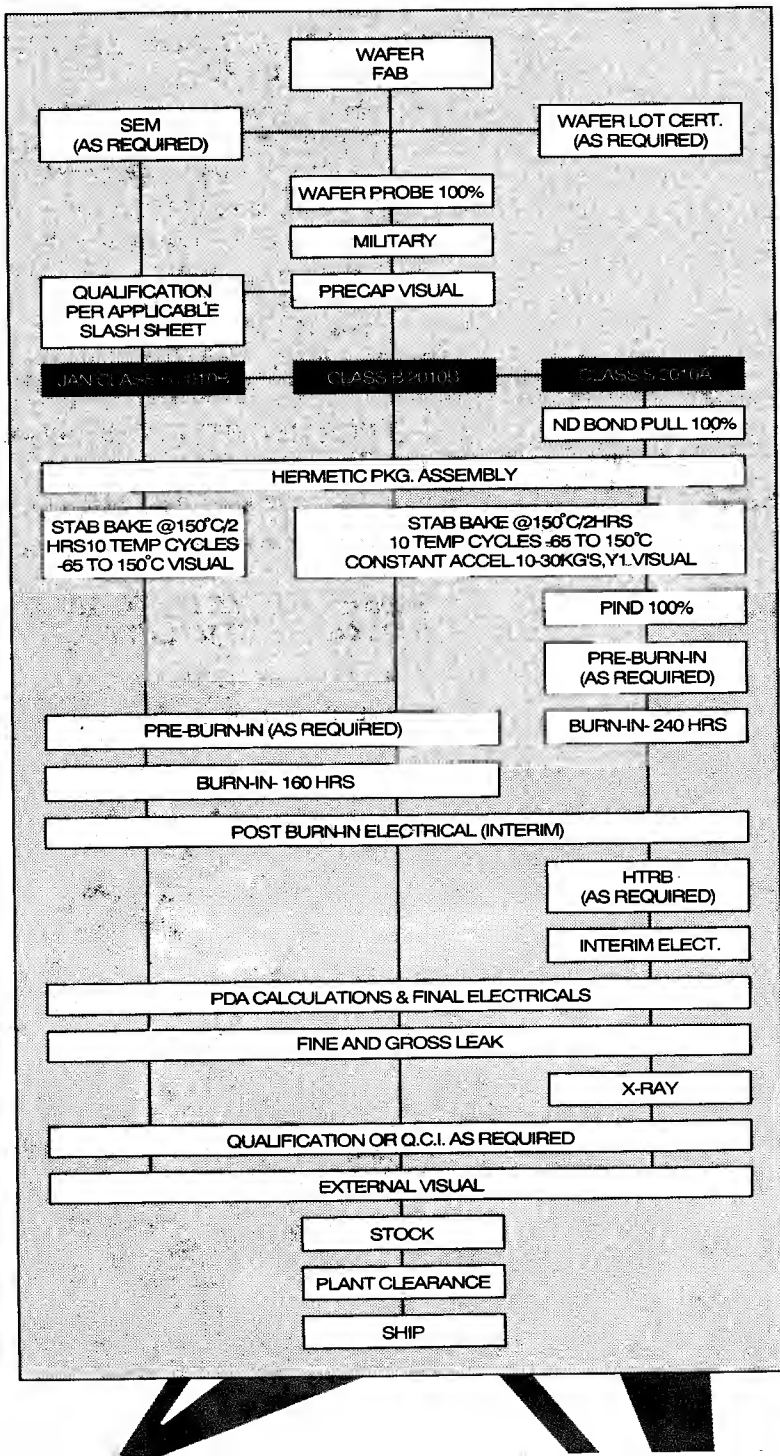
• 16 PIN	300 MIL (wide)	15 Watts	5°c/w $\theta_{J\text{-}C}$ (Bottom Plate)
• 24 PIN	600 MIL (wide)	25 Watts	3°c/w $\theta_{J\text{-}C}$ (Bottom Plate)

POWER HERMETIC TO-257 (TO-220 STYLE) PACKAGES (G,IG SUFFIX)

• 3 LEAD	(G) NON ISOLATED CASE	15 Watts	3.2°c/w
• 3 LEAD	(IG) ISOLATED CASE	15 Watts	3.7°c/w



MILITARY SCREENING FLOWCHART



JAN PRODUCT LINE

Unitrode Integrated Circuits Corporation presently has a DESC line certification to MIL-M-38510 to produce Jan Class B linear microcircuits. UICC has qualified 15 device types covering 6 slash sheets. Unitrode Integrated Circuits is the originator of the 702 current mode PWM slash sheet (UC1846/UC1847) and in January of 1990 received qualification of the 70201 (UC1846).

In a continued effort to meet and produce the highest military grade devices, Unitrode Integrated Circuits reviews all existing slash sheets applicable to our product base in the effort to either add device types or develop new slash sheets for industry use.

Unitrode Integrated Circuits also has lab suitability to perform MIL-STD-883 method 5004 and 5005 screening/QUAL/QCI issued by DESC, with the exception of internal water vapor content and vibration variable frequency. In addition, we have full self-auditing program to ensure compliance to all specifications. Our SPC program has enhanced the processing of all product. Consequently, through the control charts established in our in-house assembly area, we have been able to eliminate constant acceleration from our Jan screening flow with approval from the defense electronic supply center (DESC).

Unitrode Integrated Circuits is committed to producing military grade linear monolithic devices in full compliance to MIL-M-38510. MIL-STD-883, SMD and SCD requirements and at all times focusing on quality and reliability enhancements.

MILITARY PRODUCTS

MILITARY PACKAGE

Part No. Designator	Package Type	Typ. θJC, °c/w	TYP θJA, °c/w
G	TO-257 Non Isolated	3.2[1]	N/A
IG	TO-257 Isolated Tab	3.7[2]	N/A
H	TO-5	20	130
J	Ceramic DIL 8-Pin 14-Pin 16-Pin 18-Pin	 40 30 30 30	 130 80 80 75
JP	16-Pin 24-Pin	30 5[2], 10[3]	N/A 35
K	TO-3	3[2], 6[3]	35
L	Ceramic Leadless Chip Carrier (CLCC)	15	70
S	Side Brazed	25	90

NOTES: 1) This data is Junction to Tab
2) Junction to Bottom Plate
3) Junction to Top Plate

JAN PART NUMBERING SYSTEM

J M38510/ 117 04 B Y C

JAN DESIGNATOR	GENERAL PROCUREMENT SPEC	REFERS TO DETAIL SPEC	DEFINES DEVICE TYPE	PROCESSING LEVEL	PACKAGE TYPE	LEAD FINISH
Cannot be marked with "J" prefix unless qualified on Part I or Part II of the QPL		107 Positive Fixed Voltage Regulators 115 Negative Fixed Voltage Regulators 117 Positive Adjustment Voltager Regulators 118 Negative Adjustables Voltage Regulators 128 Voltage Mode PWMs 702 Current Mode PWM		S B C	A 14-lead 1/4 x 1/4 Flatpak C 14-lead 1/4 x 3/4 Flatpak O 14-lead 1/4 x 3/8 Flatpak E 16-lead 1/4 x 7/8 Flatpak F 14-lead 1/4 x 3/8 Flatpak 8 lead Can H 10-lead 1/4 x 1/4 Flatpak 1 10-lead Can J 24-lead 1/2 x 11/4 Dip K 24-lead 3/8 x 5/8 Flatpak P 8-lead 1/4 x 3/8 DIP V 18-lead 1/4 x 1 Dip 3 28-lead 1/2 x 1/2 LCC X Note Y Note Z Note U Note T Note N Note	A Hot Solder Dip B Tin Plate C Gold Plate X Any Finish

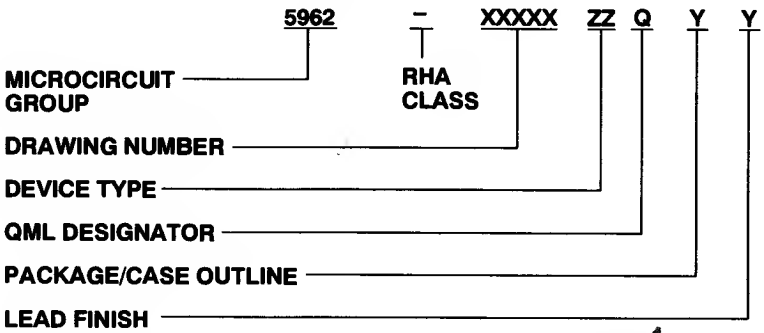
NOTE: Military package types X,Y,Z,U,T, and N are "wild card" designators reserved for packages not yet specified in M38510 (e.g. 2 lead TO-3 can, 3 lead TO-5 can, etc.) Their [illegible] counterparts vary [illegible] drawing to another. Refer to the detail spec for the correct package type designator. For additional information [illegible] use of X,Y,Z,U,T,N refer to MIL-M-38510 APPENDIX C, TABLE C-1, NOTE [illegible].

NEW PART NUMBERING SYSTEM FOR MILITARY PRODUCT

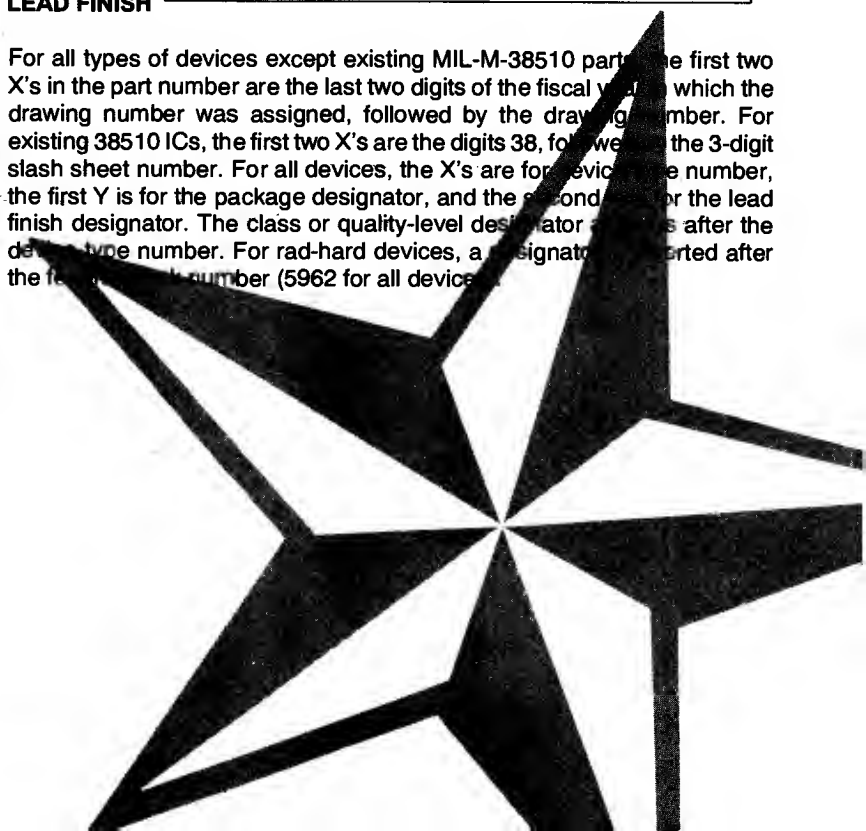
DESC has recommended a one part, one part number system which has been widely accepted throughout the industry. At the present time, the new numbering system has been incorporated into all NEW 38510 slash sheets and SMD's starting 2, Jan 1990.

The new part number is as follows:

EXISTING DOCUMENT	NEW PART NUMBER	
MIL-M-38510	5962-3811704BYA	UC117/80362
MIL-STD-883 SMD	5962-8764502MEA	UC1524A SMD



For all types of devices except existing MIL-M-38510 part[illegible]e first two X's in the part number are the last two digits of the fiscal [illegible] which the drawing number was assigned, followed by the draw[illegible]mber. For existing 38510 ICs, the first two X's are the digits 38, fo[illegible] the 3-digit slash sheet number. For all devices, the X's are for[illegible]e number, the first Y is for the package designator, and the [illegible]r the lead finish designator. The class or quality-level des[illegible] after the de[illegible] number. For rad-hard devices, a [illegible]rted after the f[illegible] number (5962 for all device[illegible]



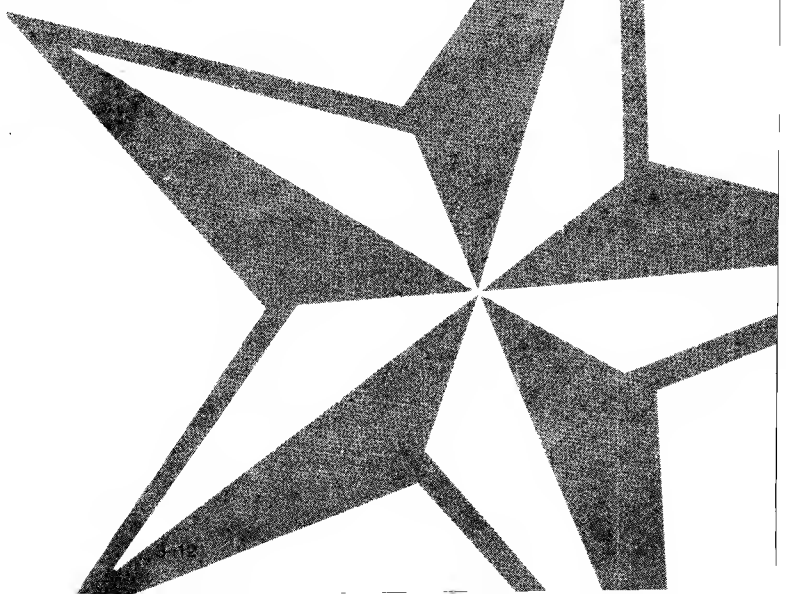
MILITARY PRODUCTS

U.I.C.C. QUALIFIED PRODUCTS CHART (QPL)

	GENERIC DEVICE	JAN-QPL PART NUMBER JM38510/
VOLTAGE REGULATORS	UC117K	11704BYA
	UC117K	11704BYC
	UC117H	11703BXA
	UC137K	11804BYA
	UC150K	11705BYA
	UC7805K	11706BYA
	UC7812K	11707BYA
	UC7815K	11708BYA
	UC7905K	11505BYA
	UC7912K	11506BYA
	UC7915K	11507BYA
PULSE WIDTH MODULATORS	UC1524J	12601BEA
	UC1525AJ	12602BEA
	UC1526J	12603BEA
	UC1846J	70201BEA

NOTES:
Unitrode Integrated Circuits Corp. (U.I.C.C.) is in a continuous mode of adding additional part numbers to the qualified parts list. Please call U.I.C.C. or your local Unitrode Sales Representative for updates and/or latest information.

Class S—Although UICC is not Class S certified, U.I.C.C. can supply any of our MIL temperature range products to customer drawings for Class S type product. U.I.C.C. can perform Class S screens per methods 5004 and 5005.



STANDARDIZED MILITARY DRAWINGS (SMDs) LISTING U.I.C.C. AS AN APPROVED SOURCE OF SUPPLY

LINEAR VOLTAGE REGULATORS	GENERIC DEVICE	TYPE	SMD PART NUMBER
	117AG/883BC	Positive Adjustable Reg.	7703405TA
	117AH/883BC	Positive Adjustable Reg.	7703405XA
	117AIG/883BC	Positive Adjustable Reg.	7703405UA
	117AK/883BC	Positive Adjustable Reg.	7703405YA
	117G/883BC	Positive Adjustable Reg.	7703401TA
	117H/883BC	Positive Adjustable Reg.	7703401XA
	117IG/883BC	Positive Adjustable Reg.	7703401UA
	117K/883BC	Positive Adjustable Reg.	7703401YA
	117L/883BC	Positive Adjustable Reg.	77034012A
	137AG/883BC	Negative Adjustable Reg.	7703406TA
	137AH/883BC	Negative Adjustable Reg.	7703406XA
	137AIG/883BC	Negative Adjustable Reg.	7703406UA
	137AK/883BC	Negative Adjustable Reg.	7703406YA
	137G/883BC	Negative Adjustable Reg.	7703403TA
	137H/883BC	Negative Adjustable Reg.	7703403XA
	137IG/883BC	Negative Adjustable Reg.	7703403UA
	137K/883BC	Negative Adjustable Reg.	7703403YA
	150AK/883BC	Positive Adjustable Reg.	5962-8767502XA
	150K/883BC	Positive Adjustable Reg.	5962-8767501XA
	1834J/883BC	Low Dropout Regulator	5962-8774201EA
	7805AG/883BC	Positive 5V Reg.	5962-8778201TA
	7805AIG/883BC	Positive 5V Reg.	5962-8778201UA
	7805AK/883BC	Positive 5V Reg.	5962-8778201YA
	7812AG/883BC	Positive 12V Reg.	5962-8777601TA
	7812AIG/883BC	Positive 12V Reg.	5962-8777601UA
	7812AK/883BC	Positive 12V Reg.	5962-8777601YA
	7815AG/883BC	Positive 15V Reg.	5962-8855301TA
	7815AIG/883BC	Positive 15V Reg.	5962-8855301UA
	7815AK/883BC	Positive 15V Reg.	5962-8855301YA
	7905AG/883BC	Negative 5V Reg.	5962-8874601TA
	7905AIG/883BC	Negative 5V Reg.	5962-8874601UA
	7905AK/883BC	Negative 5V Reg.	5962-8874601YA
	7912AG/883BC	Negative 12V Reg.	5962-8874701TA
	7912AIG/883BC	Negative 12V Reg.	5962-8874701UA
	7912AK/883BC	Negative 12V Reg.	5962-8874701YA
	7915AG/883BC	Negative 15V Reg.	5962-8874801TA
	7915AIG/883BC	Negative 15V Reg.	5962-8874801UA
	7915AK/883BC	Negative 15V Reg.	5962-8874801YA

MILITARY PRODUCTS

STANDARDIZED MILITARY DRAWINGS (SMDs) LISTING U.I.C.C. AS AN APPROVED SOURCE OF SUPPLY

	GENERIC DEVICE	TYPE	SMD PART NUMBER
PULSE WIDTH MODULATORS	1524AJ/883BC	PWM	5962-8764502EA
	1525AJ/883BC	PWM	5962-8951103EA
	1527AJ/883BC	PWM	5962-8951104EA
	1525AJ/883BC	PWM	5962-8951101EA
	1527AJ/883BC	PWM	5962-8951102EA
	1526AJ/883BC	PWM	8551502VA
	1526J/883BC	PWM	8551501VA
	1825J/883BC	High Speed PWM	5962-8768101EA
	1825L/883BC	High Speed PWM	5962-87681012A
	1842J/883BC	Current Mode PWM	5962-8670401PA
	1843J/883BC	Current Mode PWM	5962-8670402PA
	1844J/883BC	Current Mode PWM	5962-8670403PA
	1845J/883BC	Current Mode PWM	5962-8670404PA
	1846J/883BC	Current Mode PWM	5962-8680601EA
	1847J/883BC	Current Mode PWM	5962-8680602EA
POWER SUPERVISORY CIRCUITS	1543J/883BC	Power Supply Supervisory	5962-8774001EA
	1544J/883BC	Power Supply Supervisory	5962-8774002VA
	1903J/883BC	Quad Supply + Line Monitor	5962-8869701VA
	1903L/883BC	Quad Supply + Line Monitor	5962-88697012A
POWER DRIVERS	1706J/883BC	Dual Output Driver	5962-8961101EA
	1707J/883BC	Dual Channel Power Driver	5962-876190EA
	195H/883BC	Smart Power Transistor	5962-8777801XA
	195K/883BC	Smart Power Transistor	5962-8777801YA
OTHER FUNCTIONS	1611J/883BC	Quad Schottky Array	5962-8961101PA
	1637J/883BC	PWM DC Servo Control	5962-8995701VA
	1901J/883B	Iso. Feedback Generator	5962-8944101CA

MILITARY PRODUCTS

MIL-STD-883 QUALIFIED PRODUCTS

PRODUCT TYPE	GENERIC PART NUMBERS
VOLTAGE REGULATORS	UC117, UC137, UC150, UC7805/A, UC7812/A, UC7815/A, UC7905/A, UC7912/A, UC7915/A, UC1033
LOW DROP REGULATORS	UC1832, UC1833, UC1834, UC1835, UC1836
PULSE WIDTH MODULATORS	UC494/A, UC495/A, UC1524, UC1524A, UC1525A, UC1526/A, UC1823, UC1825, UC1840, UC1841, UC1842/A, UC1843/A, UC1844/A, UC1845/A, UC1846, UC1847, UC1851
RESONANT CONTROL	UC1860, UC1861, UC1864, UC1865
MOTOR CONTROL CIRCUITS	UC1517, UC1717, UC1622, UC1637, UC1625, UC1633, UC1634, UC1635, UC1720, UC1728
POWER SUPPLY SUPPORT CIRCUITS	UC195, UC1543, UC1544, UC1610, UC1611, UC1838A, UC1854 UC1901, UC1903
DRIVERS	UC1705, UC1706, UC1707, UC1708, UC1709, UC1710, UC1711
CHARGE PUMP CONVERTOR	UC1841

NOTE:
Please see individual data sheets for detail information.

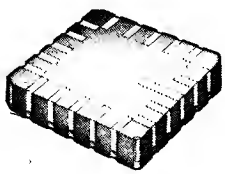
In addition to the compiant part number marking U.I.C.C. also signifies the class level for MIL-STD-883 processing (i.e., B or S)

MILITARY VOLTAGE REGULATORS
THREE TERMINAL FIXED AND ADJUSTABLE

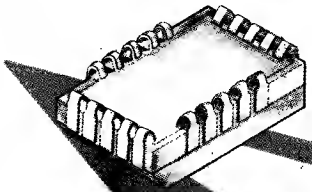
VOLTAGE REGULATOR SELECTION GUIDE

OUTPUT CURRENT	OUTPUT VOLTAGE	1% OUTPUT TOLERANCE	4% OUTPUT TOLERANCE	PACKAGES
0.5A	Adj. 1.2V to 57V Adj. 1.2V to 37V	UC117HV, UC117A UC117H		(H) TO-39 (L) Ceramic LCC
	Fixed +5 –5V +12 –12V +15 –15V	UC7805A UC7905A UC7812A UC7902A UC7815A UC7915A	UC7805 UC7905 UC7812 UC7912 UC7815 UC7915	(L) Ceramic LCC
1.5A	Fixed +5V	UC7805A, UC109	UC7805, UC109	(K) TO-3 (G) (IG) TO 257 (Hermetic)
	Fixed +12V	UC7812A	UC7812	
	Fixed +15V	UC7815A	UC7815	
	Adj. + 1.2V to +37V	UC117	UC117	
	Fixed -5V	UC7905A	UC7905	(K) TO-3 (G) (IG) TO 257 (Hermetic)
	Fixed -12V	UC7912A	UC7912	
	Fixed -15V	UC7915A	UC7915	
	Adj. –1.2V to +33V	UC137	UC137	
3.0A	Fixed -5	UC1890-5		(K) TO-3 (G) (IG) TO 257 (Hermetic)
	Adj. +1.2V to +37	UC150	UC150	
	Adj. –1.2V to –32V	UC1033	UC1033	

NOTE: See QPL or SMD listings for specific military part numbers.

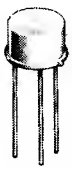


CERAMIC LCC (L)

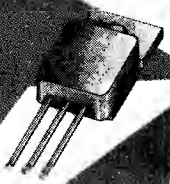


PLAS

TO-3 (K)



TO-39 (H)



ISOLATED

ISOL

TO 257 (G) (IG)

METIC

Radiation Hardened Bipolar Integrated Circuits

COMMITMENT TO PERFORMANCE

UNITRODE INTEGRATED CIRCUITS (U.I.C.C.)

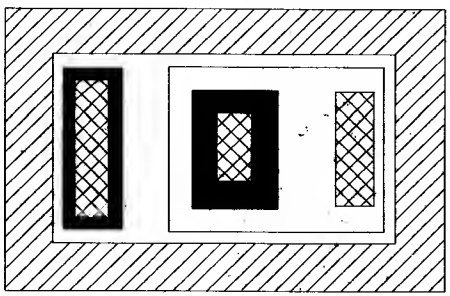
Has made a commitment not only to design innovative linear ICs but to develop unique processes to enhance their overall capabilities in harsh environments.

U.I.C.C. has the capability to design and manufacture radiation hardened integrated circuits to a wide range of customer requirements for military and space level applications.

Key to this capability is a proprietary, high density, cost effective, SOI process with full dielectric isolation. This process, developed as an alternative to junction isolation for all classes of linear circuits, exhibits electrical performance far superior to conventional circuits.

The ability for this process to withstand large radiation dose rates coupled with circuit design techniques to minimize effects to total dose, gives U.I.C.C. the means to supply circuits with a high degree of radiation hardening.

U.I.C.C. combines the use of enhanced design techniques in controlling and predicting both degradation and photocurrent compensation along with implementation of its's new dielectric isolation process in preventing the "Latch-up phenomina", during a radiation event. U.I.C.C.'s initial offering of radiation hardened designs will be in common device types of linear regulators followed by several of it's popular current mode PWMs.



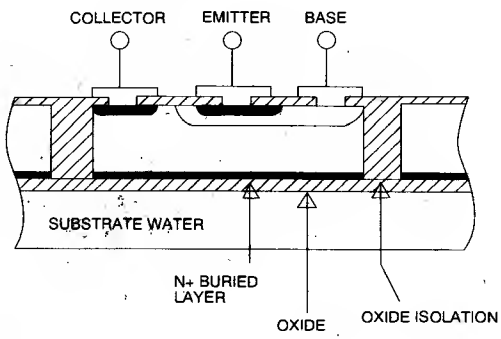
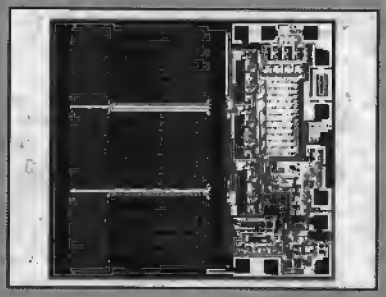
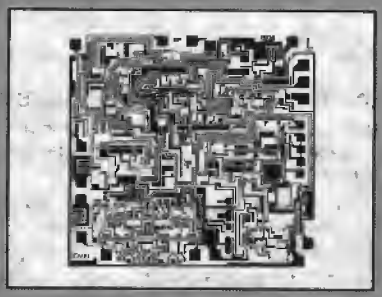


Figure 1 - Silicon Die and Wafer

MILITARY DIE CAPABILITY





HIGH RELIABILITY UNENCAPSULATED PRODUCTS

Unitrode's Military business unit offers all catalog circuits in unencapsulated form. Unencapsulated (chips) are supplied screened to MIL-STD-883B, method 2010, conditions A or B. Product is electrically tested at ambient room temperature. Shipment of this product is in individual waffle packs or as complete wafers.

For additional information contact your local Unitrode sales representative, or contact the factory.

MILITARY PRODUCTS RADIATION CAPABILITIES

RADIATION TOLERANT PRODUCTS

Unitrode recognizes the increasing market demand for radiation tolerant and radiation hardened high reliability products. Because of this we, in conjunction with customers, have characterized our key products. Several of Unitrode Linear IC's have been characterized as being radiation tolerant.

PULSE WIDTH MODULATORS

UCI825
UC1842
UCI843
UCI844
UCI845
UC1524A
UC1526
UC1526A

POWER FET DRIVERS

UC1711
UC1707

LOW DROP REGULATORS

UC1834
UC1835/36

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

4 POWER SUPPLY CIRCUITS

INTEGRATED CIRCUITS

UNITRODE

Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs

Note: Most series available screened to /883B Rev. C.

VOLTAGE MODE PWM's	PERFORMANCE CHARACTERISTICS																			
TYPE	Voltage Reference ±4%	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Oscillator Sync Terminal	Adjustable Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package Note 1
Regulating PWMs UC1524/2524/3524	X						X	100mA		300KHz	X								16 Pin N, J, *
Advanced Regulating PWMs UC1524A/2524A/3524A		X		X	X	X	X	200mA		500KHz	X						X		16 Pin N, J, *
Advanced Regulating PWMs UC1525A/2525A/3525A UC1527A/2527A/3527A		X	X	X	X		X	100mA 0.4A Pulse		500KHz			X	X	X				16 Pin N, J, *
Regulating PWMs UC1526/2526/3526		X	X	X	X	X	X	100mA		400KHz			X	X	X		X		18 Pin N, J, *
Advanced Regulating PWMs UC1526A/2526A/3526A		X	X	X	X	X	X	100mA		550KHz			X	X	X		X		18 Pin N, J *
High Frequency PWM Controllers UC1823/2823/3823		X	X	X	X	X		500mA 1.5A	X	2MHz		X	X	X	X		X	X	16 Pin N, J, *
UC1825/2825/3825		X	X	X	X	X		Pulse			X		X	X	X		X	X	
Regulating PWMs UC494	X							200mA		300KHz	X				X		X		16 Pin N, J
Advanced Regulating PWMs UC494A/UC494AC		X			X			200mA		300KHz	X				X		X		16 Pin N, J
UC495A/UC495AC																			18 Pin N, J
Programmable Primary Side PWMs UC1840/2840/3840		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J, *
Programmable Primary Side PWMs UC1841/2841/3841		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J, *
Power Supply Control System UC2850/3850	X		X	X	X	X	X	50mA		200KHz	X			X	X		X		24 Pin N, J, *
Advanced Programmable, Off-line PWM UC1851/3851		X	X	X	X	X	X	200mA	X	500KHz		X	X		X	X	N/A	X	18 Pin N, J, *
High Current Buck Regulator L296		X	X	X		X	X	4A		200KHz		X					X		15 Pin Multiwatt® V, VH

*NOTE 1: All current Mode Control IC's can be used in "Voltage Mode" Also, consult Current Mode PWM Selection Guide.

NOTE 2: N = Plastic Package
J = Ceramic Package

* = Surface Mount Available, Consult Factory

Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs

Note: Most series available screened to /883B Rev. C.

CURRENT MODE TYPE	PERFORMANCE CHARACTERISTICS																				
	Accurate Oscillator Discharge Current	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Oscillator Sync Terminal	Accurate Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package Note 1
High Frequency PWM Controllers																					
UC1823/2823/3823		X	X	X	X	X		500mA 1.5A Pulse	X	2MHz		X	X	X	X		X	X	16 Pin N, J, *
UC1825/2825/3825		X	X	X	X	X					X		X	X	X		X	X	
High Frequency PWM Controllers																					
UC1823A/2823A/3823A	X	X	X	X	X	X		500mA 1.5A Pulse	X	2MHz		X	X	X			X	X	16 Pin N, J, *
UC1825A/2825A/3825A	X	X	X	X	X	X					X		X	X	X		X	X	
Current Mode PWM Controllers																					
UC1846/2846/3846		X	X	X	X	X	X	200mA	X	500KHz			X	X	X	X	X		16 Pin N, J, *
UC1847/2847/3847																					
Current Mode PWM Controllers																					
UC1846A/2846A/3846A	X	X	X	X	X	X	X	200mA	X	500KHz			X	X	X	X	X		16 Pin N, J, *
Economy Primary Side PWMs																					
UC1842/2842/3842								100mA 1A Pulse													
UC1843/2843/3843		X		X	X	X			X	500KHZ		X			X		N/A	X	8 Pin N, J, *
UC1844/2844/3844																					
UC1845/2845/3845																					
Programmable Primary Side PWMs																					
UC1840/2840/3840		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	16 Pin N, J, *
Programmable Primary Side PWMs																					
UC1841/2841/3841		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J, *
Economy Primary Side PWMs																					
UC1842A/2842A/3842A								100mA 1A Pulse													
UC1843A/2843A/3843A		X		X	X	X			X	500KHz		X			X		N/A	X	8 Pin N, J, *
UC1844A/2844A/3844A																					
UC1845A/2845A/3845A																					
Advanced Programmable, Off-line PWM																					
UC1851/3851		X	X	X	X	X	X	200mA	X	500KHz		X	X		X	X	N/A	X	18 Pin N, J, *

Note 1: N = Plastic Package
J = Ceramic Package
* = Surface Mount Available, Consult Factory

Power Supply Controls

Current Mode Application Guide

CURRENT MODE CONTROL IC APPLICATION GUIDE

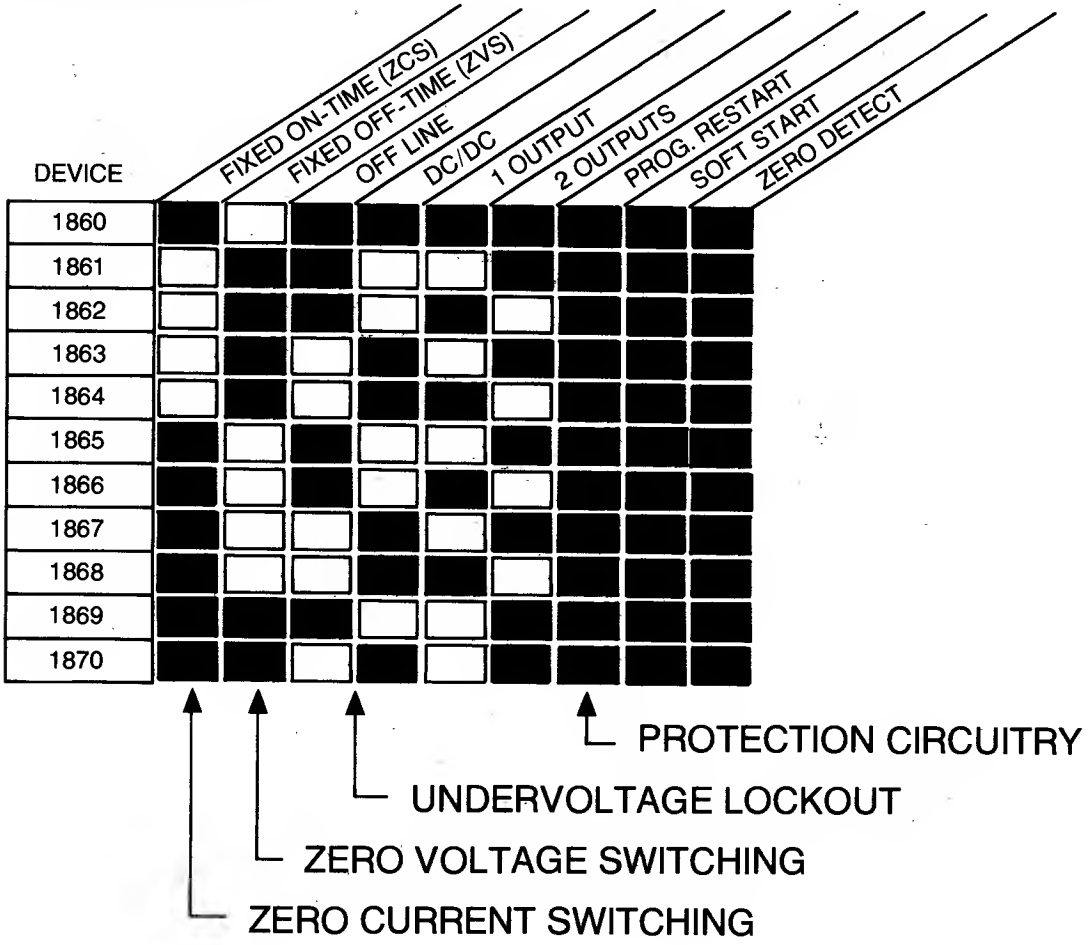
Note: Most series available screened to /883B Rev. C.

	OFF LINE	DC/DC	BUCK REGULATOR	BOOST	FORWARD (<50% MAX DUTY)	FLYBACK (<50% MAX DUTY)	FORWARD (>50% MAX DUTY)	FLYBACK (>50% MAX DUTY)	HALF-BRIDGE	FULL-BRIDGE	PUSH-PULL	PROTECTION FEATURES INCLUDED
1823	X	X	X	X			X	X				X
1825	X	X			X	X			X	X	X	X
1823A	X	X	X	X	X	X	X	X				X
1825A	X	X			X	X			X	X	X	X
1840	X	X	X	X			X	X	☆	☆	☆	X
1841	X	X	X	X			X	X	☆	☆	☆	X
1842	X		X	X			X	X	☆	☆	☆	
1843		X	X	X			X	X	☆	☆	☆	
1844	X				X	X						
1845		X			X	X						
1842A	X		X	X			X	X	☆	☆	☆	
1843A		X	X	X			X	X	☆	☆	☆	
1844A	X				X	X						
1845A		X			X	X						
1846	X	X			X	X			X	X	X	X
1847	X	X			X	X			X	X	X	X
1846A	X	X			X	X			X	X	X	X
1847A	X	X			X	X			X	X	X	X
1851	X	X			X	X						X

☆ Use UC1706 Mosfet Driver for Single to Dual Output Conversion

Power Supply Controls

Resonant Mode Control IC's



POWER SUPPLY SUPPORT FUNCTIONS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1543/2543/3543 UC1544/2544/3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	• Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC1544 Series only)	16 Pin DIL (1543 Series) 18 Pin DIL (1544 Series)
UC1705/2705/3705 UC1706/2706/3706 UC1707/2707/3707 UC1708/3708 UC1709/3709 UC1710/3710 UC1711/3711	See Power Driver & Interface Circuit Section		
UC1832/2832/3832 UC1833/2833/3833	Precision Low Dropout Linear Regulator Low Cost Linear High Efficiency Linear Regulator	• Precision 1% Reference • Over-Current Sense Threshold Accurate to 5% • Programmable Duty-Ratio Over-Current Protection • 4.5V to 36V Operation • 100mA Output Drive, Source or Sink • Under-Voltage Lockout **Additional Features of the UC1832 series:** • Adjustable Current Limit to Current Sense Ratio • Separate $+V_{in}$ terminal • Programmable Driver Current Limit • Access to V_{REF} and E/A(+) • Logic-Level Disable Input	(1832 series) 14 Pin DIL (1833 series) 8 Pin DIL
UC1834/2834/3834	High Efficiency Linear Regulator, Low Input-Output Differential	• Minimum V_{IN} — V_{OUT} less than 0.5V at 5A Load with External Pass Device • Equally Usable for either Positive or Negative Regulator Design • Adjustable Low Threshold Current Sense Amplifier • Under-and Over-Voltage Fault Alert with Programmable Delay • Over-Voltage Fault Latch with 100mA Crowbar Drive Output	16 Pin DIL
UC1835/2835/3835 UC1836/2836/3836	High Efficiency Regulator Controllers 5V Fixed (1835 Series) Adjustable (1836 Series)	• Complete Control for High Current Low Dropout Linear Regulator • Accurate 2.5A Current Limiting with Foldback • Internal Current Sense • External Shutdown	8 Pin DIL
UC1838A/2838A/3838A	Magnetic Amplifer Controller	• Indpendent 1% Reference • Two Uncommitted, Identical Op Amps • 100mA Reset Current Source with - 120V capability	16 Pin DIL Power Pkg.
UC1901/12901/3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	• An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock	14 Pin DIL
UC1903/2903/3903	Quad Supply and Line Monitor Precision System	• Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP	18 Pin DIL

PRODUCT APPLICATIONS CIRCUITS

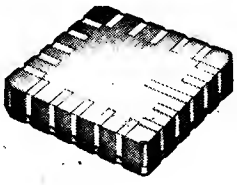
PRODUCT SERIES	TYPICAL APPLICATIONS
UC1611/2611/3611 Quad Schottky Array For other similar product refer to UC1610/3610 Schottky Array	• Matched, Four Diode Monolithic Array • High Peak Current • Low Cost MINIDIP Package • Low Forward Voltage • Parallelable for Lower V_F or Higher V_F • Fast Recovery Time • Military Temperature Range
UC3704 Bridge Transducer Switch	Any Analog to Digital monitoring system; coupled with any of a wide range of sensors almost any type of physical phenomena may be monitored. Samples: • Air-Flow Sensor Circuits • Liquid or Gas Flow Circuits • Passing Object Circuits
UC1906/2906 Lead-Acid Battery Charger	"IC Circuitry that results in optimized charge cycles for specific battery applications." • Uninterruptable Power Supplies • Portable Electrical Equipment • Emergency Power and Light Systems • Volatile Data Handling Computers—Power Back-Up
UC1730/2730/3730 Temperature and Air Flow Sensor	By combining a temperature monitor and heater, this IC permits airflow velocity past the IC package to be mointored. • On-Chip Temperature Transducer • Temperature Comparator Gives Threshold Temp-Airflow Alarm • Low 2.5mA Quiescent Current
LT1054M LT1054C Charge Pump Convertor	• 3.5V to 15V operation as a convertor • Low voltage loss • 100mA output current • Low 2.5mA quiescent current • Reference and error amplifier for regulation • External shutdown • Can be paralleled
ISDN Primary Side Current Motor Controller	• Can Function as a General-purpose Low-power Controller • Fully Synchronizing Oscillator • Synchronization to Secondary side Logic • Leading Edge Blanking of Current Sense • 50% Maximum Duty Cycle • Undervoltage Lockout • Programmable Low Line Sensing • Programmable Softstart • Programmable Fault/Restart Delay **ISDN FEATURES** • Zero-power Startup Capability • Restricted Mode Detection • Frequency Agile PWM in Restricted Mode • Precision Programmable Quiescent Current • Very Low Quiescent Power for CCITT 25mW Restricted Mode • Accurate, Programmable Input Power Limit or Input Current Limit
ISDN Seconday Regulator	• Wide Operating Range. • Fully Synchronized Oscillator • Temperature stable Oscillator • Logic Level Synchronization Input • Precision Reference • Error Amplifier for Loop Regulation and Compensation • Undervoltage Lockout **ISDN FEATURES** • Low Line Logic Output • Restricted Mode Logic Output • Precision Programmable Quiescent Current • Very Low Quiescent Power for CCITT 25mW Restricted Mode

THREE TERMINAL FIXED AND ADJUSTABLE REGULATORS

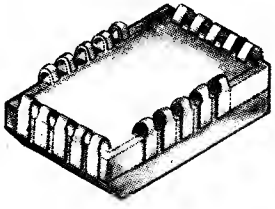
VOLTAGE REGULATOR SELECTION GUIDE

OUTPUT CURRENT	OUTPUT VOLTAGE	1% OUTPUT TOLERANCE	4% OUTPUT TOLERANCE	PACKAGES
0.5A	Adj. 1.2V to 57V Adj. 1.2V to 37V	UC117HV UC117H		(H) TO-39 (L) Ceramic LCC
	Fixed +5 –5V +12V –12V +15V –15V	UC7805A UC7905A UC7812A UC7902A UC7815A UC7915A	UC7805 UC7905 UC7812 UC7912 UC7815 UC7915	(L) Ceramic LCC
1.5A	Fixed +5V	UC7805A	UC7805	(K) TO-3 (G) (IG) TO-257 (Hermetic)
	Fixed +12V	UC7812A	UC7812	
	Fixed +15V	UC7815A	UC7815	
	Adj. +1.2V to +37V	UC117	UC117	
	Fixed –5V	UC7905A	UC7905	(K) TO-3 (G) (IG) TO-257 (Hermetic)
	Fixed –12V	UC7912A	UC7912	
	Fixed –15V	UC7915A	UC7915	
	Adj. –1.2V to +33V	UC137	UC137	
3.0A	Fixed –5V	UC1890-5		(K) TO-3 (G) (IG) TO-257 (Hermetic)
	Adj. +1.2V to +37V	UC150	UC150	
	Adj. –1.2V to –32V	UC1033, UC3033	UC1033, UC3033	

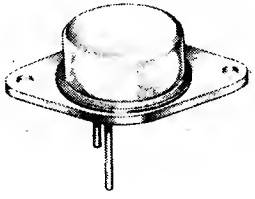
NOTE: See QPL or SMD listings for specific military part numbers



CERAMIC LCC (L)

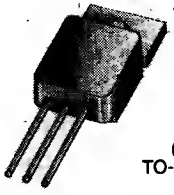


PLASTIC PLCC



TO-3 (K)
G= NON ISOLATED CASE
IG = ISOLATED CASE

TO-39 (H)



(Similar to TO-220 package)

TO-257 HERMETIC

INTEGRATED CIRCUITS
UNITRODE

LAS 1900 SERIES

5 AMP POSITIVE VOLTAGE REGULATORS

FEATURES

- Guaranteed Power Dissipation 50 Watts @ 80°C Case
- Guaranteed input-output differential: + 2.6 Volts
- Low noise, band gap reference
- Remote sense capability
- Sample power cycled burn-in
- Guaranteed thermal resistance junction to case: 0.9°C/W
- Available in TO-3 and TO-247 packages
- Grounded case

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNITS
Input Voltage	V_{IN}		30(35)[1][2]	Volts
Power Dissipation	P_D		Internally Limited[3]	
Thermal Resistance Junction To Case	θ_{JC}		0.9	°C/Watt
Operating Junction Temperature Range	T_J			°C
LAS 1900		−55	150	
LAS 19U				
LAS1900P		0	125	
Storage Temperature Range	T_{STG}	−65	150	°C
Lead Temperature (Soldering, 60 Seconds Time Limit)	T_{LEAD}		300	°C

[1] Short circuit protection is only assured to V_{IN} max. Value of 30V applies to V_O of −5V to −12V. Value of 35V applies to V_O of 15V and LAS 19U.
[2] In case of short circuit with input-output voltages approaching V_{IN} max, regulator may require the removal of the input voltage to restart.
[3] For operation above 80°C T_{CASE}, derate @ 1 111 watt °/C.

DEVICE SELECTION GUIDE

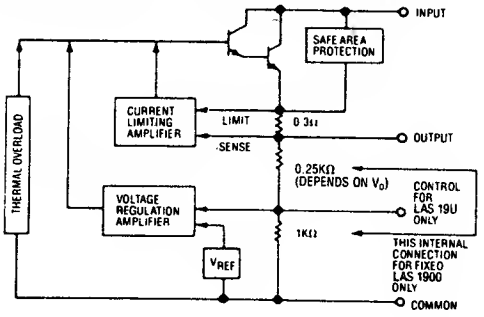
V_{OUT}	V_{OUT} TOLERANCE		
	±5%	+5%, −3%	±2%
5	LAS 1905	LAS 1905B	LAS 19A05
	LAS 1905P	LAS 1905BP	LAS 19A05P
12	LAS 1912	LAS 1912B	LAS 19A12
	LAS 1912P	LAS 1912BP	LAS 19A12P
4 to 30	LAS 19U (Adjustable/Remote Sense)		

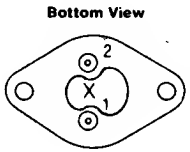
DESCRIPTION

The LAS 1900 Series voltage regulators are monolithic integrated circuits designed for use in applications requiring a well regulated positive output voltage. Outstanding features include full power usage up to 5.0 amperes of load current, internal current limiting, thermal shutdown, and safe area protection on the chip, providing protection of the series pass Darlington, under most operating conditions. Hermetically sealed copper and copper/steel TO-3 packages are utilized for high reliability and low thermal resistance, while the TO-247 package is intended for cost effective designs. A low-noise, temperature stable band gap reference is the key design factor insuring excellent temperature regulation of the LAS 1900 Series. This, coupled to a very low output impedance, insures superior load regulation.

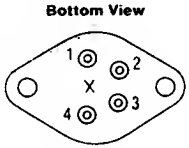
The LAS 19U, a four terminal, adjustable regulator is available with an output range from +4 to +30 Volts, providing remote sense capability with a single potentiometer.

BLOCK DIAGRAM





1 – Input
2 – Output
Case is common



1 – Common
2 – Control
3 – Output
4 – Input
Case is common

1 – Input
2 – Common
3 – Output
Tab Is Common

NOTE: Case temperature measured at point X.

ELECTRICAL CHARACTERISTICS

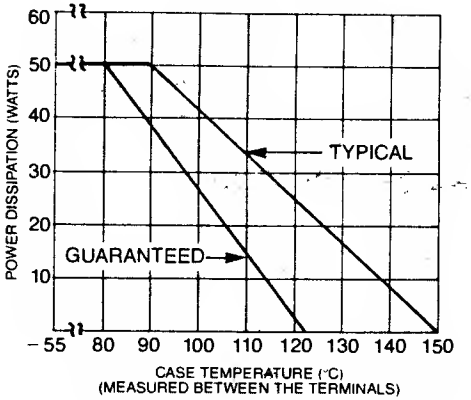
Input voltage test conditions are as follows: $V_1 = V_O + 3$ Volts, $V_2 = V_O + 10$ Volts, $V_3 = V_O + 15$ Volts, or the maximum input, whichever is less.

		Test Conditions			Test Limits		
Parameter	**Symbol**	**V_{IN}**	**I_O**	**T_J**	**Min**	**Max**	**Units**
Output Voltage[2] LAS 1900[1] LAS 1900B[1] LAS 19A00[1] LAS 19U[5]	V_O	V_1 to V_2	10mA to 5.0A	25°C	 $0.95\|V_O\|$ $0.97\|V_O\|$ $0.98\|V_O\|$ 4.0	 $1.05\|V_O\|$ $1.05\|V_O\|$ $1.02\|V_O\|$ 30.0	Volts
Input-Output Differential	V_{IN}-V_O		5.0A	0-125°C	2.6		Volts
Line Regulation[2]	$REG_{(LINE)}$	V_1 to V_3	3.0A	25°C		1.0	$\%V_O$
Load Regulation[2]	$REG_{(LOAD)}$	V_1	10mA to 5.0A	25°C		0.6	$\%V_O$
Quiescent Current	I_Q	V_1	10mA	25°C		25.0	mA
Quiescent Current Line	$I_{Q\ (LINE)}$	V_1 to V_2	10mA	25°C		5.0	mA
Quiescent Current Load	$I_{O\ (LOAO)}$	V_1	10mA to 5.0A	25°C		5.0	mA
Current Limit[2]	I_{LIM}	$V_O + 5V$		25°C		15	Amps
Temperature Coefficient	T_C	V_1	0.1A	0-125°C		0.03	$\%V_O$/°C
Output Noise[3] Voltage	V_N	V_1	0.1A	0-125°C		10	$\mu V_{rms}/V$
Ripple Attenuation[4]	R_A	$V_O + 5V$	2.0A	0-125°C	60		dB
Control Voltage LAS 19U	V_C	V_1 to V_2	10mA	25°C	3.6	4.0	Volts
Power Dissipation	P_O	V_{IN}-V_{OUT} 2.6V to 10.0V	10mA to 5.0A	0-125°C		50	Watts

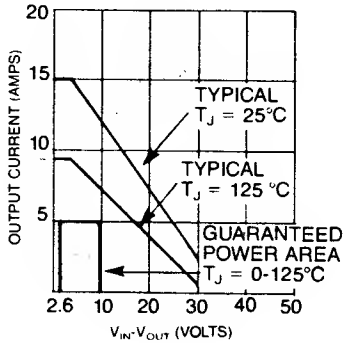
(1) Nominal output voltages are specified under Device Selection Guide.
(2) Low duty cycle pulse testing with Kelvin connections required. Die temperature changes must be accounted for separately.
(3) BW = 10Hz - 100KHz
(4) Ripple attenuation is specified for a 1Vrms, 120Hz, input ripple.
Ripple attenuation is minimum of 60 dB at 5V output and is 1 dB less for each volt increase in the output voltage.
(5) $V_O = V_C (1 + R1/R2)$
R1 = Resistance from output to control
R2 = Resistance from control to common

OPERATIONAL DATA

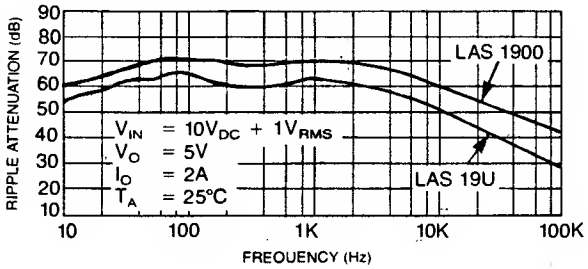
POWER DERATING



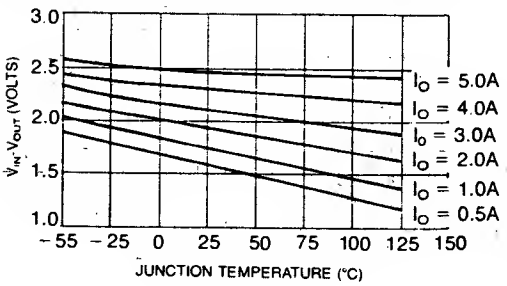
CURRENT LIMIT



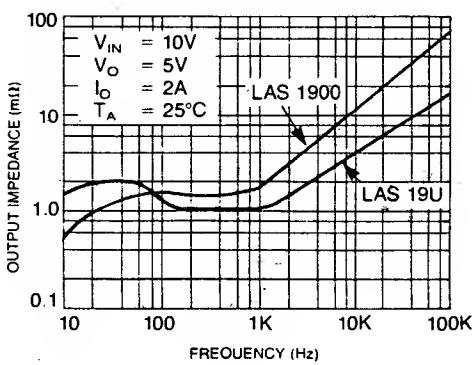
TYPICAL RIPPLE ATTENUATION VS FREQUENCY



TYPICAL INPUT-OUTPUT VOLTAGE DIFFERENTIAL VS JUNCTION TEMPERATURE

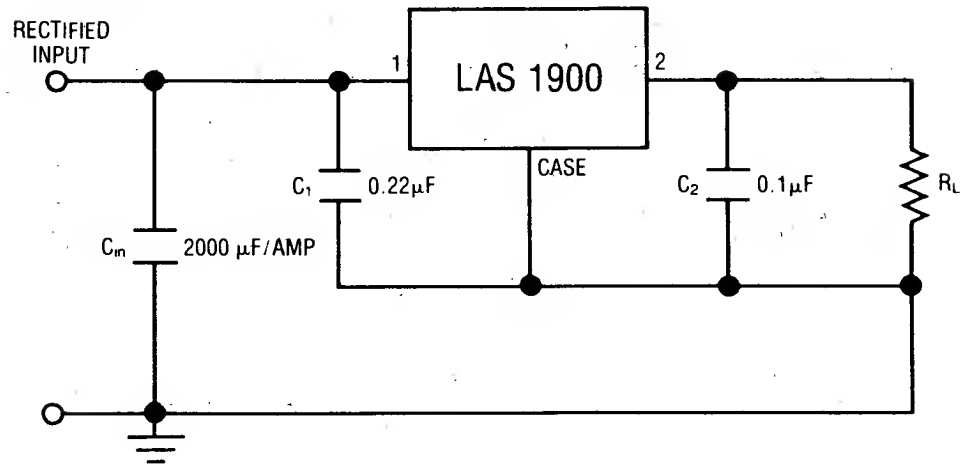


TYPICAL OUTPUT IMPEDANCE VS FREQUENCY

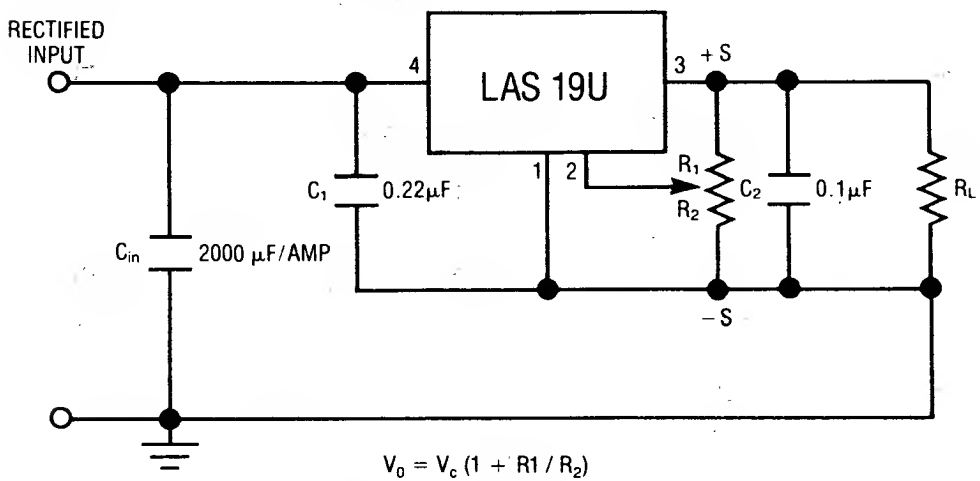


TYPICAL APPLICATIONS

FIXED VOLTAGE REGULATOR [1]



ADJUSTABLE VOLTAGE REGULATOR [1,2]



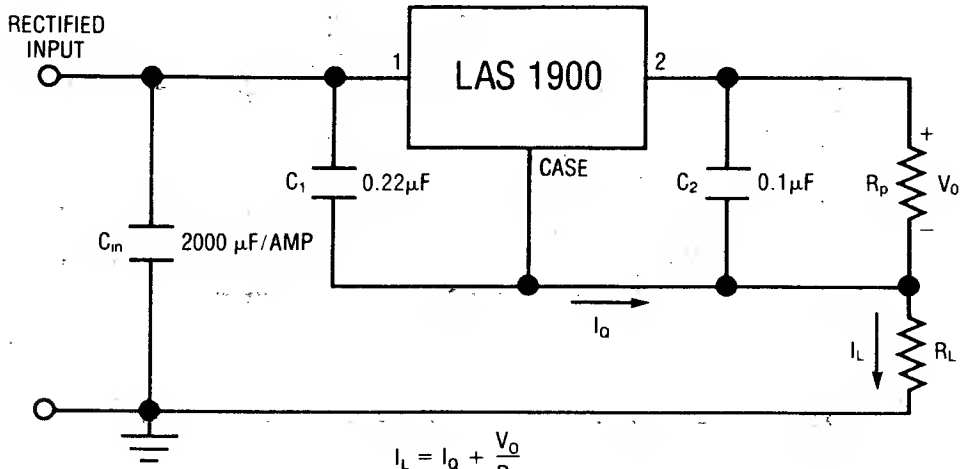
$$V_o = V_c (1 + R1 / R_2)$$

[1] C_1 and C_2 should be placed as close as possible to the regulator.

[2] $\frac{V_o}{R_1 + R_2} \geq 10$ mA

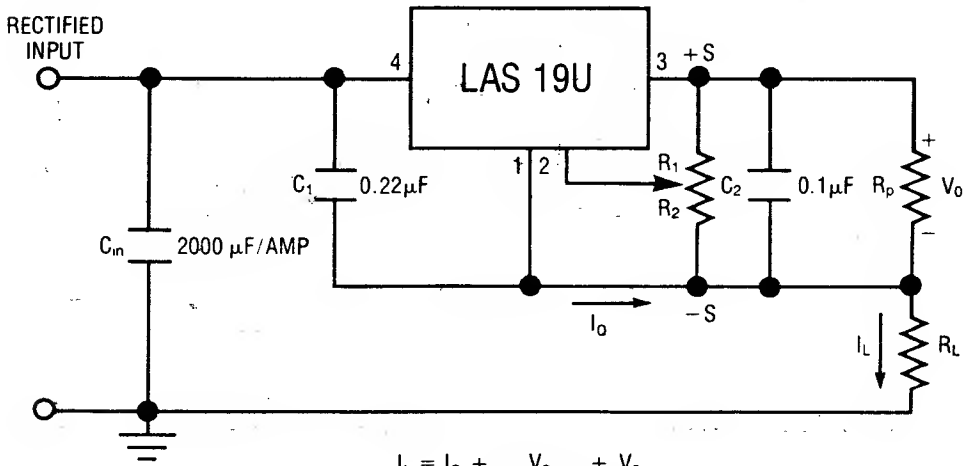
TYPICAL APPLICATIONS

FIXED CURRENT REGULATOR[1]



$$I_L = I_Q + \frac{V_O}{R_p}$$

ADJUSTABLE CURRENT REGULATOR[1,2]



$$I_L = I_Q + \frac{V_O}{R_1 + R_2} + \frac{V_O}{R_p}$$

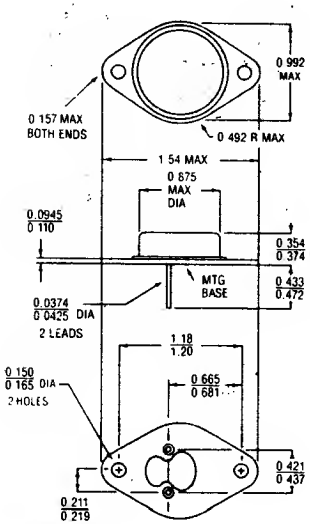
$$V_O = V_c\,(1 + R_1 / R_2)$$

[1] C_1 and C_2 should be placed as close as possible to the regulator.

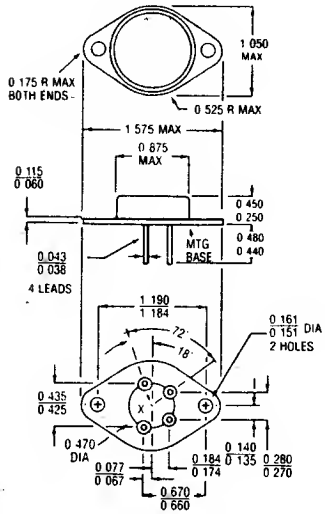
[2] $\frac{V_O}{R_1 + R_2} \geq 10$ mA

DEVICE OUTLINE

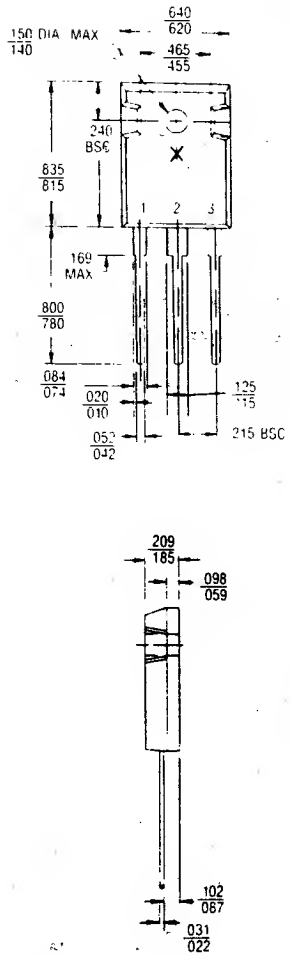
TO-3 (COPPER/STEEL)



TO-3



TO-247



All dimensions are in inches.

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INTEGRATED CIRCUITS
UNITRODE

8 AMP POSITIVE VOLTAGE REGULATORS

LAS 3900 SERIES

FEATURES

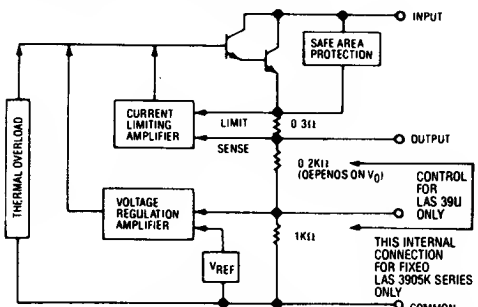
- Guaranteed Power Dissipation 80 Watts @ 69°C Case
- Guaranteed input-output differential: + 2.6 Volts
- Low noise, band gap reference
- Remote sense capability
- Sample power cycled burn-in
- Guaranteed thermal resistance junction to case: 0.7°C/W

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNITS
Input Voltage	V_{IN}		25(1) (2)	Volts
Power Dissipation	P_D		Internally Limited(3)	
Thermal Resistance Junction To Case	θ_{JC}		0.7	°C/Watt
Operating Junction Temperature Range	T_J	−55	150	°C
Storage Temperature Range	T_{STG}	−65	150	°C
Lead Temperature (Soldering, 60 Seconds Time Limit)	T_{LEAD}		300	°C

(1) Short circuit protection is only assured to V_{IN} = 25V max.
(2) In case of short circuit, with input-output voltages approaching 25V, regulator may require the removal of the input voltage to restart.
(3) For operation above 69°C T_{CASE}, derate @ 1.42 Watt/°C.

BLOCK DIAGRAM



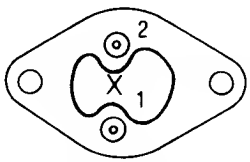
LAS 3905K, LAS 39U

Note: See p. 3 for LAS 3905 Block Diagram

DESCRIPTION

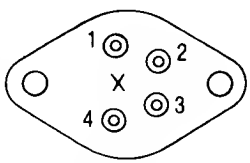
The LAS 3900 Series voltage regulators are monolithic integrated circuits designed for use in applications requiring a well regulated positive output voltage. Outstanding features include full power usage up to 8.0 amperes of load current, internal current limiting, thermal shutdown, and safe area protection on the chip, providing protection of the series pass Darlington, under most operating conditions. Hermetically sealed copper and copper/steel TO-3 packages are utilized for high reliability and low thermal resistance. A low-noise, temperature stable band gap reference is the key design factor insuring excellent temperature regulation of the LAS 3900 Series. This, coupled to a very low output impedance, insures superior load regulation.

The LAS 39U, a four terminal, adjustable regulator is available with an output range from +4 to +16 volts, providing remote sense capability with a single potentiometer.



LAS 3905K

1 — Input
2 — Output
Case Is Common



LAS 3905

1 — Input
2 — Common
3 — Sense
4 — Output
Case Is Common

LAS 39U

1 — Common
2 — Control
3 — Output
4 — Input
Case Is Common

NOTE: Case temperature measured at point X.

ELECTRICAL CHARACTERISTICS

Input voltage test conditions are as follows: $V_1 = V_0 + 3$ Volts, $V_2 = V_0 + 10$ Volts, $V_3 = V_0 + 15$ Volts, or the maximum input, whichever is less.

		Test Conditions			Test Limits		
Parameter	**Symbol**	**V_{IN}**	**I_O**	**T_J**	**Min**	**Max**	**Units**
Output Voltage[2] LAS 3905[1] LAS 3905K[1] LAS 39A05, 39A05K[1] LAS 39U[5]	V_O	V_1 to V_2	10mA to 8.0A	25°C	 $0.95\|V_O\|$ $0.97\|V_O\|$ $0.98\|V_O\|$ 4.0	 $1.05\|V_O\|$ $1.05\|V_O\|$ $1.02\|V_O\|$ 16	Volts
Input-Output Differential	V_{IN}-V_O		8A	0-125°C	2.6		Volts
Line Regulation[2]	$REG_{(LINE)}$	V_1 to V_3	5A	25°C		2.0	$\%V_O$
Load Regulation[2]	$REG_{(LOAD)}$	V_1	10mA to 8.0A	25°C		0.6	$\%V_O$
Quiescent Current	I_O	V_1	10mA	25°C		20.0	mA
Quiescent Current Line	$I_{O\ (LINE)}$	V_1 to V_2	10mA	25°C		5.0	mA
Quiescent Current Load	$I_{O\ (LOAD)}$	V_1	10mA to 8.0A	25°C		5.0	mA
Current Limit[2]	I_{LIM}	$V_O + 5V$		25°C		18	Amps
Temperature Coefficient	T_C	V_1	0.1A	0-125°C		0.03	$\%V_O$/°C
Output Noise[3] Voltage	V_N	V_1	0.1A	0-125°C		10	$\mu V_{rms}/V$
Ripple Attenuation[4]	R_A	$V_O + 5V$	2.0A	0-125°C	60		dB
Control Voltage LAS 39U	V_C	V_1 to V_2	10mA	25°C	3.6	4.0	Volts
Power Dissipation	P_O	V_{IN}-V_{OUT} 2.6V to 10.0V	10mA to 8A	0-125°C		80	Watts

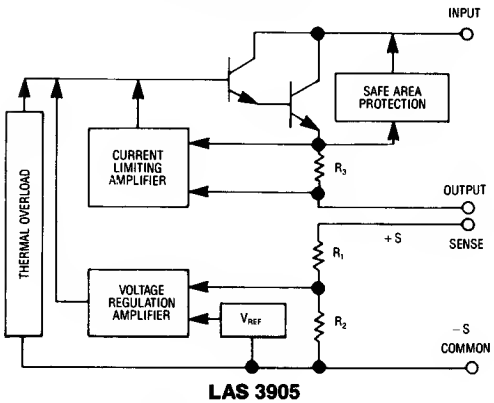
(1) Nominal output voltages are specified under Device Selection Guide.
(2) Low duty cycle pulse testing with Kelvin connections required. Die temperature changes must be accounted for separately.
(3) BW = 10Hz - 100KHz
(4) Ripple attenuation is specified for a 1Vrms, 120Hz, input ripple.
Ripple attenuation is minimum of 60 dB at 5V output and is 1 dB less for each volt increase in the output voltage.
(5) $V_O = V_C (1 + R1/R2)$
R1 = Resistance from output to control
R2 = Resistance from control to common

DEVICE SELECTION GUIDE

V_{OUT}	V_{OUT} TOLERANCE		
	±5%	+5%, −3%	±2%
5	LAS 3905*	LAS 3905K	LAS 39A05*, 39A05K
4 to 16	LAS 39U* (Adjustable)		

*Remote Sense Capability

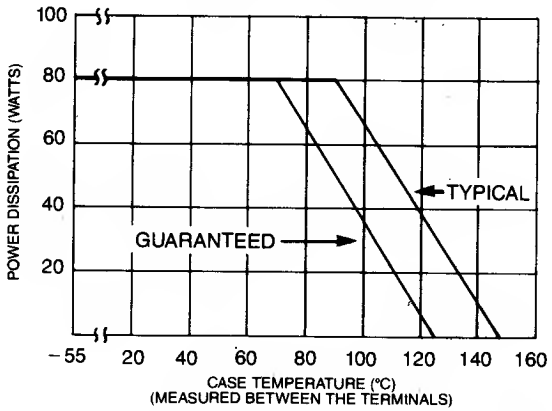
BLOCK DIAGRAM



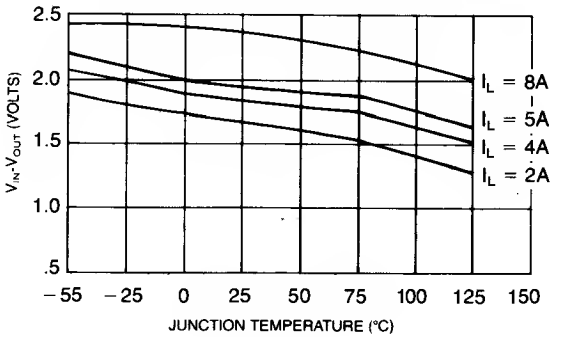
LAS 3905

OPERATIONAL DATA

POWER DERATING

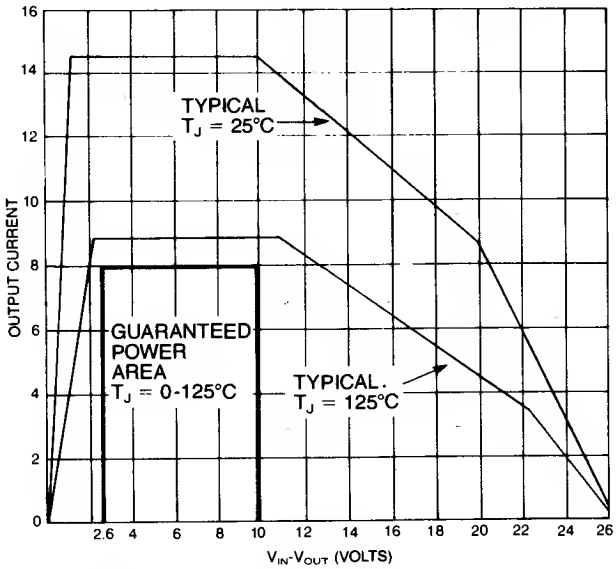


TYPICAL INPUT-OUTPUT VOLTAGE DIFFERENTIAL VS JUNCTION TEMPERATURE

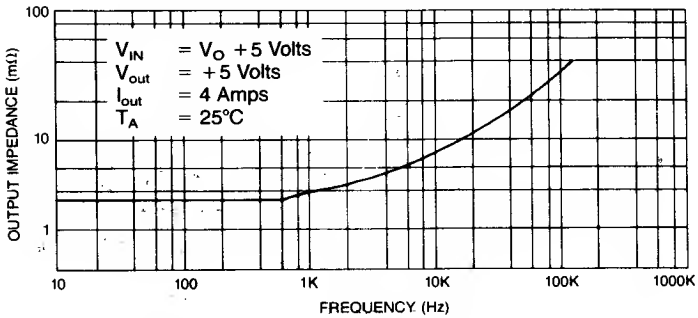


OPERATIONAL DATA

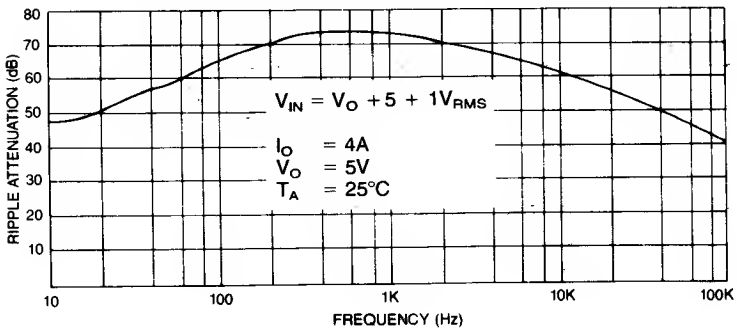
CURRENT LIMIT



TYPICAL OUTPUT IMPEDANCE VS FREQUENCY

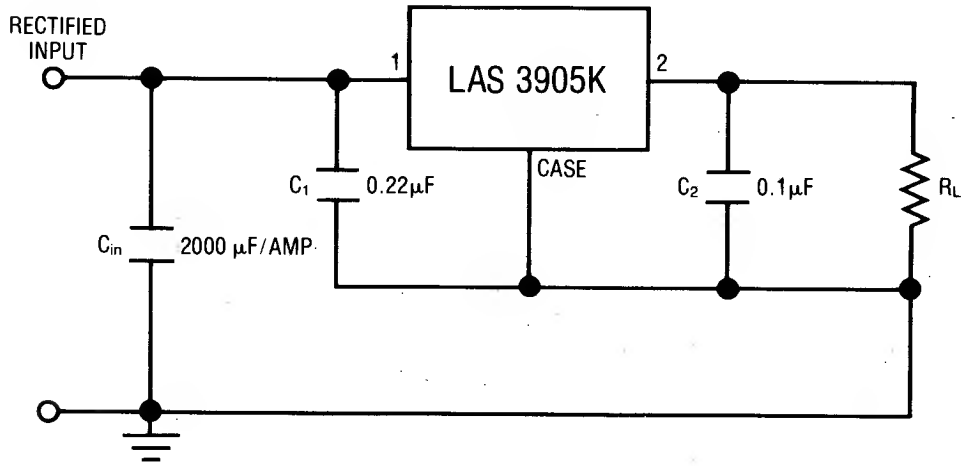


TYPICAL RIPPLE ATTENUATION VS FREQUENCY

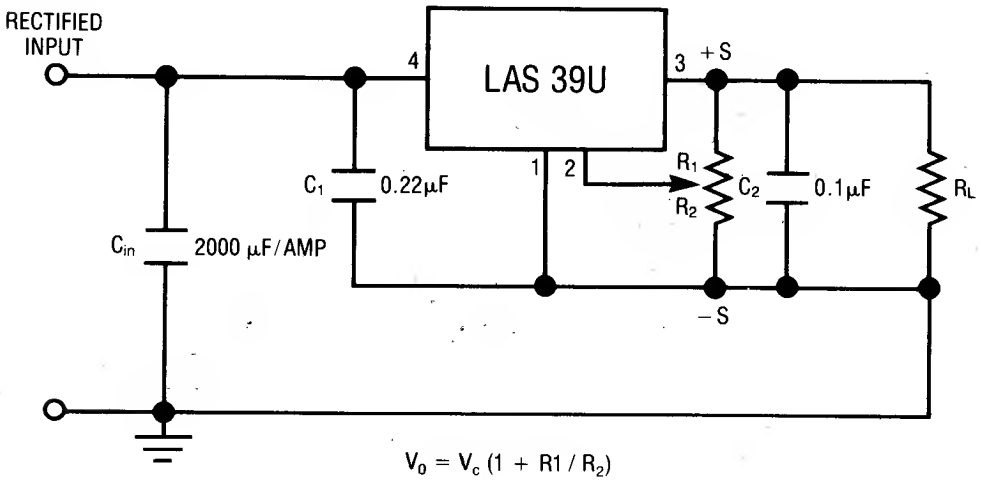


TYPICAL APPLICATIONS

FIXED VOLTAGE REGULATOR [1]



ADJUSTABLE VOLTAGE REGULATOR [1,2]



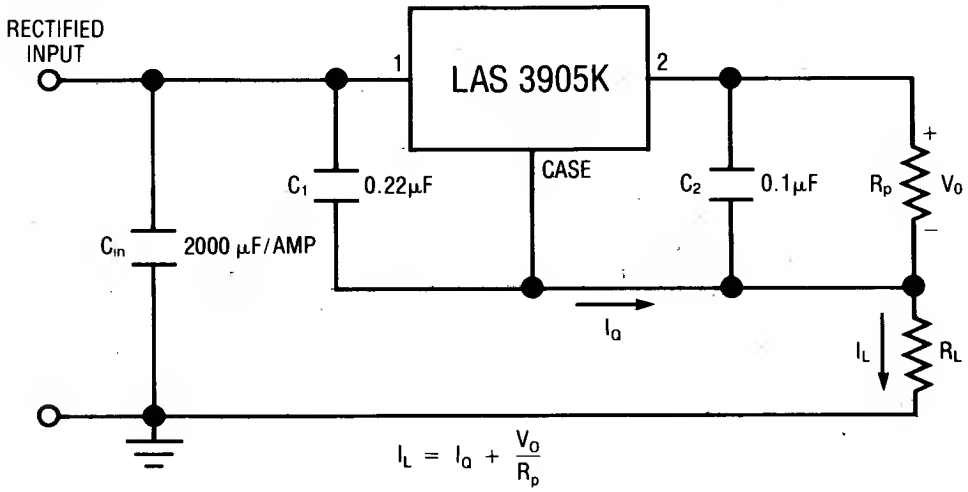
$$V_o = V_c (1 + R1 / R_2)$$

[1] C_1 and C_2 should be placed as close as possible to the regulator.

[2] $\frac{V_o}{R_1 + R_2} \geq 10$ mA

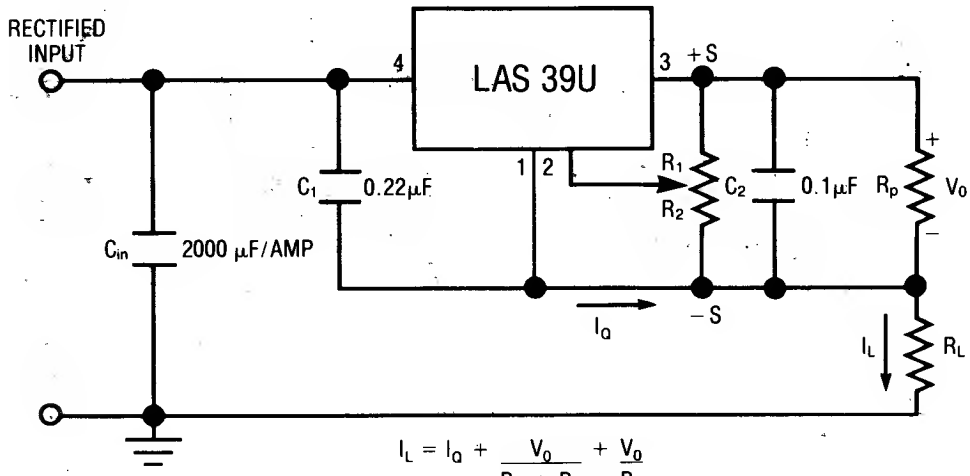
TYPICAL APPLICATIONS

FIXED CURRENT REGULATOR[1]



$$I_L = I_Q + \frac{V_O}{R_p}$$

ADJUSTABLE CURRENT REGULATOR[1,2]



$$I_L = I_Q + \frac{V_O}{R_1 + R_2} + \frac{V_O}{R_p}$$

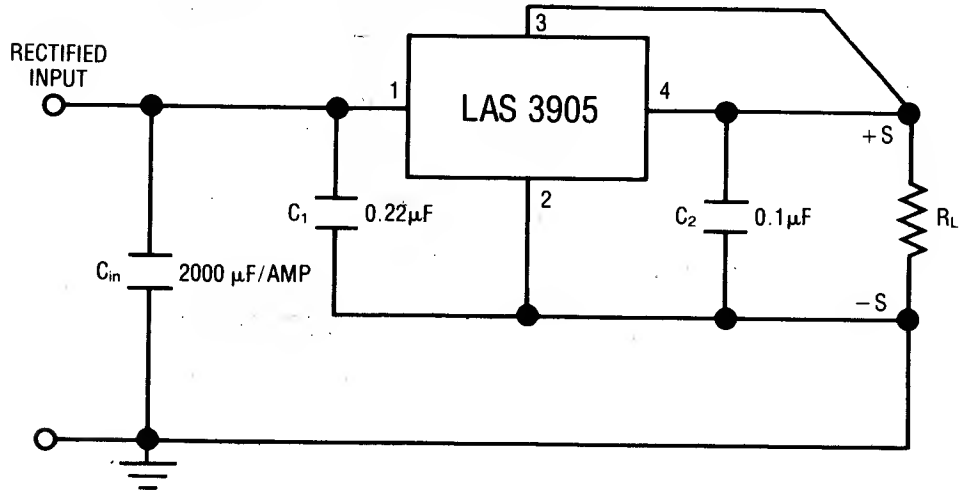
$$V_O = V_c (1 + R_1 / R_2)$$

[1] C_1 and C_2 should be placed as close as possible to the regulator.

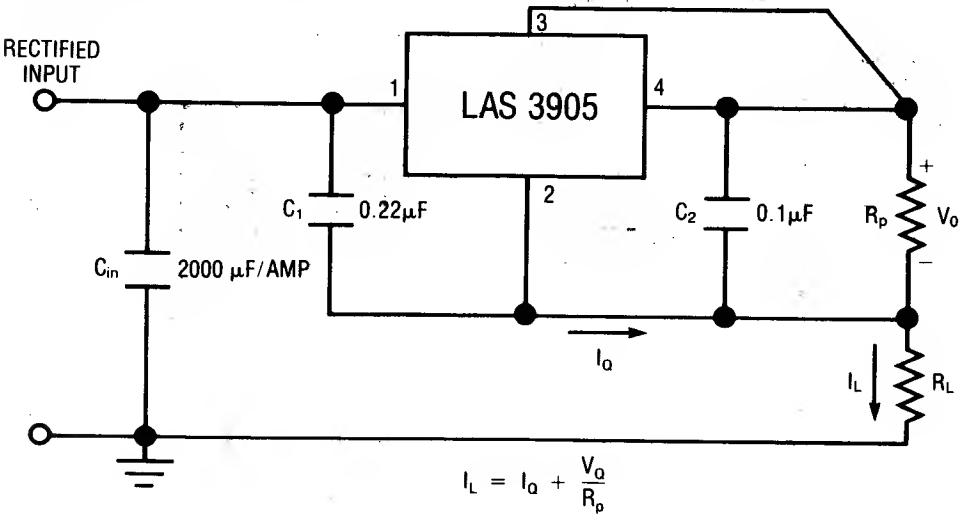
[2] $\frac{V_O}{R_1 + R_2} \geq 10$ mA

TYPICAL APPLICATIONS

FIXED VOLTAGE REGULATOR WITH REMOTE SENSE[1]



FIXED CURRENT REGULATOR[1]

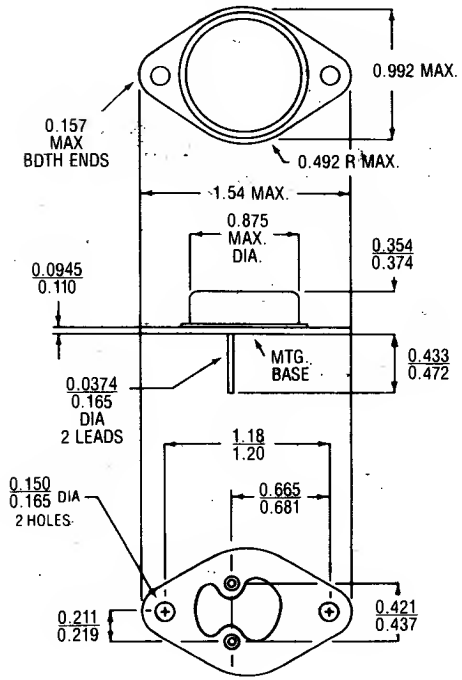


$$I_L = I_Q + \frac{V_Q}{R_p}$$

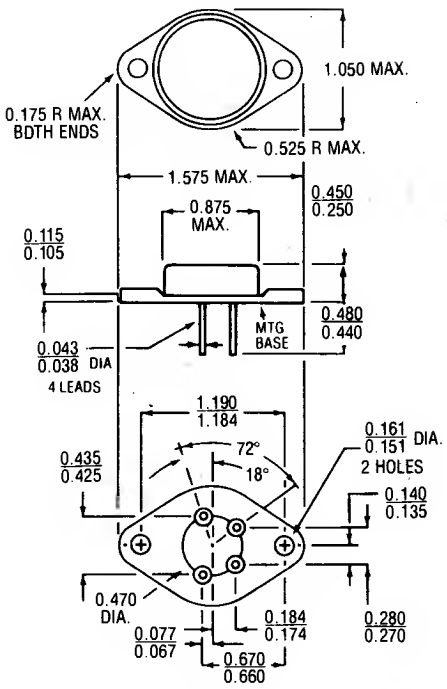
[1] C_1 and C_2 should be placed as close as possible to the regulator.

DEVICE OUTLINE

TO-3 (COPPER/STEEL)



TO-3 (COPPER)



4

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INTEGRATED CIRCUITS
UNITRODE

LAS 6350 SERIES

5 AMP SWITCHING REGULATORS

FEATURES

- DC to 100 kHz operation
- Adjustable output voltage
- Cycle-by-cycle current limit
- Internal thermal shutdown
- Inhibit/enable control pin

DESCRIPTION

The LAS 6350 Series are monolithic integrated circuits designed for fixed frequency, pulse width modulated, switching converter applications such as step-down, step-up, flyback, forward, Cük and voltage inverting DC-to-DC converters and motor controls. The LAS 6350 Series includes a temperature compensated voltage reference, sawtooth oscillator with over-current frequency shift, linear trailing edge pulse width modulator with double pulse suppression logic, transconductance error amplifier, and a 5 amp Darlington output transistor with internal current limit protection.

The LAS6350 & 6350P1 can be used in step-down or step-up applications. The LAS6351 & 6351P1 are for step-down applications where current limit adjustment is necessary. The LAS 6350 Series is available in TO-3 steel packages for true hermetic seal and board insertable plastic SIP packages.

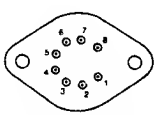
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
Control Circuit Voltage	V_{CC}	35	Volts
Output Collector Voltage	C_O	35	Volts
Power Dissipation	P_D	Internally Limited	Watts
Thermal Resistance Junction to Case LAS 6350&6351 LAS 6350P1&6351P1	θ_{JC}	 2.1 1.1	°C/W
Operating Junction and Storage Temperature Range	T_J T_{STG}	-25 to 125	°C
Lead Temperature (Soldering) 60 sec for TO-3 10 sec for SIP	T_{LEAD}	 300 260	°C

DEVICE SELECTION GUIDE

DEVICE	CURRENT LIMIT	PACKAGE
LAS 6350	Fixed	TO-3
LAS 6351	Adjustable	TO-3
LAS 6350P1	Fixed	Plastic SIP
LAS6351P1	Adjustable	Plastic SIP

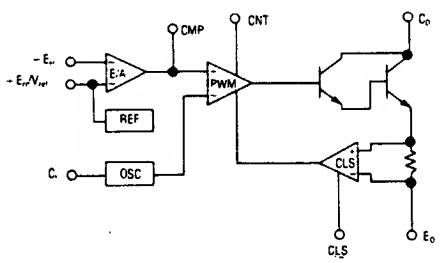
LAS6350



Bottom View

1 – C_O
2 – V_{CC}
3 – C_t
4 – CNT
5 – V_{REF}
6 – $E_{rr}(-)$
7 – CMP
8 – E_O
Case is Ground

BLOCK DIAGRAM



LAS6351

1 – C_O/V_{CC}
2 – C_t
3 – CNT
4 – V_{REF}
5 – E_{rr} (–)
6 – CMP
7 – CLS
8 – E_O
Case is Ground

LAS6350P1

1 – C_O
2 – V_{CC}
3 – C_t
4 – CNT
5 – GND
6 – V_{REF}
7 – E_{rr} (–)
8 – CMP
9 – E_O
Tab is Ground

LAS6351P1

1 – C_O/V_{CC}
2 – C_t
3 – CNT
4 – V_{REF}
5 – GND
6 – E_{rr} (–)
7 – CMP
8 – CLS
9 – E_O
Tab is Ground

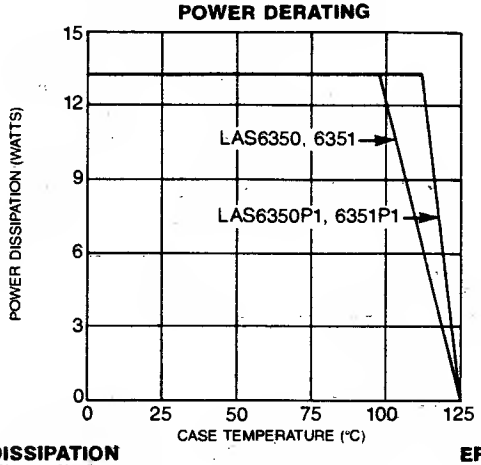
ELECTRICAL CHARACTERISTICS

Test conditions are as follows: V_{CC} = 24V, V_O = 5V, I_O = 5A, C_t = 0.0056μF, T_J = 25°C, unless otherwise specified.

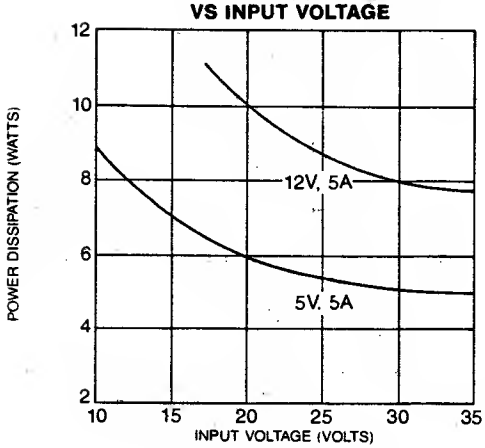
Parameter	Symbol	Test Conditions			Test Limits			Units
		V_{CC}	I_O	T_J	Minimum	Typical	Maximum	
REFERENCE SECTION								
Reference Voltage	V_{REF}				2.137	2.25	2.363	Volts
Line Regulation	$REG_{(LINE)}$	12V to 30V				0.015	0.04	%/V
Temperature Coefficient	T_C			0 to 125°C		0.01	0.02	%/°C
OSCILLATOR SECTION								
Initial Frequency Accuracy					−33	±10	+33	%
Line Regulation of Frequency	$REG_{(LINE)}$	12V to 30V				0.1	0.15	%/V
Frequency Temperature Coefficient	T_C			0 to 125°C		0.05		%/°C
Sawtooth Duty Cycle	d.c.					85		%
ERROR AMPLIFIER SECTION								
Input Offset Voltage						±5		mV
Transconductance						2.7		mA/V
Output Sink/Source Current						0.26		mA
Input Common Mode Range					1.5		3.0	Volts
Open Loop Voltage Gain					50	60		dB
OUTPUT SECTION								
Peak Switching Current Limit	I_{CL}				5.5	7.25	9.0	Amps
Output Saturation Voltage	V_O (sat)	$C_O = V_{CC}$ $C_O = V_{CC}$ E_O = GND E_O = GND	2A 5A 2A 5A			2.0 2.4 1.2 1.6	 2.6 1.8	Volts Volts Volts Volts
Efficiency	η				70	75		%
Current Rise Time	t_R	Inductive Load				50	100	nS
Current Fall Time	t_F	Inductive Load				700	900	nS
CONTROL PIN								
Output inhibit					0.64	0.75	1.06	Volts
Quiescent Current	I_Q	V_O = 0V				18	30	mA

OPERATIONAL DATA

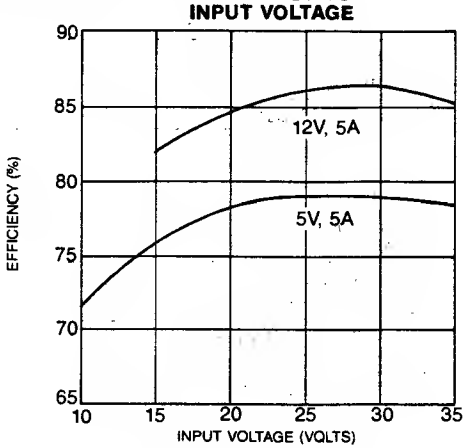
POWER DERATING



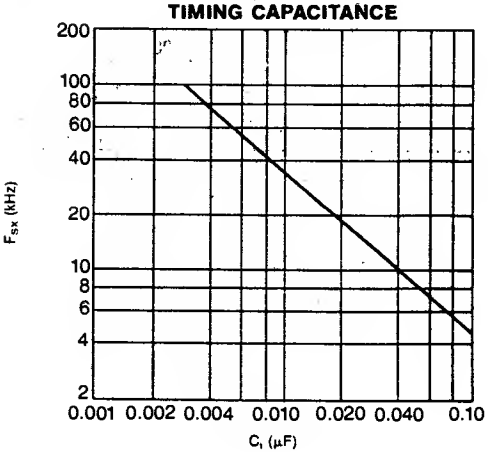
POWER DISSIPATION VS INPUT VOLTAGE



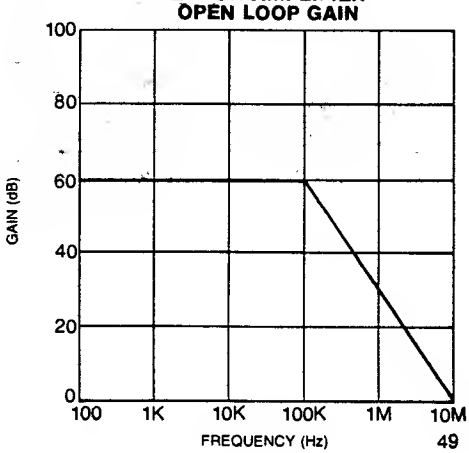
EFFICIENCY VS INPUT VOLTAGE



FREQUENCY VS TIMING CAPACITANCE



ERROR AMPLIFIER OPEN LOOP GAIN



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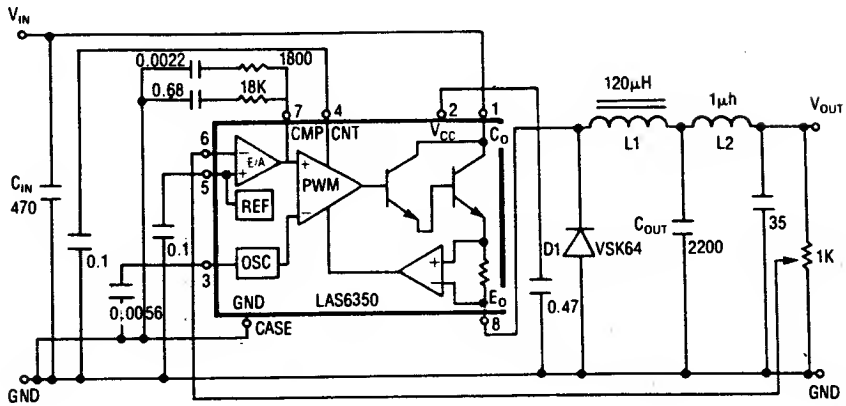
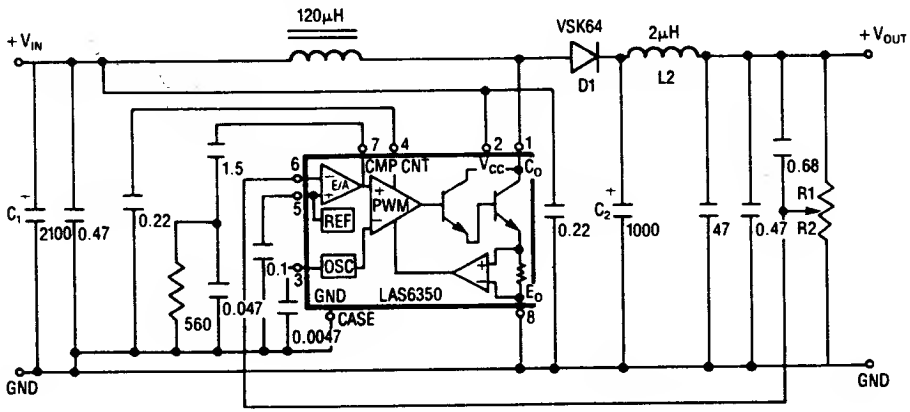
TYPICAL APPLICATIONS

DC-TO-DC STEP-DOWN CONVERTER



V_{IN} = 24V
V_{OUT} = 5V @ 5A

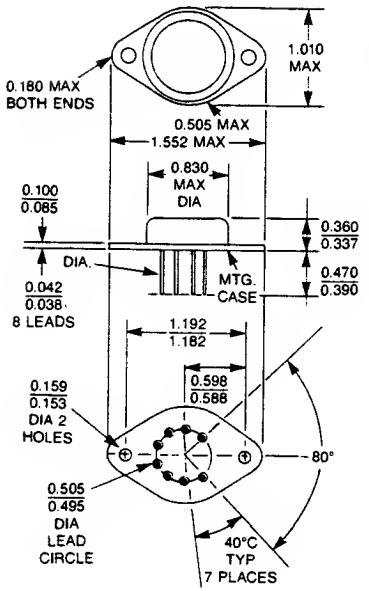
DC-TO-DC STEP-UP CONVERTER



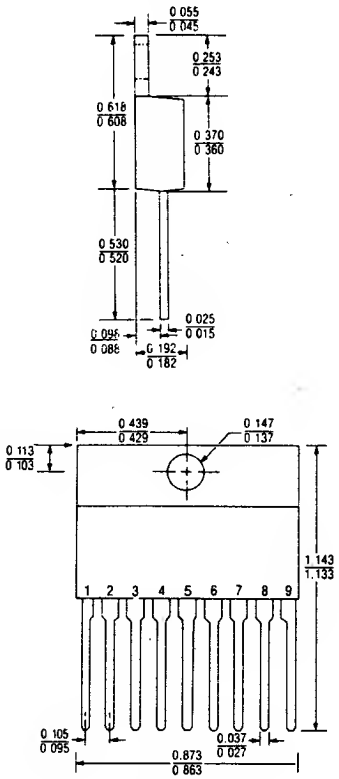
V_{IN} = 12V
V_{OUT} = 24V @ 1.5A

DEVICE OUTLINE

LAS6350, 6351



LAS6350P1, 6351P1



Front View

NOTE: All dimensions are in inches.

INTEGRATED CIRCUITS
UNITRODE

LAS 6380 SERIES

8 AMP SWITCHING REGULATORS

FEATURES

- DC to 100 kHz operation
- Adjustable output voltage
- Cycle-by-cycle current limit
- Internal thermal shutdown
- Inhibit/enable control pin

DESCRIPTION

The LAS 6380 Series are monolithic integrated circuits designed for fixed frequency, pulse width modulated, switching converter applications such as step-down, step-up, flyback, forward, Cŭk and voltage inverting DC-to-DC converters and motor controls. The LAS 6380 Series includes a temperature compensated voltage reference, sawtooth oscillator with over-current frequency shift, linear trailing edge pulse width modulator with double pulse suppression logic, transconductance error amplifier, and an 8 amp Darlington output transistor with internal current limit protection.

The LAS 6380 & 6380P1 can be used in step-down or step-up applications. The LAS 6381 & LAS 6381P1 are for step-down applications where current limit adjustment is necessary. The LAS 6380 Series is available in TO-3 steel packages for true hermetic seal and board insertable plastic SIP packages.

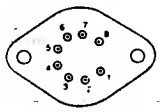
4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
Control Circuit Voltage	V_{CC}	35	Volts
Output Collector Voltage	C_O	35	Volts
Power Dissipation	P_D	Internally Limited	Watts
Thermal Resistance Junction to Case LAS 6380&6381 LAS 6380P1&6381P1	θ_{JC}	 1.5 0.8	°C/W
Operating Junction and Storage Temperature Range	T_J T_{STG}	– 25 to 125	°C
Lead Temperature (Soldering) 60 sec for TO-3 10 sec for SIP	T_{LEAD}	 300 260	°C

DEVICE SELECTION GUIDE

DEVICE	CURRENT LIMIT	PACKAGE
LAS 6380	Fixed	TO-3
LAS 6381	Adjustable	TO-3
LAS 6380P1	Fixed	Plastic SIP
LAS 6381P1	Adjustable	Plastic SIP

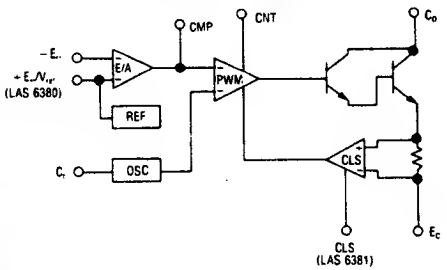


Bottom View

LAS6380

1 – C_O
2 – V_{CC}
3 – C_t
4 – CNT
5 – V_{REF}
6 – $E_{rr}(-)$
7 – CMP
8 – E_O
Case is Ground

BLOCK DIAGRAM



LAS6381

1 – C_O/V_{CC}
2 – C_t
3 – CNT
4 – V_{REF}
5 – $E_{rr}(-)$
6 – CMP
7 – CLS
8 – E_O
Case is Ground

LAS6380P1

1 – C_O
2 – V_{CC}
3 – C_t
4 – CNT
5 – GND
6 – V_{REF}
7 – $E_{rr}(-)$
8 – CMP
9 – E_O
Tab is Ground

LAS6381P1

1 – C_O/V_{CC}
2 – C_t
3 – CNT
4 – V_{REF}
5 – GND
6 – $E_{rr}(-)$
7 – CMP
8 – CLS
9 – E_O
Tab is Ground

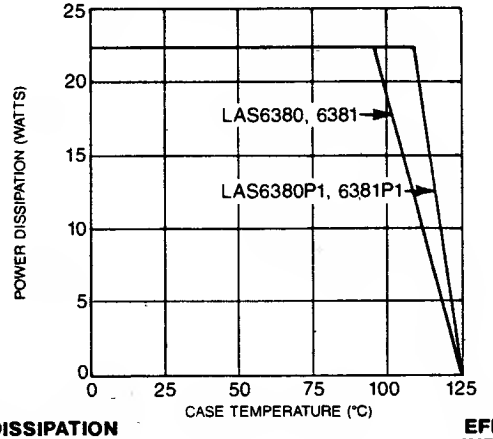
ELECTRICAL CHARACTERISTICS

Test conditions are as follows: V_{CC} = 24V, V_O = 5V, I_O = 8A, C_t = 0.0056μF, T_J = 25°C, unless otherwise specified.

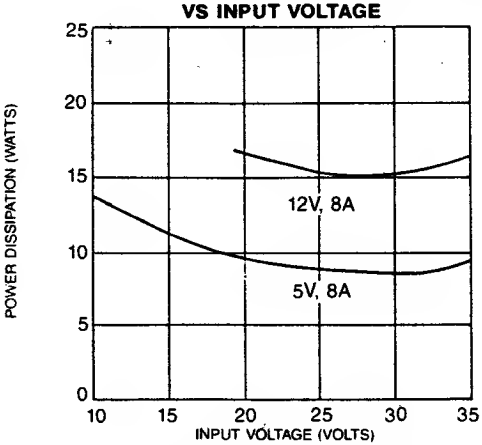
Parameter	Symbol	Test Conditions			Test Limits			Units
		V_{CC}	I_O	T_J	Minimum	Typical	Maximum	
REFERENCE SECTION								
Reference Voltage	V_{REF}				2.137	2.25	2.363	Volts
Line Regulation	$REG_{(LINE)}$	12V to 30V				0.015	0.04	%/V
Temperature Coefficient	T_C			0 to 125°C		0.01	0.02	%/°C
OSCILLATOR SECTION								
Initial Frequency Accuracy					−33	±10	+33	%
Line Regulation of Frequency	$REG_{(LINE)}$	12V to 30V				0.1	0.15	%/V
Frequency Temperature Coefficient	T_C			0 to 125°C		0.05		%/°C
Sawtooth Duty Cycle	d.c.					85		%
ERROR AMPLIFIER SECTION								
Input Offset Voltage						±5		mV
Transconductance						2.7		mA/V
Output Sink/Source Current						0.26		mA
Input Common Mode Range					1.5		3.0	Volts
Open Loop Voltage Gain					50	60		dB
OUTPUT SECTION								
Peak Switching Current Limit	I_{CL}				9	11	13	Amps
Output Saturation Voltage	V_O (sat)	C_O = V_{CC} C_O = V_{CC} E_O = GND E_O = GND	4A 8A 4A 8A			1.6 2.1 0.9 1.4	 2.5 1.8	Volts Volts Volts Volts
Efficiency	η				70	75		%
Current Rise Time	t_R	Inductive Load				50	100	nS
Current Fall Time	t_F	Inductive Load				700	900	nS
CONTROL PIN								
Output Inhibit					0.64	0.75	1.06	Volts
Quiescent Current	I_Q	V_O = 0V				18	30	mA

OPERATIONAL DATA

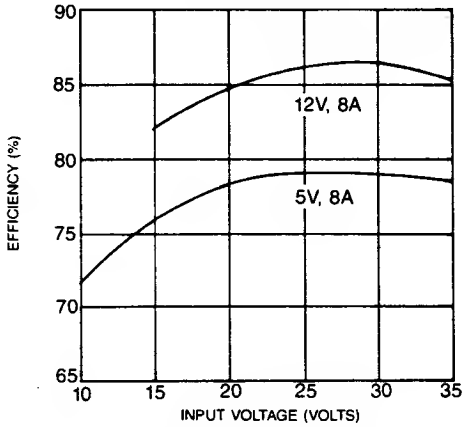
POWER DERATING



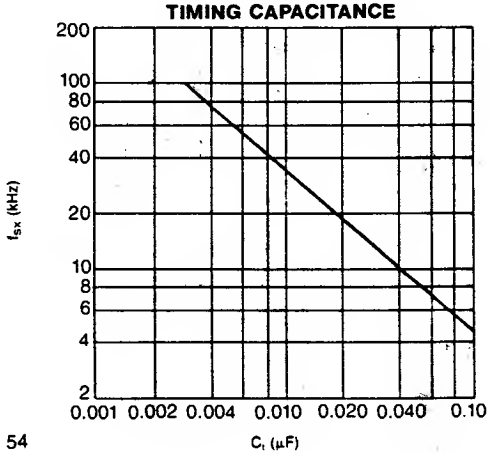
POWER DISSIPATION VS INPUT VOLTAGE



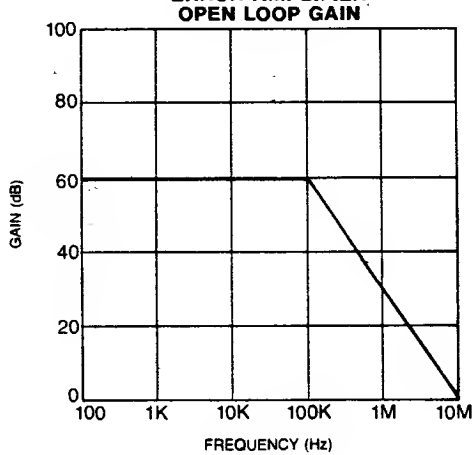
EFFICIENCY VS INPUT VOLTAGE



FREQUENCY VS TIMING CAPACITANCE

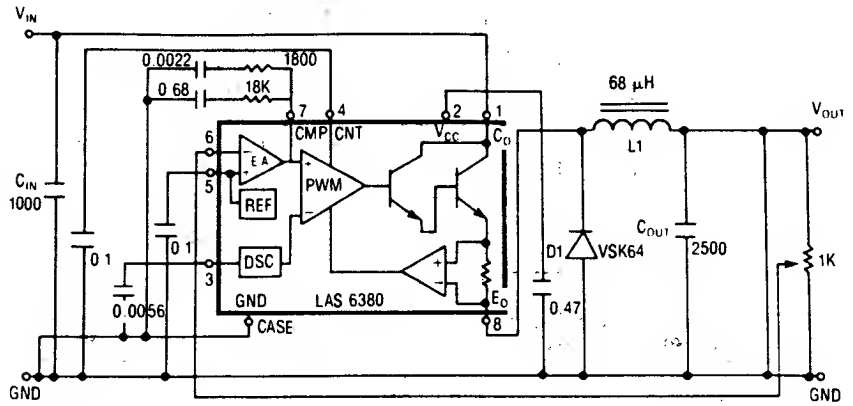


ERROR AMPLIFIER OPEN LOOP GAIN



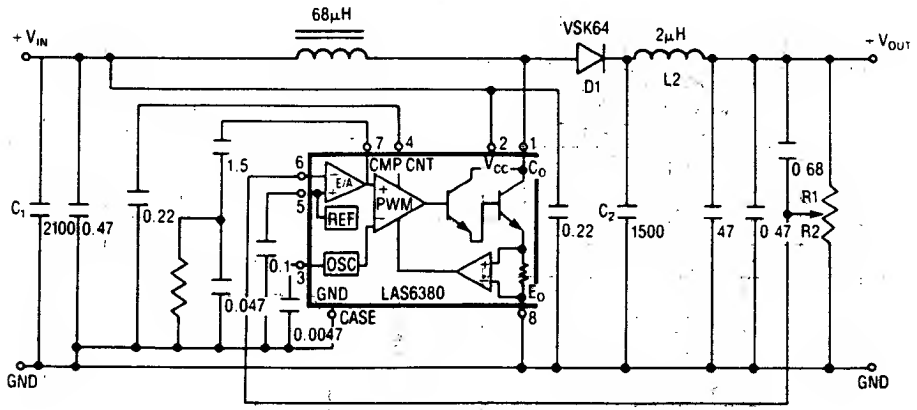
TYPICAL APPLICATIONS

DC-TO-DC STEP-DOWN CONVERTER



V_{IN} = 24V
V_{OUT} = 5V @ 8A

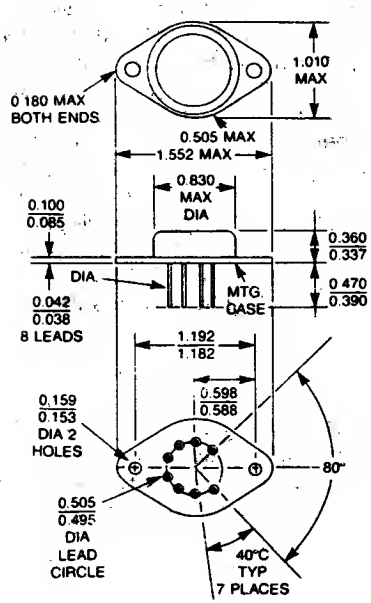
DC-TO-DC STEP-UP CONVERTER



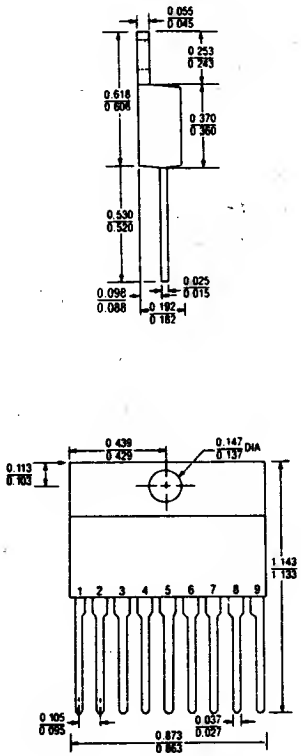
V_{IN} = 12V
V_{OUT} = 24V @ 2.5A

DEVICE OUTLINE

LAS6380, 6381



LAS6380P1, 6381P1



Front View

NOTE: All dimensions are in inches.

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Marrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

LLM 338

5 AMP POSITIVE ADJUSTABLE VOLTAGE REGULATOR

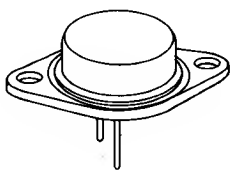
FEATURES

- Adjustable output down to 1.2V
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Standard 3-terminal, TO-3 package

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNITS
Input-Output Voltage Differential	V_{IN}-V_{OUT}		35	Volts
Power Dissipation	P_D		Internally Limited	
Thermal Resistance Junction to Case	θ_{JC}		1.0	°C/Watt
Operating Junction Temperature Range	T_J	0	125	°C
Storage Temperature Range	T_{STG}	−65	150	°C
Lead Temperature (Soldering, 60 Seconds Time Limit)	T_{LEAD}		300	°C

TO-3 (K)

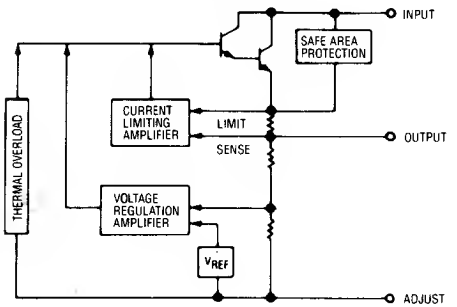


DESCRIPTION

The LLM 338 voltage regulator is a monolithic integrated circuit designed for use in applications requiring a well regulated positive output voltage. Outstanding features include full power usage up to 5.0 amperes of load current, internal current limiting, thermal shutdown, and safe area protection on the chip, providing protection of the series pass Darlington, under most operating conditions. Hermetically sealed copper/steel TO-3 packages are utilized for high reliability and low thermal resistance.

The LLM 338, a three terminal adjustable regulator, is available with an output range from +1.2 to +32 Volts. The output voltage is easily set by two external resistors. Since the regulator is "floating", higher output voltages can be regulated as long as the maximum input-output voltage differential is not exceeded.

BLOCK DIAGRAM

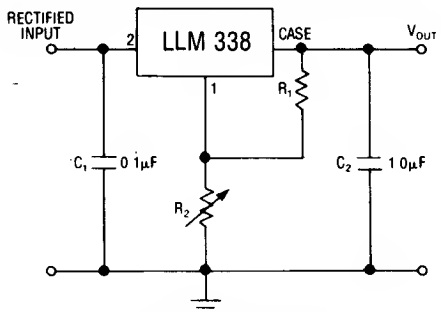


ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions[1]			Test Limits			
	V_{IN}-V_{OUT}	I_O	T_J	Min	Typ	Max	Units
Line Regulation[2]	3V to 35V	2.5A	25°C 0°C to 125°C		0.005 0.02	0.03 0.06	%/V %/V
Load Regulation[2] $V_O \leq 5V$ $V_O \geq 5V$ $V_O \leq 5V$ $V_O \geq 5V$		10mA to 5A	25°C 25°C 0°C to 125°C 0°C to 125°C		5 0.1 20 0.3	25 0.5 50 1.0	mV % mV %
Thermal Regulation[3]	5V	2.5A	25°C		0.002	0.02	%/W
Adjust Pin Current	5V	2.5A	0°C to 125°C		45	100	μA
Adjust Pin Current Change	3V to 35V	10mA to 5A	0°C to 125°C		0.2	5	μA
Reference Voltage	3V to 35V	10mA to 5A	0°C to 125°C	1.19	1.24	1.29	V
Temperature Stability	5V	2.5A	0°C to 125°C		1		%
Minimum Load Current	35V		0°C to 125°C		3.5	10.0	mA
Current Limit 0.5mS peak	≤10V ≤10V 30V		0°C to 125°C	5 7	8 12 1		A.
RMS Output Noise[4]	5V	2.5A	25°C		0.003		%/V_O
Ripple Rejection Ratio[5] C_{ADJ} = 10μF	V_O = 10V	2.5A	0°C to 125°C	60	60 75		dB

(1) Although power dissipation is internally limited, these specifications are applicable for power dissipations of 50 Watts.
(2) Low duty cycle pulse testing with Kelvin connections required. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(3) 20mS pulse
(4) BW = 10Hz to 10kHz
(5) 120Hz input ripple

TYPICAL APPLICATION
ADJUSTABLE VOLTAGE REGULATOR[1,2]

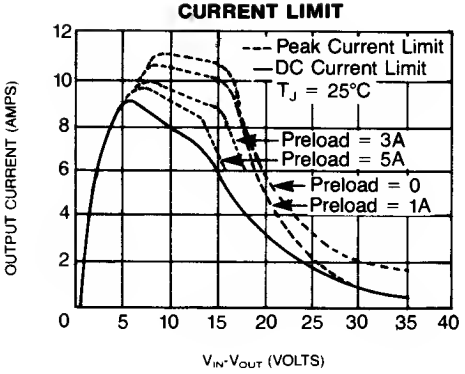


$V_{OUT} = 1.25V\ (1 + R_2/R_1)$

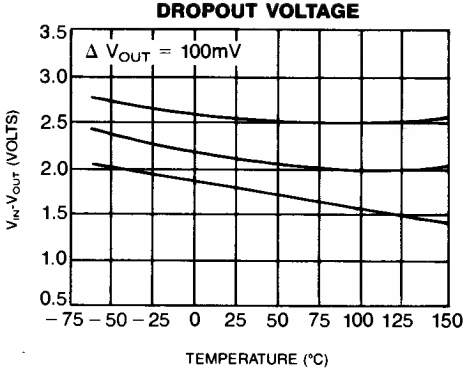
[1] C_1 needed if device is far from filter capacitors.
[2] C_2 optional - improves transient response.

OPERATIONAL DATA

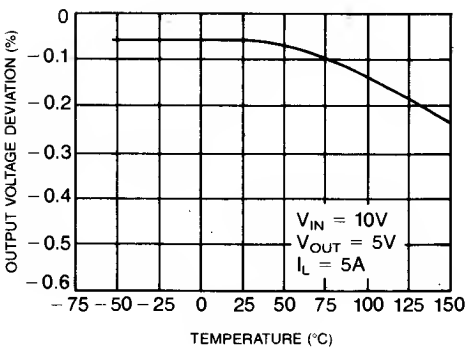
CURRENT LIMIT



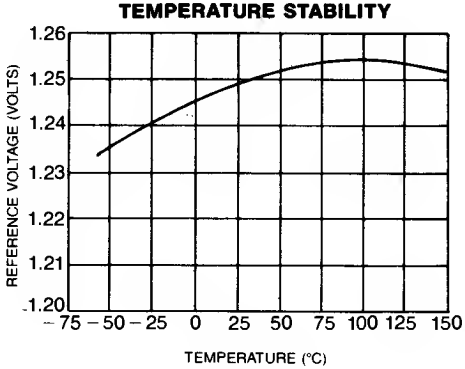
DROPOUT VOLTAGE



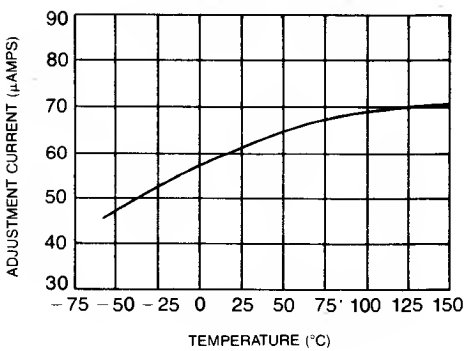
LOAD REGULATION



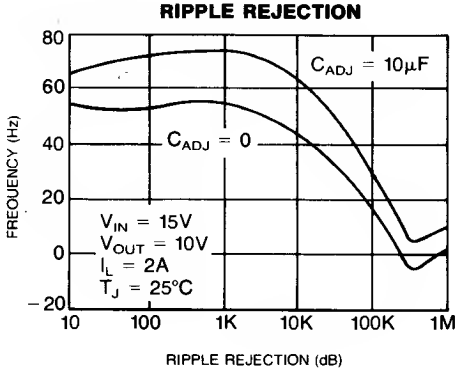
TEMPERATURE STABILITY



ADJUSTMENT CURRENT

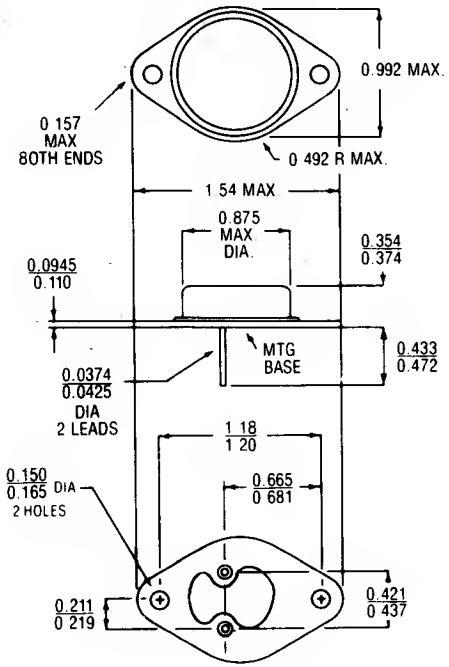


RIPPLE REJECTION

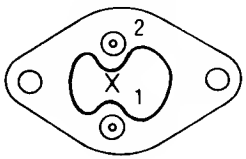


DEVICE OUTLINE

TO-3 (COPPER/STEEL)



Bottom View



1 – Adjust
2 – Input
Case is Output

NOTE: Case temperature measured at point X.
All dimensions are in inches.

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS
UNITRODE

High Current Switching Regulator

FEATURES

- 4A Output Current
- 5.1V to 40V Output Voltage Range
- 0 to 100% Duty Cycle Range
- Precise (±2%) On-Chip Reference
- Switching Frequency up to 200KHz
- Very High Efficiency (Up to 90%)
- Very Few External Components
- Soft Start
- Reset Output
- Control Circuit for Crowbar SCR
- Input for Remote Inhibit and Synchronous PWM
- Thermal Shutdown

DESCRIPTION

The L296 is a stepdown power switching regulator delivering 4A at voltages from 5.1V to 40V. The device features programmable current limiting, remote inhibit, soft start, thermal protection, reset output for microprocessors, and a PWM comparator input for synchronization in multichip configurations. The L296 is offered in a 15-lead Multiwatt® plastic power package and requires very few external components. Efficient operation at switching frequencies up to 200KHz allows reduction, in size and cost, of external filter components. A voltage sense input and SCR drive output are provided for optical crowbar over-voltage protection with an external SCR.

ABSOLUTE MAXIMUM RATINGS

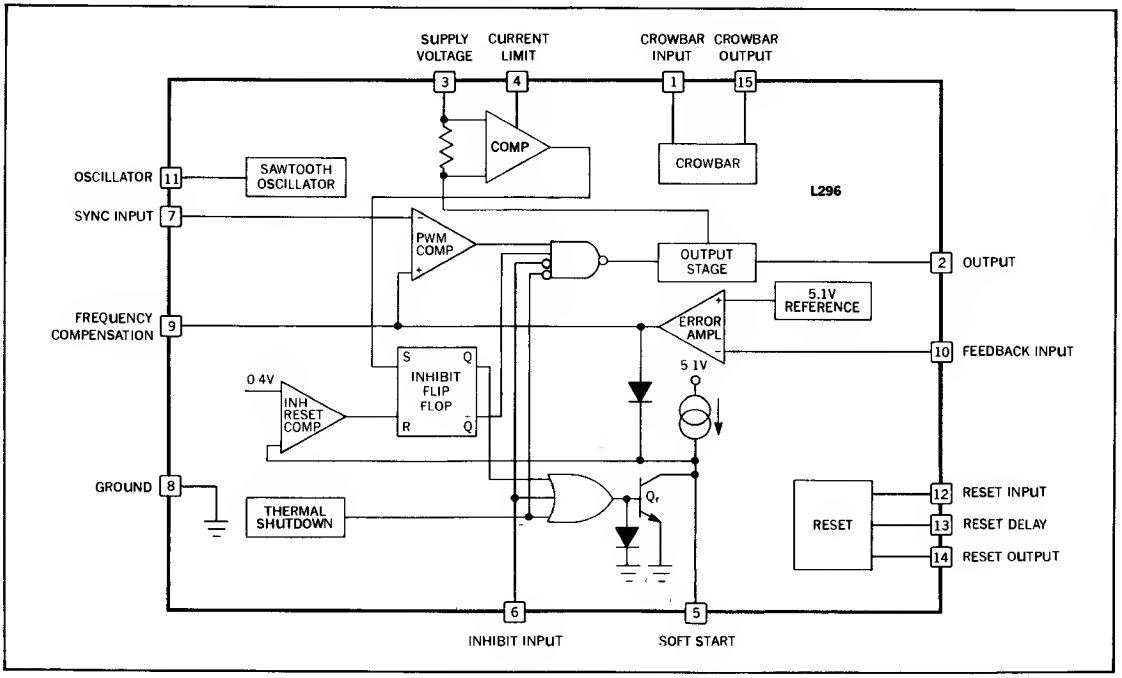
Supply Voltage, V_3 ..... 50V
Input to Output Voltage Difference, $V_3 - V_2$ 50V
Output DC Voltage, V_2 ..... -1V
Output Peak Voltage at t = 0.1μsec, f = 200KHz ..... -7V
Voltage at Pins 1 and 12, V_1, V_{12} 10V
Voltage at Pins 6 and 15, V_6, V_{15} 15V
Voltage at Pins 4, 5, 7 and 9, V_4, V_5, V_7, V_9, ... 5.5V
Voltage at Pins 10 and 6, V_{10}, V_6 ..... 7V
Voltage at Pin 14 ($I_{14} \leq 1mA$), V_{14} ..... V_3
Pin 9 Sink Current, I_9 ..... 1mA
Pin 11 Source Current, I_{11} ..... -20mA
Pin 14 Sink Current ($V_{14} < 5V$), I_{14} 50mA
Power Dissipation at $T_{case} \leq 90°C$, P_{tot} 20W
Junction and Storage Temperature, T_j, T_{stg} .. -40°C to +150°C

THERMAL DATA

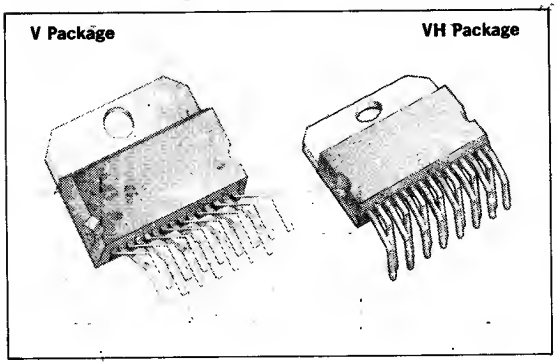
Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max.
Thermal Resistance Junction-Ambient, θ_{JA} ..... 35°C/W max.

Note: Currents into the device (sink) are positive value. Currents out of the device (source) are negative value.

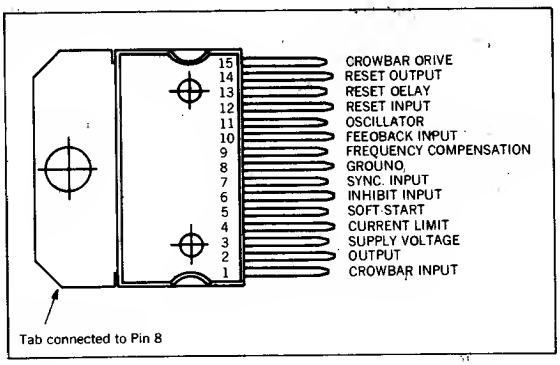
BLOCK DIAGRAM



LEAD FORM OPTIONS



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_3 = 35V, unless otherwise specified) $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dynamic Characteristics (Pin 6 to GND unless otherwise specified)						
Output Voltage Range	V_o	V_3 = 46V, I_o = −1A	V_{REF}		40	V
Supply Voltage Range	V_3	$V_o = V_{REF}$ to 36V, I_o = −4A	9		46	V
Line Regulation	ΔV_o	V_3 = 10V to 40V, $V_o = V_{REF}$, I_o = −2A		15	50	mV
Load Regulation	ΔV_o	$V_o = V_{REF}$, I_o = −2A to −4A		10	30	mV
		$V_o = V_{REF}$, I_o = −0.5A to −4A		15	45	mV
Internal Reference Voltage (Pin 10)	V_{REF}	V_3 = 9V to 46V, I_o = −2A	5	5.1	5.2	V
Average Temperature Coefficient of Reference Voltage*	$\frac{\Delta V_{REF}}{\Delta T}$	T_j = 0°C to 125°C, I_o = −2A		0.4		mV/°C
Dropout Voltage (Between Pin 2 and Pin 3)	V_d	I_o = −4A		2	3.2	V
		I_o = −2A		1.3	2.1	V
Maximum Operating Load Current	I_{om}	V_3 = 9V to 46V, $V_o = V_{REF}$ to 36V	−4			A
Current Limiting Threshold (Pin 2)	I_{2L}	V_3 = 9V to 46V, $V_o = V_{REF}$ to 40V, Pin 4 Open			−8	A
		V_3 = 9V to 46V, $V_o = V_{REF}$ to 40V, R_{lim} = 33KΩ		−2.5		A
Input Average Current	I_{SH}	V_3 = 46V, Output Short-Circuited		60	100	mA
Efficiency	η	I_o = −3A, $V_o = V_{REF}$		75		%
		I_o = −3A, V_o = 12V		85		%
Supply Voltage Ripple Rejection	SVRR	$\Delta V_3 = 2V_{rms}$, f_{ripple} = 120Hz, $V_o = V_{REF}$, I_o = −2A	50	56		dB
Switching Frequency	f		85	100	115	KHz
Voltage Stability of Switching Frequency		V_3 = 9V to 46V		0.5		%
Temperature Stability of Switching Frequency*		T_j = 0°C to 125°C		1		%
Maximum Operating Switching Frequency	f_{max}	$V_o = V_{REF}$, I_o = −1A, R = 1.75KΩ, C = 2.2nF	200			KHz
Thermal Shutdown Junction Temperature*	T_{jsd}		135	150		°C

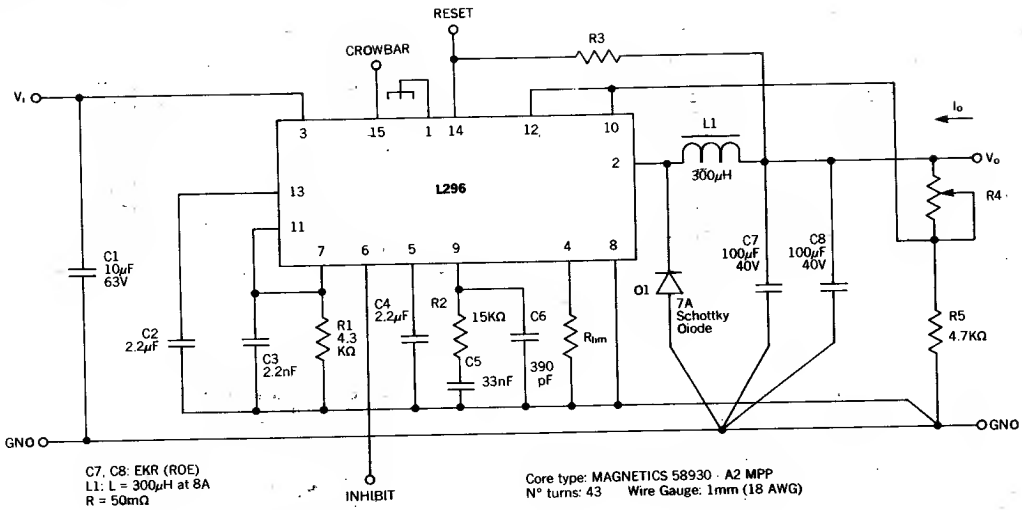
* Guaranteed by design; not 100% tested.

ELECTRICAL CHARACTERISTICS(Refer to the test circuit, T_j = 25°C, V_3 = 35V, unless otherwise specified) T_A=T_J

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC Characteristics							
Quiescent Drain Current	I_{3Q}	V_3 = 46V, V_7 = 0V, V_{10} = 0V, Pin 11: Open	V_6 = 0V		66	85	mA
			V_6 = 3V		30	40	
Output Leakage Current	I_{2L}		V_6 = 3V			−2	mA
Soft Start							
Source Current	I_5	V_6 = 0V, V_5 = 3V		−100	−130	−160	μA
Sink Current	I_5	V_6 = 3V, V_5 = 3V		50	70	120	μA
Inhibit							
Low Input Voltage	V_{6L}	V_3 = 9V to 46V, V_7 = 0V, V_{10} = 0V, Pins 2. 11: Open		−0.3		0.8	V
High Input Voltage	V_{6H}			2		5.5	V
Input Current with Low Input Voltage	I_{6L}		V_6 = 0.8V			−10	μA
Input Current with High Input Voltage	I_{6H}		V_6 = 2V			−3	μA
Error Amplifier							
High Level Output Voltage	V_{9H}	V_{10} = V_{REF} − 400mV, I_9 = +1		3.5			V
Low Level Output Voltage	V_{9L}	V_{10} = V_{REF} + 400mV, I_9 = −100μA				0.5	V
Sink Output Current	I_9	V_{10} = V_{REF} + 400mV		100	150		μA
Source Output Current	I_9	V_{10} = V_{REF} − 400mV		−100	−150		μA
Input Bias Current	I_{10}	V_{10} = 5.2V			2	10	μA
DC Open Loop Gain	G_V	V_9 = 1V to 3V		46	55		dB
Oscillator and PWM Comparator							
Input Bias Current of PWM Comparator	I_7	V_7 = 0.5V to 3.5V				−5	μA
Oscillator Source Current	I_{10}	V_{11} = 2V, Pin 2: Open		−5			mA
Reset							
Rising Threshold Voltage	V_{12R}	V_3 = 9V to 46V, I_{14} = 16mA, Pin 13: Open		V_{REF} −150mV	V_{REF} −100mV	V_{REF} −50mV	V
Falling Threshold Voltage	V_{12F}			4.75.	V_{REF} −150mV	V_{REF} −100mV	V
Delay Threshold Voltage	V_{13D}	V_{12} = 5.3V, I_{14} = 16mA		4.3	4.5	4.7	V
Delay Threshold Voltage Hysteresis	V_{13H}	V_{12} = 5.3V, I_{14} = 16mA			100		mV
Output Saturation Voltage	V_{14S}	I_{14} = 16mA, V_{12} = 4.7V, Pin 13: Open				0.4	V
Input Bias Current	I_{12}	V_{12} = 0V to V_{REF}, I_{14} = 16mA, Pin 13: Open			1	3	μA
Delay Source Current	I_{13}	V_{13} = 3V, I_{14} = 16mA, V_{12} = 5.3V		−70	−110	−140	μA
Delay Sink Current	I_{13}	V_{13} = 3V, I_{14} = 16mA, V_{12} = 4.7V		10			mA
Output Leakage Current	I_{14}	V_3 = 46V, V_{12} = 5.3V, Pin 13: Open				+100	μA
Crowbar							
Input Threshold Voltage	V_1	V_{15} = 2V		5.5	6	6.4	V
Output Saturation Voltage	V_{15}	V_3 = 9V to 46V, V_1 = 5.4V, I_{15} = 5mA			0.2	0.4	V
Input Bias Current	I_1	V_1 = 6V, V_{15} = 2V				10	μA
Output Source Current	I_{15}	V_3 = 9V to 46V, V_1 = 6.5V, V_{15} = 2V		−70	−100		mA

* Guaranteed by design; not 100% tested.

DYNAMIC TEST CIRCUIT



APPLICATION INFORMATION

Choosing the Inductor and Capacitor

The input and output capacitors of the L296 must have a low ESR and low inductance at high current ripple.

Saturation must not occur at current levels below 1.5 times the current limiter level.

$$L = \frac{(V_3 - V_o)\, V_o}{V_3\, f\, \Delta I_L}$$

$$C = \frac{(V_3 - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

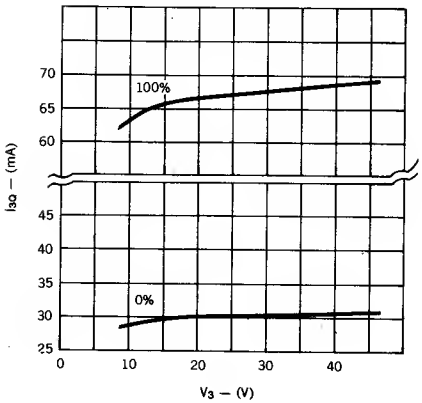
f = frequency

ΔI_L = Inductance current ripple

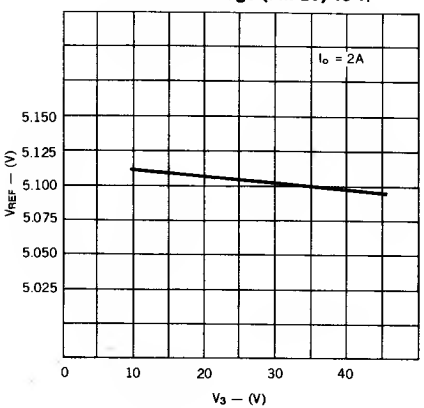
ΔV_O = Output ripple voltage

Resistor Values for Standard Output Voltages		
V_o	R_5	R_4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

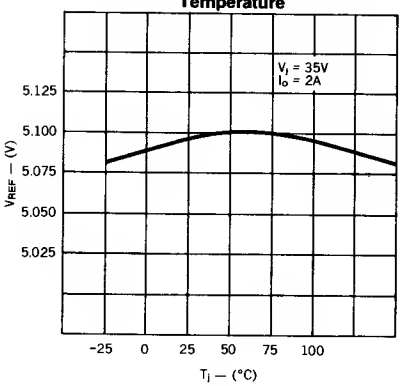
Quiescent Drain Current vs Supply Voltage (0% + 100% Duty Cycle)



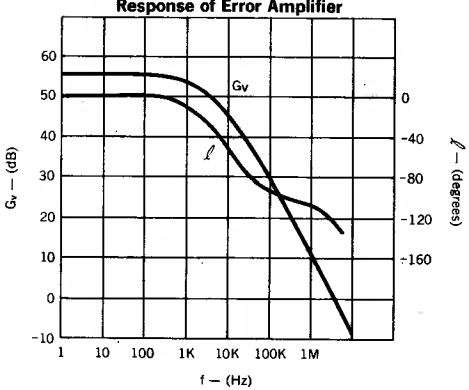
Reference Voltage (Pin 10) vs V_i



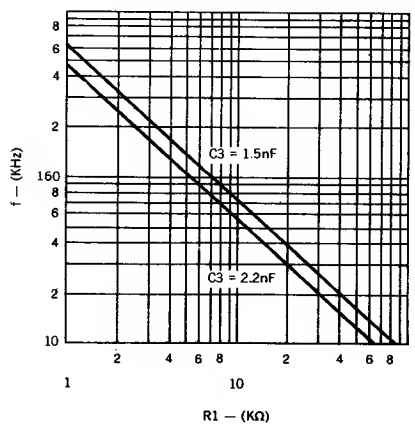
Reference Voltage (Pin 10) vs Junction Temperature



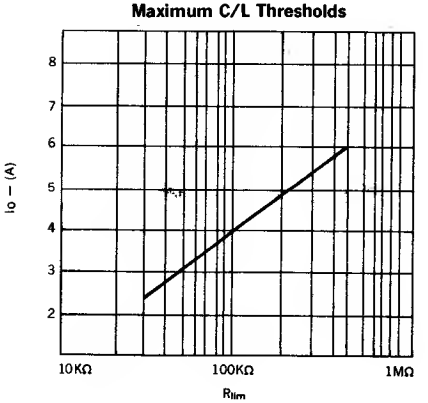
Open Loop Frequency and Phase Response of Error Amplifier



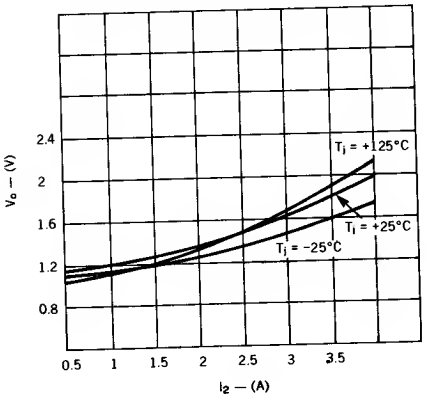
Switching Frequency vs R1



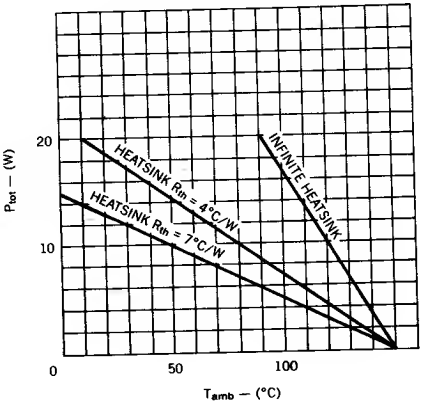
Maximum C/L Thresholds



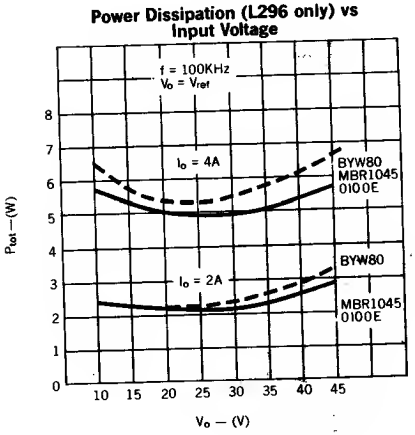
Dropout Voltage Between Pin 3 and Pin 2 vs Current at Pin 2



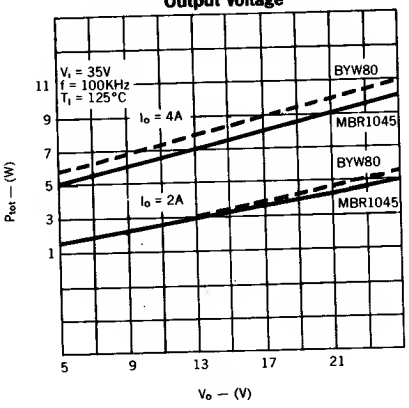
Power Dissipation Derating Curve



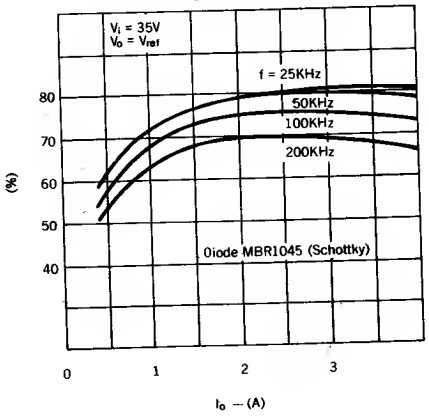
Power Dissipation (L296 only) vs Input Voltage



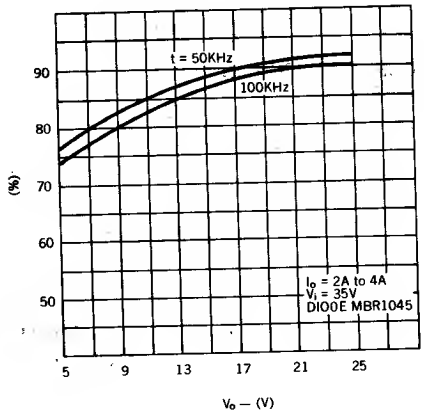
Power Dissipation (L296 only) vs Output Voltage



Efficiency vs Output Current



Efficiency vs Output Current



CIRCUIT OPERATION

Figure 1. Reset Output Waveforms

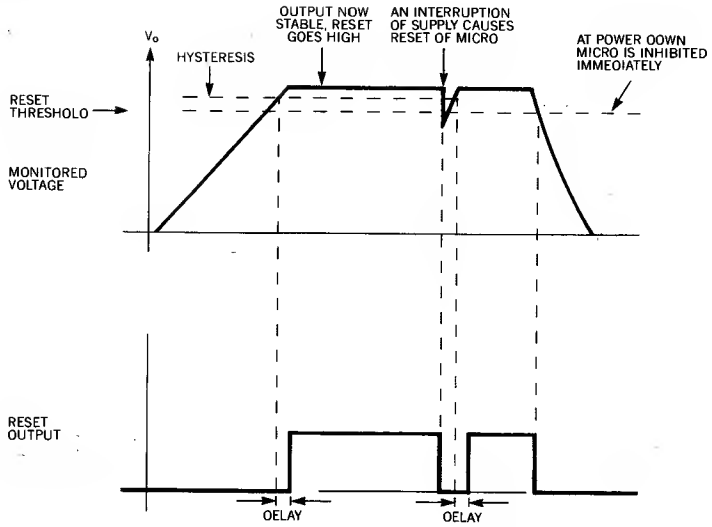


Figure 2. Soft Start Waveforms

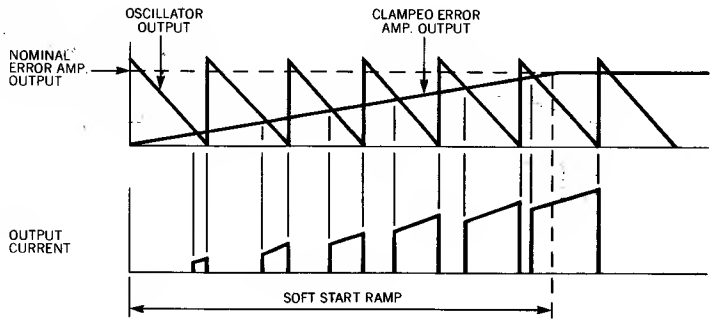
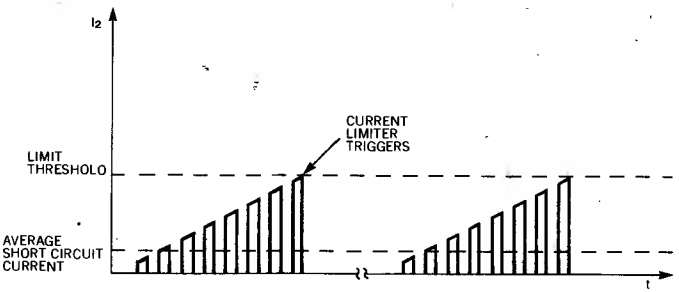


Figure 3. Current Limiter Waveforms



PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

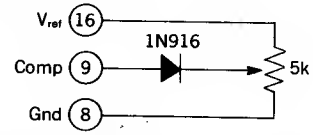
$$f \simeq \frac{1.18}{R_T C_T}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

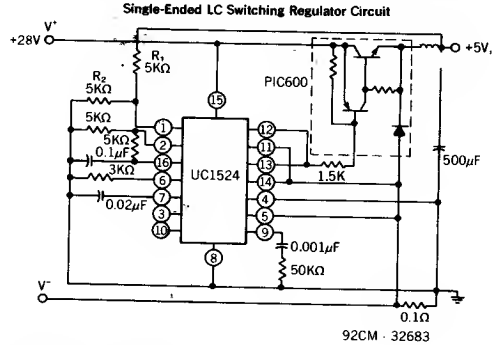


Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

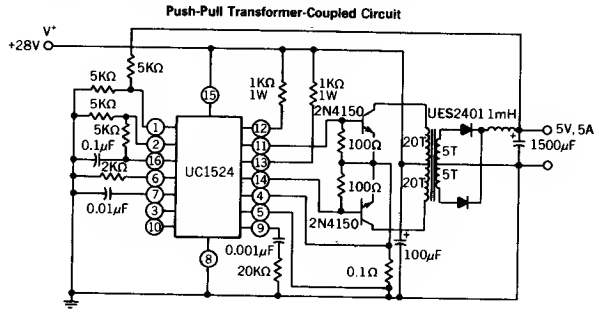
If two or more UC1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Single-Ended LC Switching Regulator Circuit

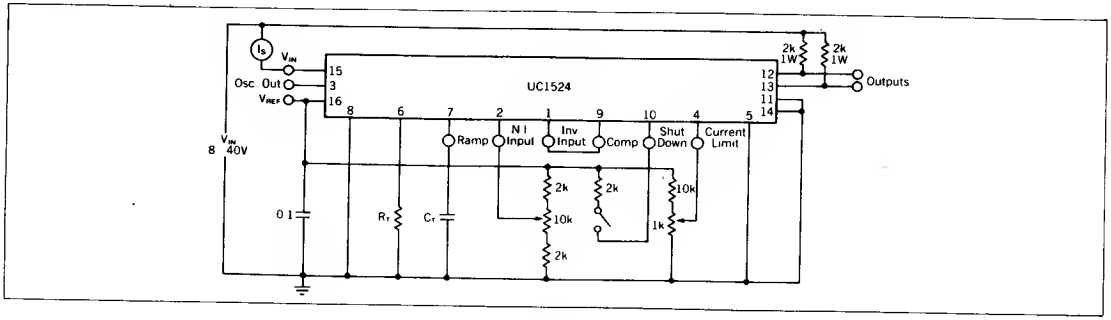


92CM-32683

Push-Pull Transformer-Coupled Circuit



OPEN LOOP TEST CIRCUIT



INTEGRATED CIRCUITS

UNITRODE

Advanced Regulating Pulse Width Modulators

UC1524A
UC2524A
UC3524A

FEATURES

- Fully interchangeable with standard UC1524 family
- Precision reference internally trimmed to ±1%
- High-Performance current limit function
- Under-voltage lockout with hysteretic turn-on
- Start-up supply current less than 4mA
- Output current to 200mA
- 60V output capability
- Wide common-mode input range for both error and current limit amplifiers
- PWM latch insures single pulse per period
- Double pulse suppression logic
- 200ns shutdown through PWM latch
- Guaranteed frequency accuracy
- Thermal shutdown protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from −55°C to +125°C. The UC2524A and UC3524A are available in either ceramic or plastic packages and are rated for operation from −25°C to +85°C and 0°C to 70°C, respectively.

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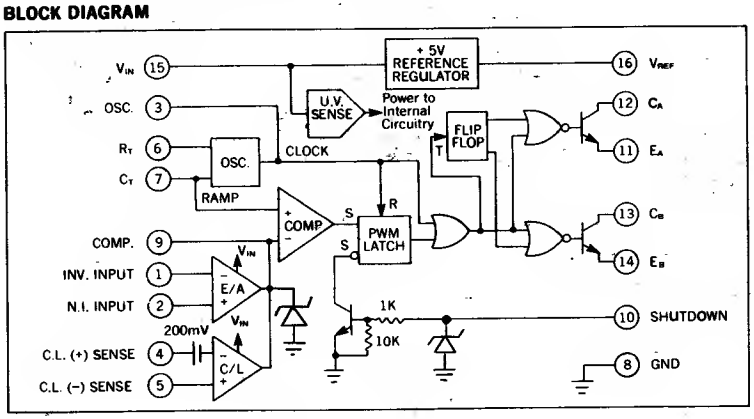
ABSOLUTE MAXIMUM RATINGS

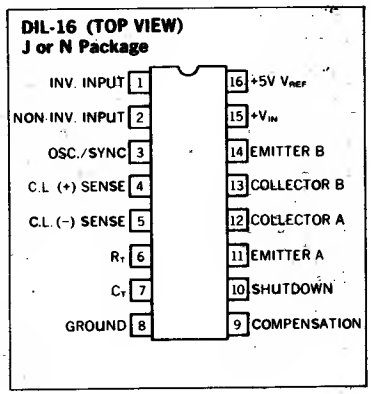
Supply Voltage (V_{IN})	40V
Collector Supply Voltage (V_C)	60V
Output Current (Each Output)	200mA
Maximum Forced Voltage (PIN 9, 10)	-3 to +5V
Maximum Forced Current (PIN 9, 10)	±10mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T_A = +25°C	1000mW
Derate above +50°C	10mW/°C
Power Dissipation at T_C = +25°C	2000mW
Derate for Case Temperature above +25°C	16mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524A, −25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_j = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Output Voltage	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10hz ≤ f ≤ 10kHz, T_j = 25°C		40			40		μVrms
Long Term Stability*	T_j = 125°C, 1000 Hrs.		20	50		20	50	mV
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_j = 25°C	41	43	45	39	43	47	kHz
Initial Accuracy	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1 mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470 pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	μs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_j = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			−1.0			−1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current			.05	1		0.5	1	μA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 2)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔVo = 1 to 4V, R_L ≥ 10 Meg Ω	72	80		64	80		dB
Gain-Bandwidth*	T_j = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*†	T_j = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 200Ω, C_T = 0.01 mfd)								
Maximum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%

* These parameters are guaranteed by design but not 100% tested in production.

† DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground.

The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

Note 1. Min limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1524A, −25°C to +85°C for the UC2524A, and 0°C to +70°C for the UC3524A; V_{IN} = V_C = 20V.) $T_A = T_j$

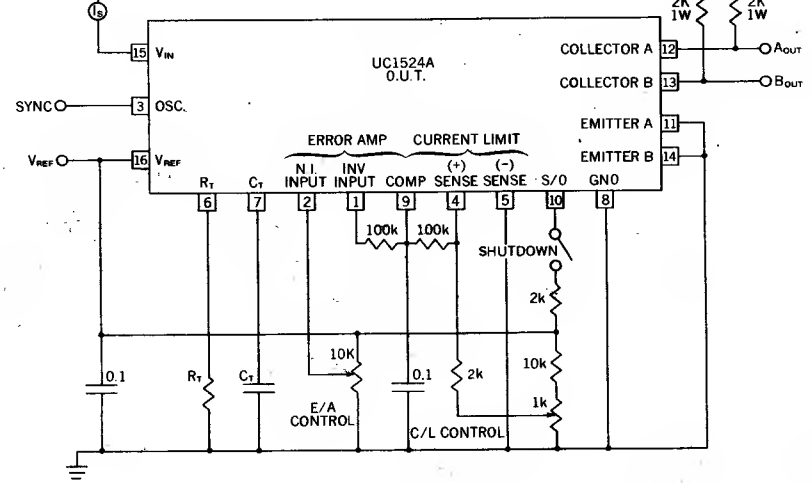
PARAMETER	TEST CONDITIONS	UC1524A UC2524A			UC3524A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_j = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
Input Offset Voltage	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			−1	−10		−1	−10	μA
Common Mode Rejection Ratio	$V_{(Pin\ 5)}$ = −0.3V to +5.5V	50	60		50	60		dB
Power Supply Rejection Ration	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10 Meg Ω	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100μA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	μA
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_j = 25°C, R = 2K Ω		120	400		120	400	ns
Fall Time*	T_j = 25°C, R = 2K Ω		25	200		25	200	ns
Comparator Delay*	T_j = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_j = 25°C, Pin 10 to Output		200			200		ns
Shutdown Threshold	T_j = 25°C, R_C = 2K Ω	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.		0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

* These parameters are guaranteed by design but not 100% tested in production.

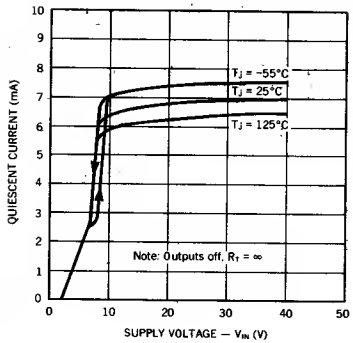
OPEN-LOOP TEST CIRCUIT

Note: The UC1524A should be able to be tested in any 1524 test circuit with two possible exceptions:
1. The higher gain-bandwidth of the current limit amplifier in the UC1524A may cause oscillations in an uncompensated 1524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs.

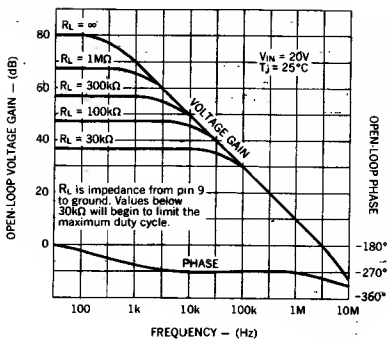
The circuit below will allow all UC1524A functions to be evaluated.



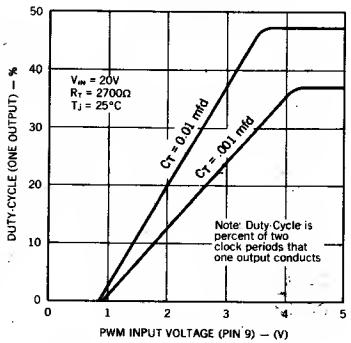
Supply Current vs Voltage



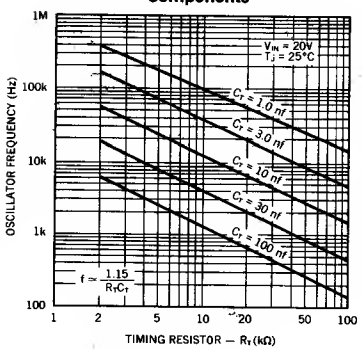
Error Amplifier Voltage Gain and Phase vs Frequency



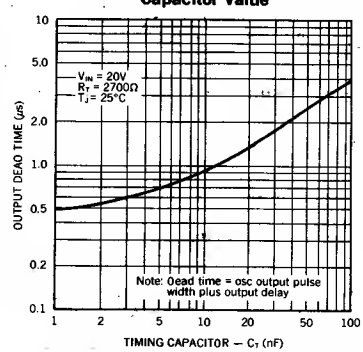
Pulse Width Modulator Transfer Function



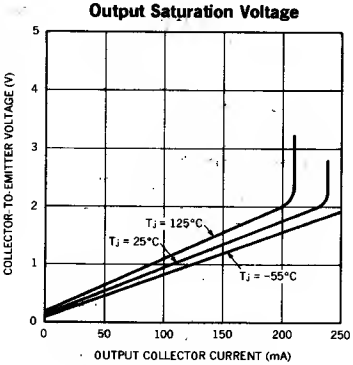
Oscillator Frequency vs Timing Components



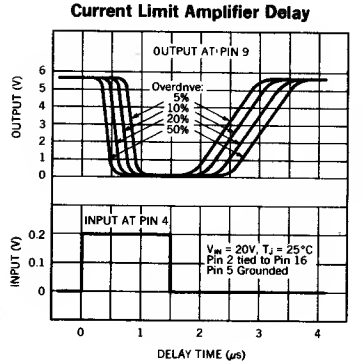
Output Dead Time vs Timing Capacitor Value



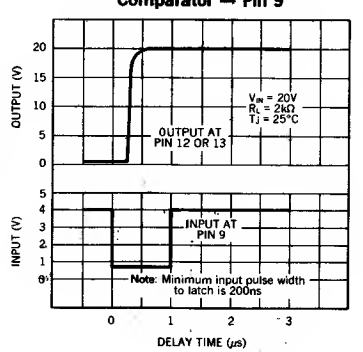
Output Saturation Voltage



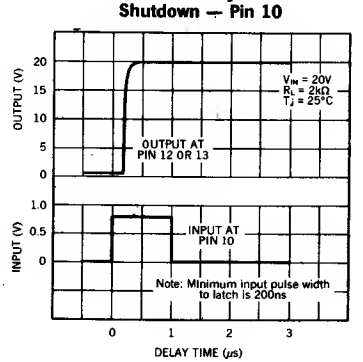
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator — Pin 9



Turn-Off Delay From Shutdown — Pin 10



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INTEGRATED CIRCUITS

UNITRODE

Regulating Pulse Width Modulators

UC1525A UC1527A
UC2525A UC2527A
UC3525A UC3527A

FEATURES

- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100Hz to 500kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Pulse-by-pulse shutdown
- Input undervoltage lockout with hysteresis
- Latching PWM to prevent multiple pulses
- Dual source/sink output drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

4

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, ($+V_{IN}$)	+40V
Collector Supply Voltage (V_C)	+40V
Logic Inputs	−0.3V to +5.5V
Analog Inputs	−0.3V to $+V_{IN}$
Output Current, Source or Sink	500mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T_A= +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T_C = +25°C (Note 3)	2000mW
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	−55°C to +150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

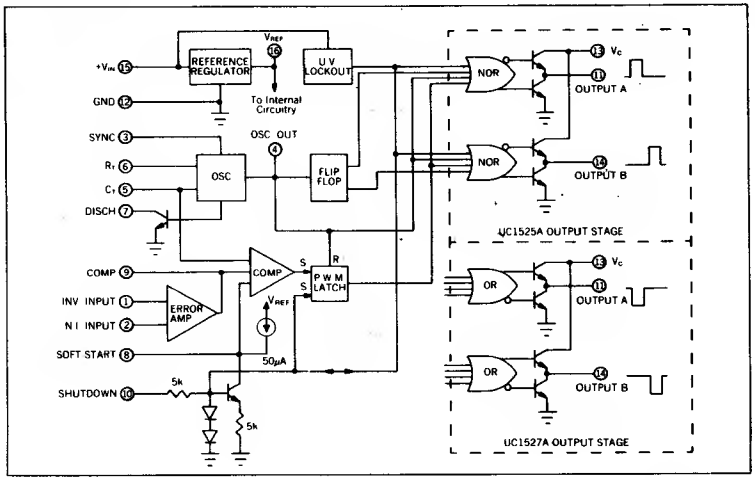
Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 16mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage ($+V_{IN}$)	+8V to +35V
Collector Supply Voltage (V_C)	+4.5V to +35V
Sink/Source Load Current (steady state)	0 to 100mA
Sink/Source Load Current (peak)	0 to 400mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	100Hz to 400kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	.001μF to 0.1μF
Dead Time Resistor Range	0 to 500Ω
Operating Ambient Temperature Range	
UC1525A, UC1527A	−55°C to +125°C
UC2525A, UC2527A	−25°C to +85°C
UC3525A, UC3527A	0°C to +70°C

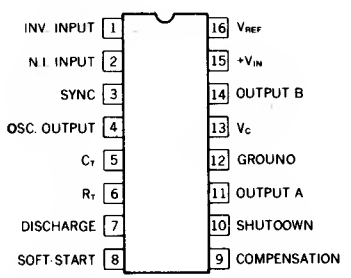
Notes: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (Top View)
J or N Package



ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	mV
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	V_{REF} = 0, T_j =25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T_j = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T_j = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_j = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 5)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	R_T = 200kΩ, C_T = 0.1μF			120			120	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_j = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R_L ≥ 10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_j = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T_j = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

6. Tested at f_{OSC} = 40KHz (R_T = 3.6kΩ, C_T = .01μF, R_D = 0Ω). Approximate oscillator frequency is defined by: $f = \frac{1}{C_T(0.7R_T + 3R_D)}$

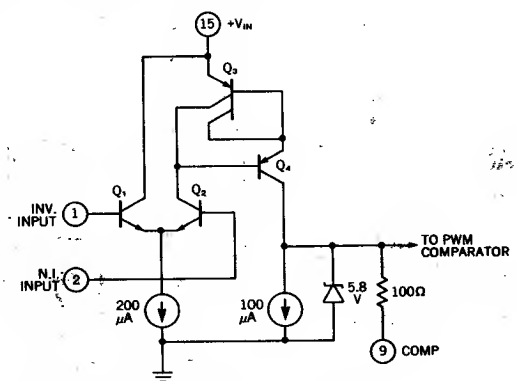
7. DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground.
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS (+V_{IN} = 20V, and over operating temperature, unless otherwise specified) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 6)	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	μA
Shutdown Section								
Soft Start Current	V_{SD} = 0V, V_{SS} = 0V	25	50	80	25	50	80	μA
Soft Start Low Level	V_{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V_{SS} = 5.1V, T_j = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V_{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V_{SD} = 2.5V, T_j = 25°C		0.2	0.5		0.2	0.5	μS
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Under-Voltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
V_C OFF Current (Note 7)	V_C = 35V			200			200	μA
Rise Time (Note 5)	C_L = 1nF, T_j = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nf, T_j =25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

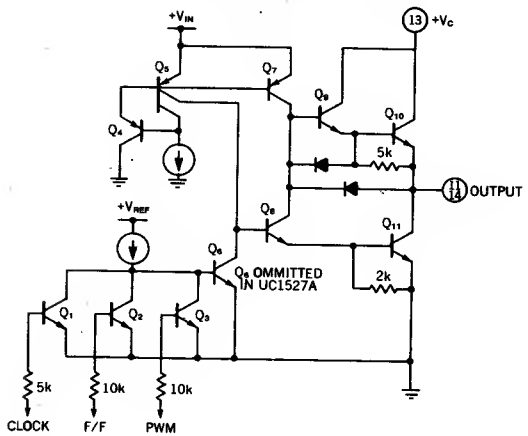
Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
6. Tested at f_{OSC} = 40KHz (R_T =3.6kΩ, C_T = 0.1μF, R_D = 0Ω).
7. Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

UC1525A Error Amplifier

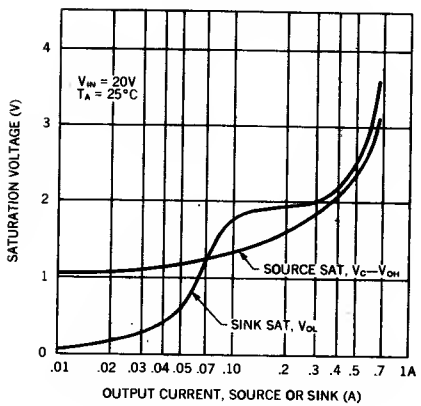


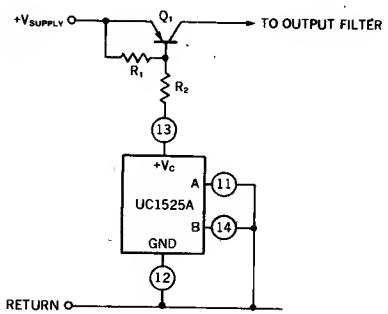
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A Output Circuit
(½ Circuit Shown)

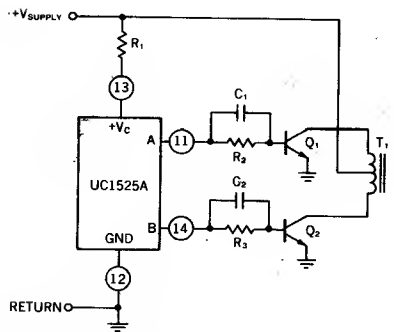


UC1525A Output Saturation Characteristics

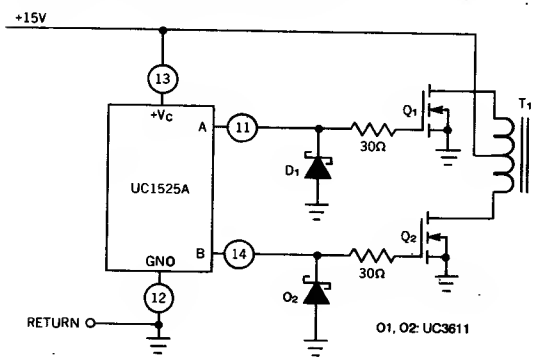




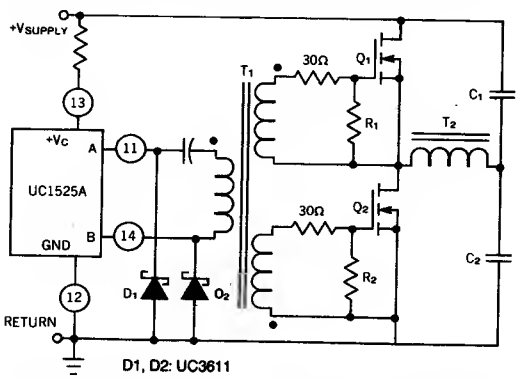
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1-R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

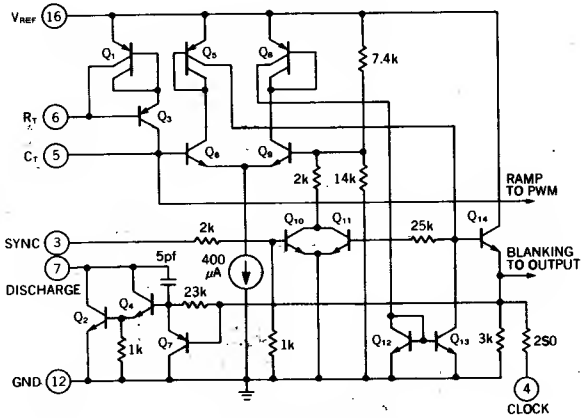
SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

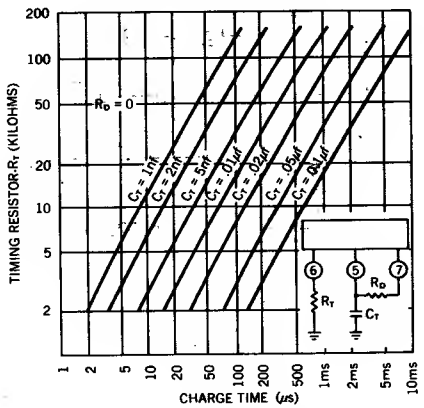
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

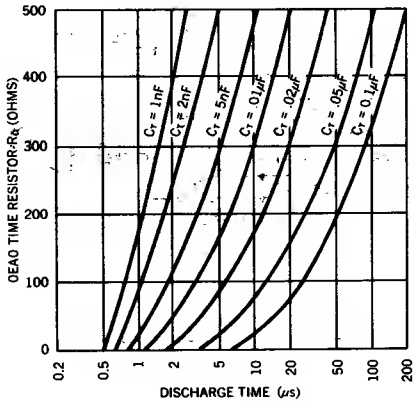
UC1525A Oscillator Schematic



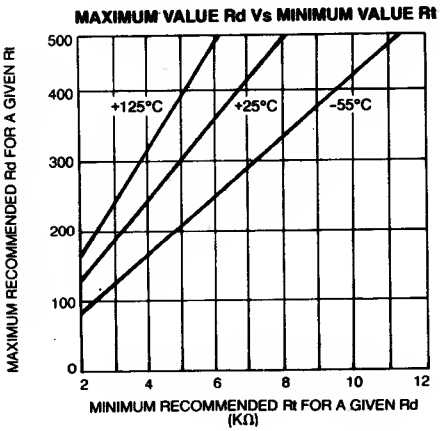
Oscillator Charge Time vs. R_T and C_T



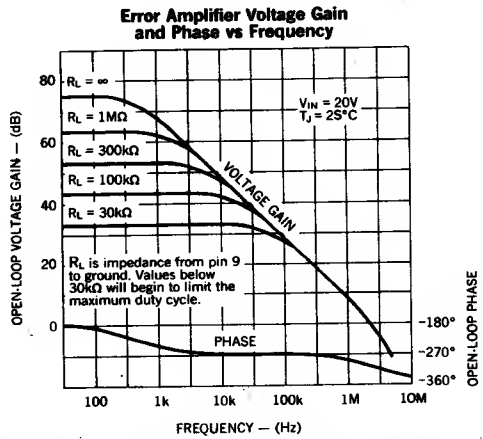
Oscillator Discharge Time vs. R_D and C_T



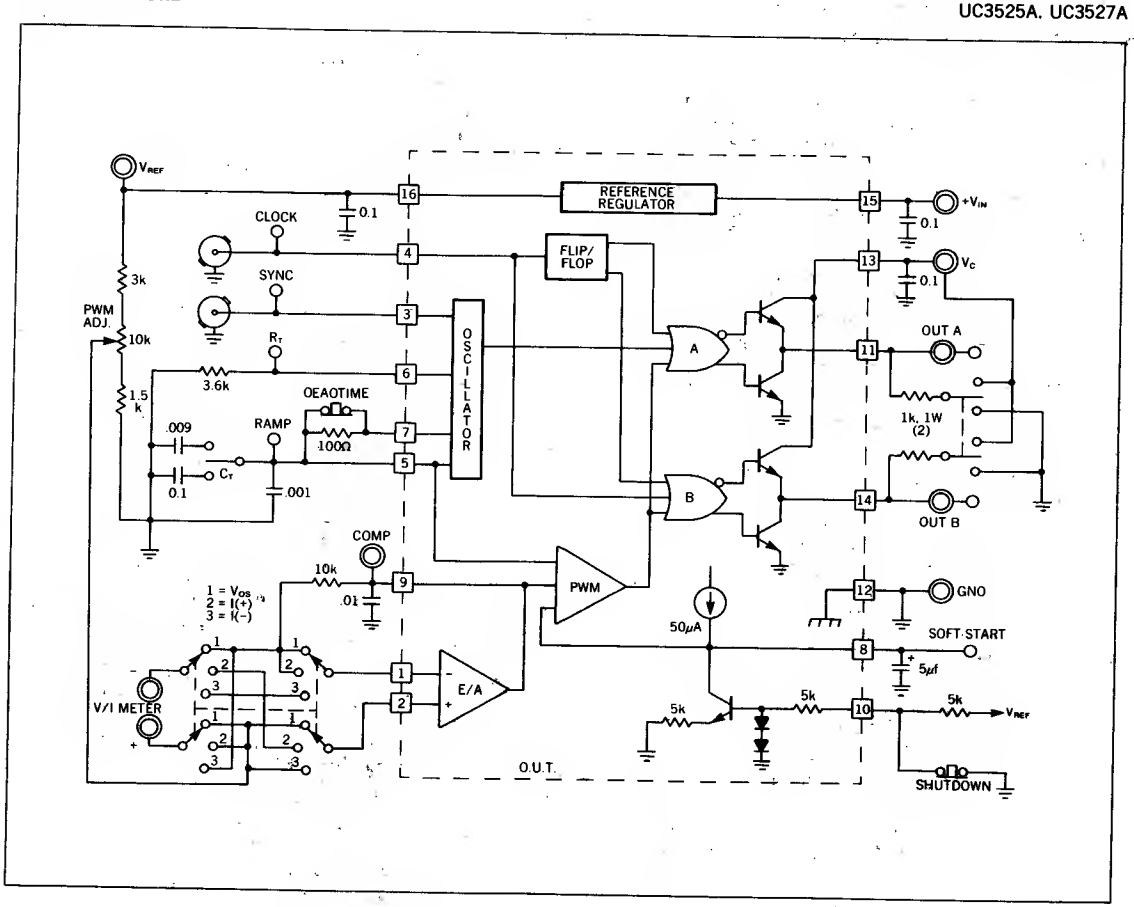
MAXIMUM VALUE Rd Vs MINIMUM VALUE Rt



Error Amplifier Voltage Gain and Phase vs Frequency



LAB TEST FIXTURE



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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

UC1526
UC2526
UC3526

Regulating Pulse Width Monitor

FEATURES

- 8 to 35V operation
- 5V reference trimmed to ±1%
- 1Hz to 400kHz oscillator range
- Dual 100mA source/sink outputs
- Digital current limiting
- Double pulse suppression
- Programmable deadtime
- Under-voltage lockout
- Single pulse metering
- Programmable soft-start
- Wide current limit common mode range
- TTL/CMOS compatible logic ports
- Symmetry correction capability
- Guaranteed 6 unit synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of −55°C to +125°C. The UC2526 is characterized for operation from −25°C to +85°C, and the UC3526 is characterized for operation from 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$)	+40V
Collector Supply Voltage ($+V_C$)	+40V
Logic Inputs	−0.3V to +5.5V
Analog Inputs	−0.3V to $+V_{IN}$
Source/Sink Load Current (each output)	200mA
Reference Load Current	50mA
Logic Sink Current	15mA
Power Dissipation at T_A = +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T_C = +25°C (Note 3)	3000mW
Thermal Resistance, Junction to Case	42°C/W
Operating Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 24mW/°C for case temperatures above +25°C.

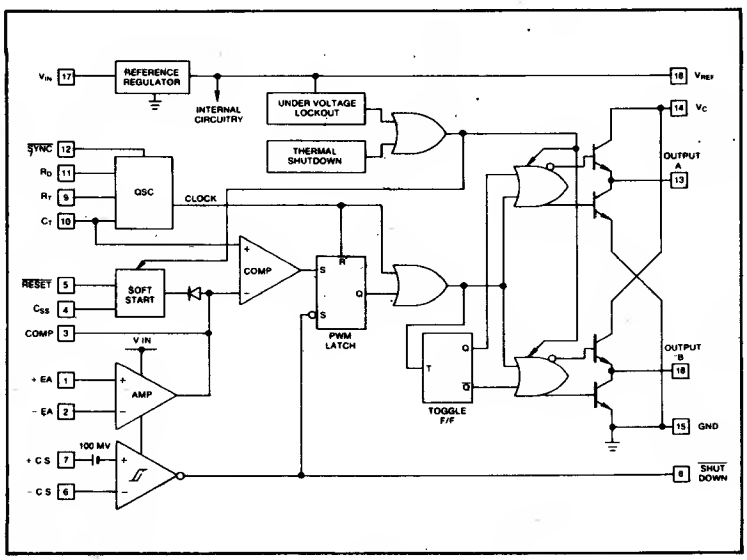
RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage	+8V to +35V
Collector Supply Voltage	+4.5V to +35V
Sink/Source Load Current (each output)	0 to 100mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	1Hz to 400kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	1nF to 20μF
Available Deadtime Range at 40kHz	3% to 50%
Operating Ambient Temperature Range	
UC1526	−55°C to +125°C
UC2526	−25°C to +85°C
UC3526	0°C to +70°C

Note: 4. Range over which the device is functional and parameter limits are guaranteed.

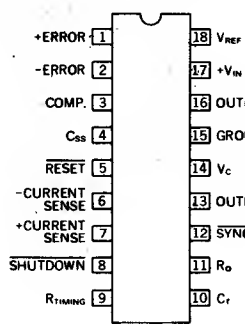
4

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section (Note 5)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 8 to 35V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 7)								
Input Offset Voltage	$R_S \leq$ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$R_L \geq$ 10 Meg Ω	64	72		60	72		dB
HIGH Output Voltage	Vpin1-Vpin2≥150mV, I_{source} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	Vpin2-Vpin1≥150mV, I_{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq$ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	$V_{compensation}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{compensation}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{source} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{sink} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA

Notes: 5. I_L = 0mA.
6. F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = .01μF ± 1%, R_D = 0Ω
7. V_{CM} = 0 to +5.2V

ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1526/UC2526			UC3526			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Comparator (Note 8)								
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I_{source} = 20mA	12.5	13.5		12.5	13.5		V
	I_{source} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{sink} = 20mA		0.2	0.3		0.2	0.3	V
	I_{sink} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	μA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	μs
Power Consumption (Note 10)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		18	30		18	30	mA

Notes: 8. V_{CM} = 0 to +12V
9. V_C = +15V
10. +V_{IN} = +35V, R_T = 4.12kΩ

4

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

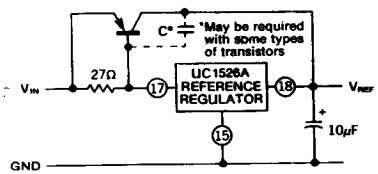


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage. If +V_{IN} is too low, the circuit disables the output drivers and holds the $\overline{RESET}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{RESET}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When +V_{IN} to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{RESET}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the V_{REF} pin to the +V_{IN} pin and maintaining the supply between +4.8 and +5.2V.

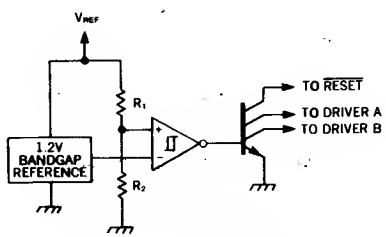


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q_3. Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q_1 turns off, allowing the internal 100μA current source to charge C_S. Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

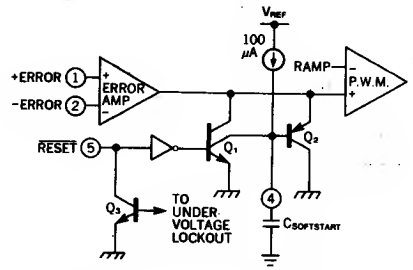


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

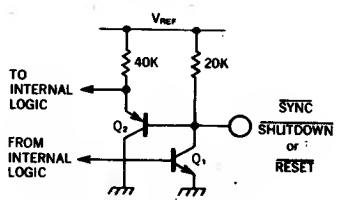


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T, C_T and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a large value of R_D. At 40kHz dead time increases by 400nS/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5μs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

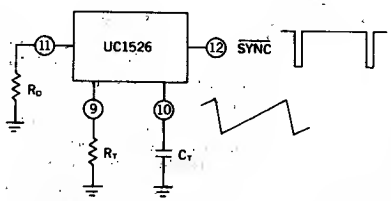


Figure 5. Oscillator Connections and Waveforms

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

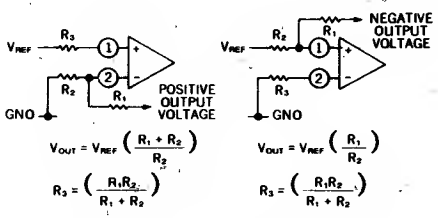


Figure 6. Error Amplifier Connections

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

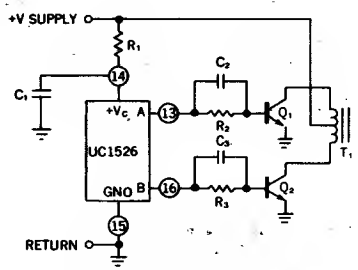


Figure 7. Push-Pull Configuration

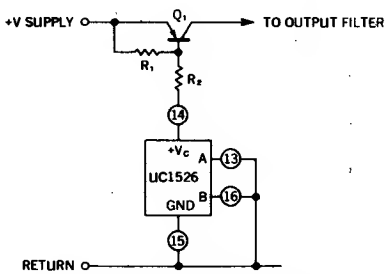


Figure 8. Single-Ended Configuration

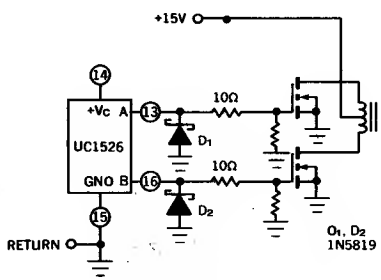
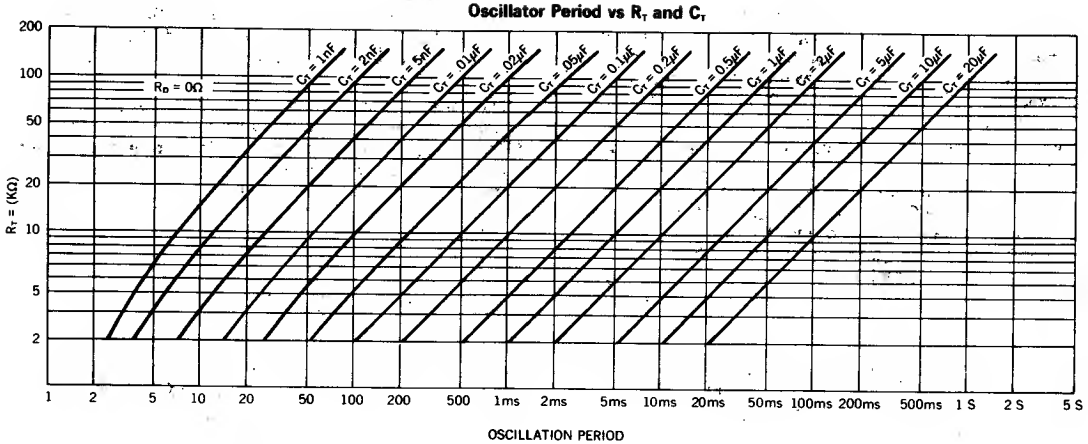


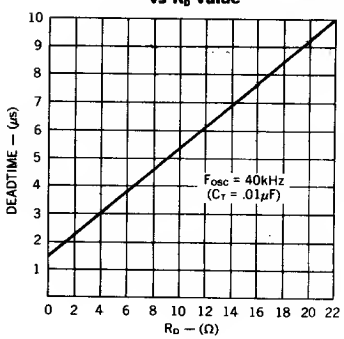
Figure 9. Driving N-Channel Power Mosfets

TYPICAL CHARACTERISTICS

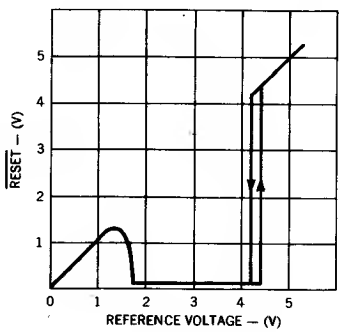
Oscillator Period vs R_T and C_T



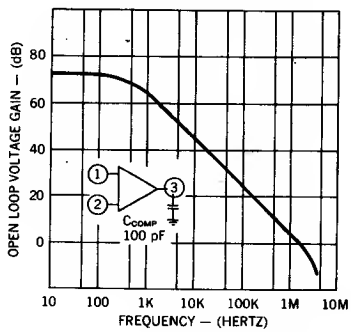
Output Driver Deadtime vs R_D Value



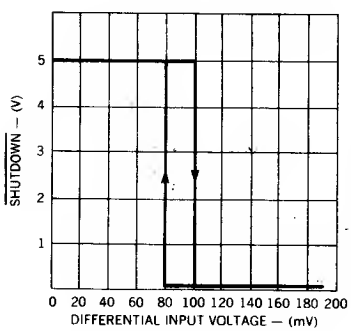
Under-Voltage Lockout Characteristic



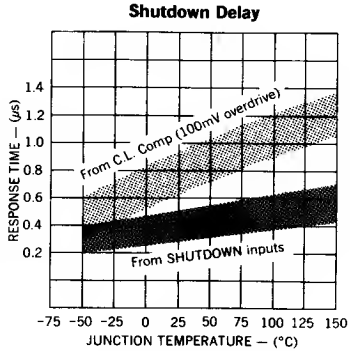
Error Amplifier Open Loop Gain vs Frequency



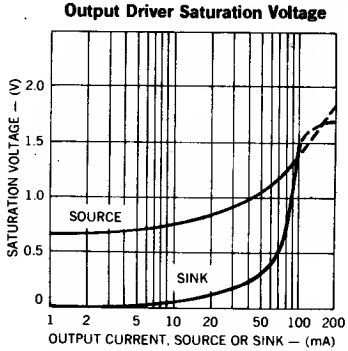
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



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INTEGRATED CIRCUITS

UNITRODE

Regulating Pulse Width Modulator

UC1526A
UC2526A
UC3526A

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600KHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation ($V_{IN} = V_C = V_{REF} = 5.0V$)

DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non-"A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting V_{IN}, V_C and V_{REF} to a precision 5V input supply. Consult factory for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage ($+V_{IN}$)	+40V
Collector Supply Voltage ($+V_C$)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to $+V_{IN}$
Source/Sink Load Current (each output)	200mA
Reference Load Current	50mA
Logic Sink Current	15mA
Power Dissipation at T_A = +25°C (Note 2)	1000mW
Thermal Resistance, Junction to Ambient	100°C/W
Power Dissipation at T_C = +25°C (Note 3)	3000mW
Thermal Resistance, Junction to Case	42°C/W
Operating Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

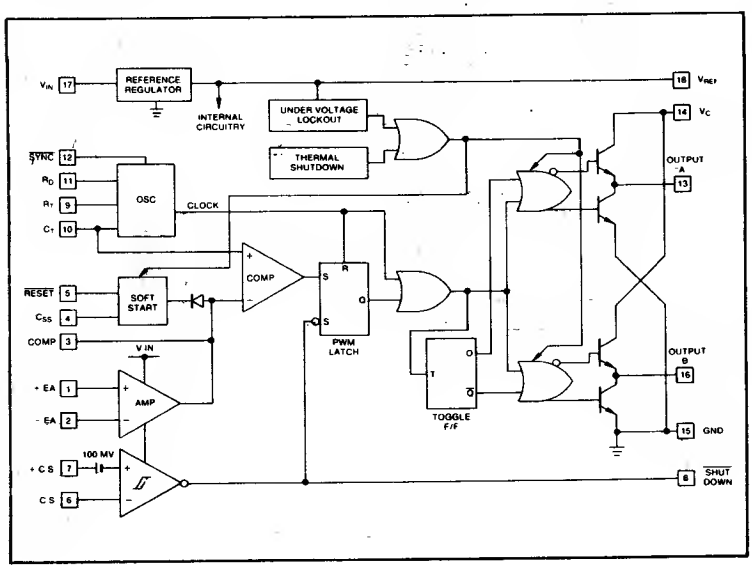
Notes: 1. Values beyond which damage may occur.
2. Derate at 10mW/°C for ambient temperatures above +50°C.
3. Derate at 24mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS (Note 4)

Input Voltage	+7V to +35V
Collector Supply Voltage	+4.5V to +35V
Sink/Source Load Current (each output)	0 to 100mA
Reference Load Current	0 to 20mA
Oscillator Frequency Range	1Hz to 600kHz
Oscillator Timing Resistor	2kΩ to 150kΩ
Oscillator Timing Capacitor	400pF to 20μF
Available Deadtime Range at 40kHz	1% to 50%
Operating Ambient Temperature Range	
UC1526A	-55°C to +125°C
UC2526A	-25°C to +85°C
UC3526A	0°C to +70°C

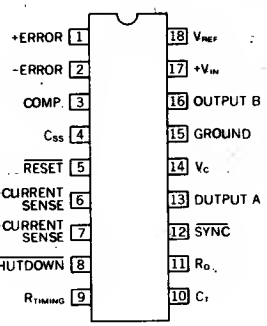
Note: 4. Range over which the device is functional and parameter limits are guaranteed.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (+V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1526A/UC2526A			UC3526A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section (Note 5)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T_J (Note 6)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 7)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J (Note 6)		2	6		1	3	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF (Note 6)			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 7V	0.5	1.0		0.5	1.0		V
$\overline{\text{SYNC}}$ Pulse Width	T_J = 25°C, R_L = 2.7kΩ to V_{REF}		1.1			1.1		μs
Error Amplifier Section (Note 8)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10 Meg Ω	64	72		60	72		dB
HIGH Output Voltage	Vpin1-Vpin2≥150mV, I_{source} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	Vpin2-Vpin1≥150mV, I_{sink} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 7)								
Minimum Outy Cycle	$V_{compensation}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{compensation}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, SHUTDOWN, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{source} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{sink} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA
Shutdown Delay	From Pin 8, T_J = 25°C		160			160		ns

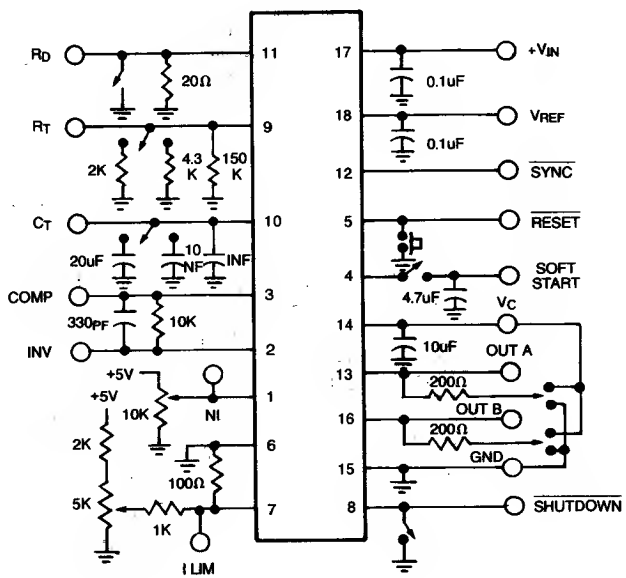
Notes: 5. I_L = 0mA.
6. Guaranteed by design, not 100% tested in production.
7. Fosc = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01μF ± 1%, R_D = 0Ω)
8. V_{CM} = 0 to +5.2V

ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1526A/UC2526A			UC3526A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit Comparator (Note 9)								
Sense Voltage	$R_S \leq 50\Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Delay	From Pin 7, 100mV Overdrive, T_J = 25°C		260			260		nS
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 10)								
HIGH Output Voltage	I_{source} = 20mA	12.5	13.5		12.5	13.5		V
	I_{source} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{sink} = 20mA		0.2	0.3		0.2	0.3	V
	I_{sink} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	μA
Rise Time	C_L = 1000pF (Note 6)		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF (Note 6)		0.1	0.2		0.1	0.2	μs
Cross-Conduction Charge	Per cycle, T_J = 25°C		8			8		nC
Power Consumption (Note 11)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		14	20		14	20	mA

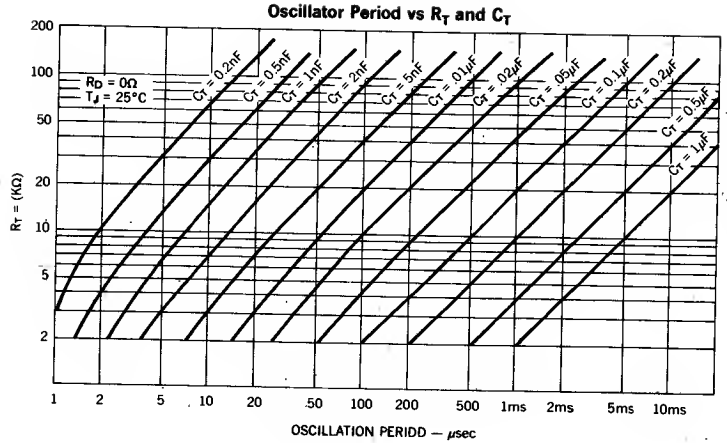
Notes: 9. V_{CM} = 0 to +12V
10. V_C = +15V
11. $+V_{IN}$ = +35V, R_T = 4.12kΩ

OPEN LOOP TEST CIRCUIT
UC1526A

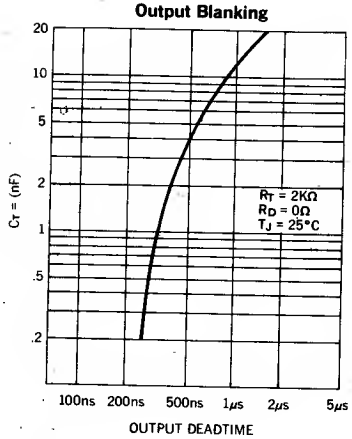


TYPICAL CHARACTERISTICS

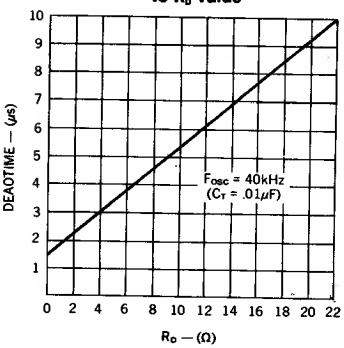
Oscillator Period vs R_T and C_T



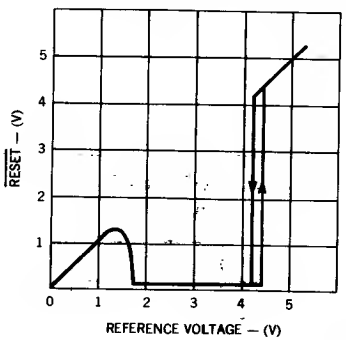
Output Blanking



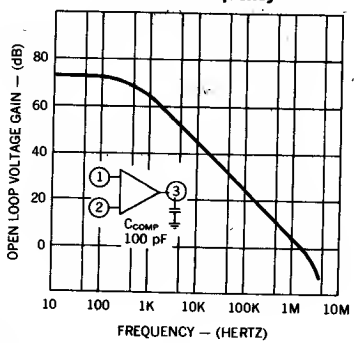
Output Driver Deadtime vs R_D Value



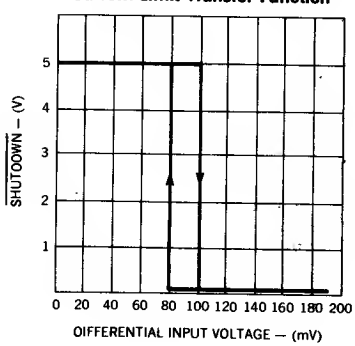
Under-Voltage Lockout Characteristic



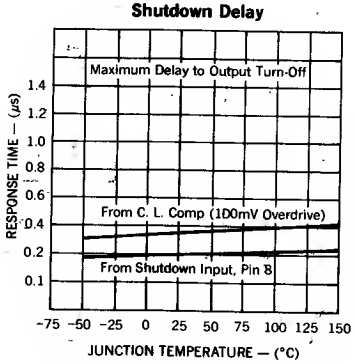
Error Amplifier Open Loop Gain vs Frequency



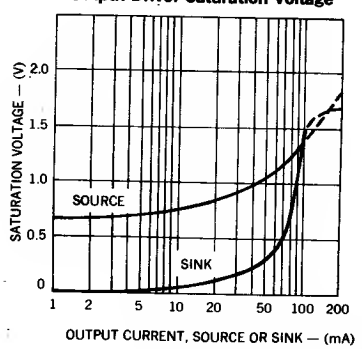
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

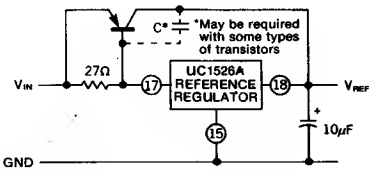


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{RESET}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{RESET}$ pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{RESET}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2V.

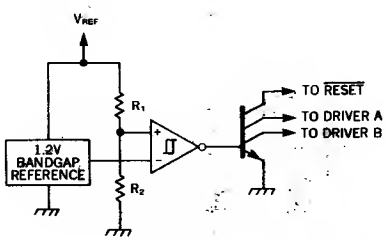


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds $\overline{RESET}$ LOW with Q_3. Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{RESET}$ will go HIGH. Q_1 turns off, allowing the internal 100μA current source to charge C_S. Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

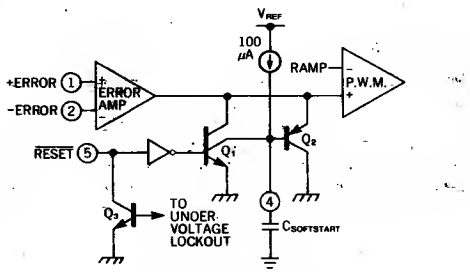


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{SYNC}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{SHUTDOWN}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{RESET}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

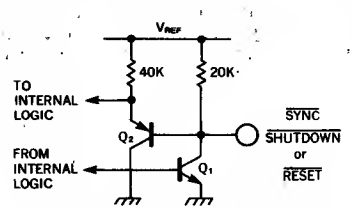


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T, C_T and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D. At 40kHz dead time increases by $400ns/\Omega$.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately $0.5\mu s$ wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{SYNC}$ terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

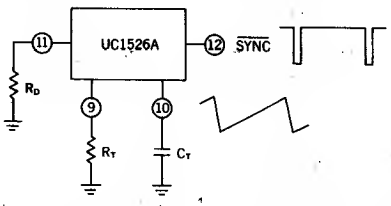


Figure 5. Oscillator Connections and Waveforms

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

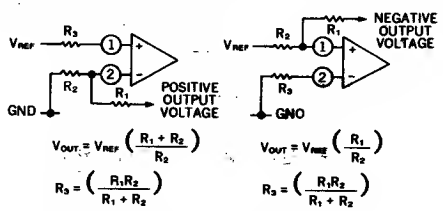


Figure 6. Error Amplifier Connections

Output Drivers

The totem-pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at V_C is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

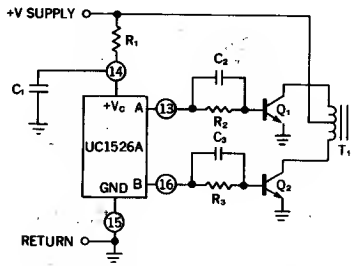


Figure 7. Push-Pull Configuration

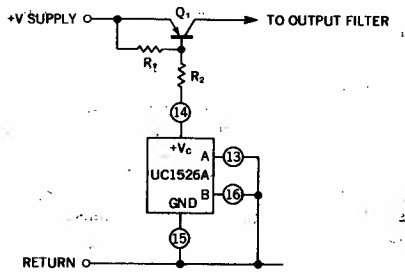


Figure 8. Single-Ended Configuration

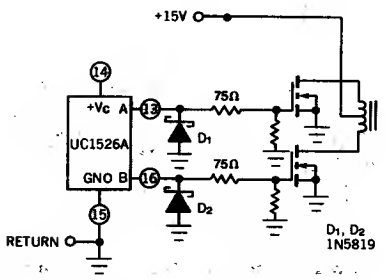


Figure 9. Driving N-Channel Power Mosfets

INTEGRATED CIRCUITS

UNITRODE

Power Supply Supervisory Circuit

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

FEATURES

- Includes over-voltage, under-voltage, and current sensing circuits
- Internal 1% accurate reference
- Programmable time delays
- SCR "crowbar" drive of 300mA
- Remote activation capability
- Optional over-voltage latch
- Uncommitted comparator inputs for low voltage sensing (UC1544 series only)

DESCRIPTION

These monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage.

The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

4

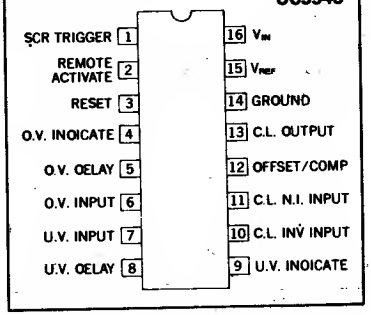
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs, Voltage Range	0 to V_{IN}
SCR Trigger Current	-600mA*
Indicator Output Voltage	40V
Indicator Output Sink Current	50mA
Power Dissipation (Package Limitation)	1000mW
Derate Above 25°C	8.0mW/°C
Operating Temperature Range	
UC1543, UC1544	-55°C to +125°C
UC2543, UC2544	-25°C to +85°C
UC3543, UC3544	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

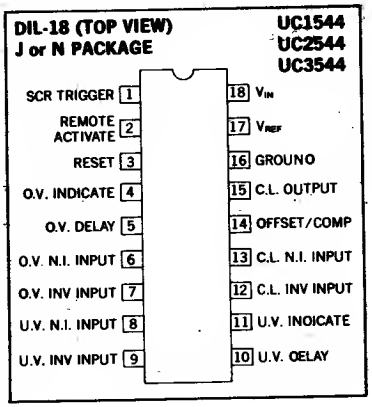
*At higher input voltages, a dissipation limiting resistor, R_S, is required.
Note: Currents are positive into, negative-out of the specified terminal.

CONNECTION DIAGRAMS

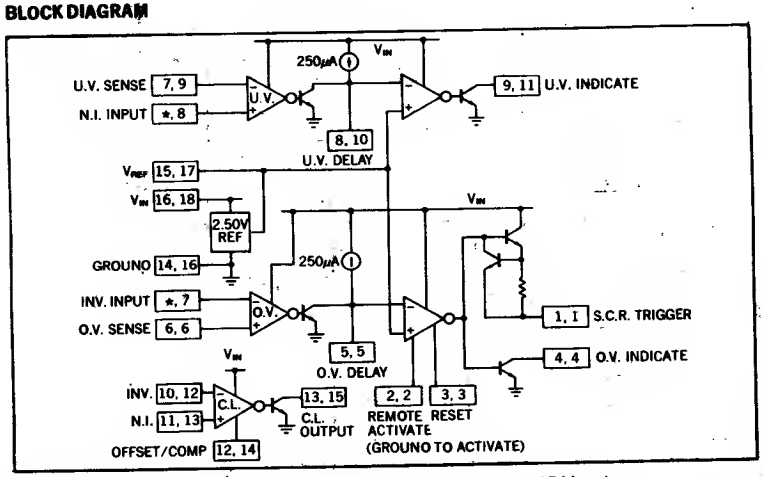
DIL-16 (TOP VIEW)
J or N PACKAGE
UC1543 UC2543 UC3543



DIL-18 (TOP VIEW)
J or N PACKAGE
UC1544 UC2544 UC3544



BLOCK DIAGRAM

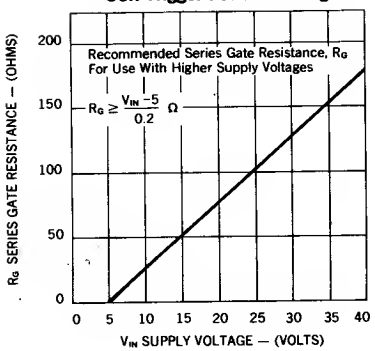


Note: For each terminal, first number refers to 1543 series, second to 1544 series.
★ On 1543 series, this function is internally connected to V_{REF}.

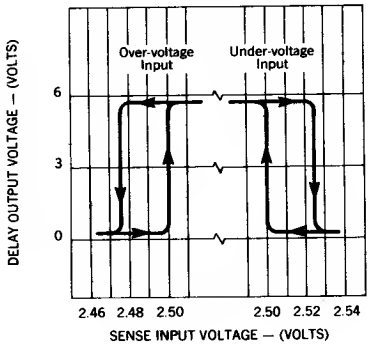
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1543 & UC1544; −25°C to +85°C for the UC2543 & UC2544; and 0°C to +70°C for the UC3543 & UC3544; and for V_{IN} = 5 to 35V. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical ratings and specifications for the UC1544, UC2544 & UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference.) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1543/UC2543 UC1544/UC2544			UC3543 UC3544			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
Input Voltage Range	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Outputs Open T_j = 25°C		7	10		7	10	mA
	$T_{MIN} \le T_j \le T_{MAX}$			15			15	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	−12	−20	−40	−12	−20	−40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	−100	−300	−600	−100	−300	−600	mA
Peak Output Voltage	V_{IN} = 15V, I_D = −100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		−0.4	−0.8		−0.4	−0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		−0.4	−0.8		−0.4	−0.8	mA
Reset Voltage	Reset Open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/μs
Prop. Delay from R/A			300			300		ns
Prop. Delay from O/V input			500			500		ns
Comparator Sections								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		−0.3	−1.0		−0.3	−1.0	μA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_D = 0	−200	−250	−300	−200	−250	−300	μA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	μA
Propagation Delay	Input Dverdrive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Dverdrive = 200mV, T_J = 25°C, C_D = 1μF		10			10		ms
Current Limit Section								
Input Voltage Range		0		(V_{IN}−3V)	0		(V_{IN}−3V)	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		−0.3	−1.0		−0.3	−1.0	μA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
Input Offset Voltage	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVDL	Offset Pin Open, V_{CM} = 0V, R_L = 10k to 15k Ω, V_{OUT} = 1 to 6V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	μA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{overdrive}$ = 100mV, T_J = 25°C		200			200		ns

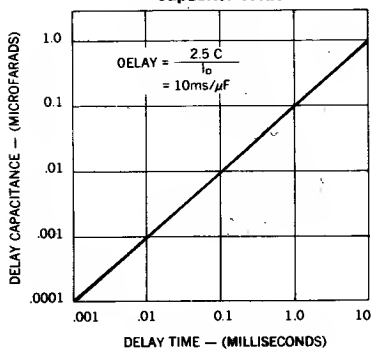
SCR Trigger Power Limiting



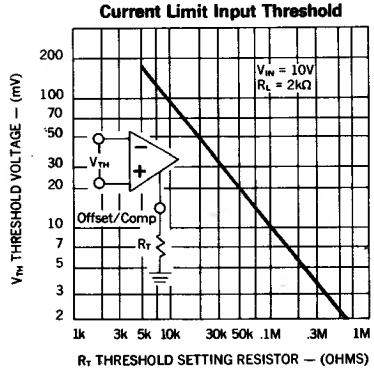
Comparator Input Hysteresis



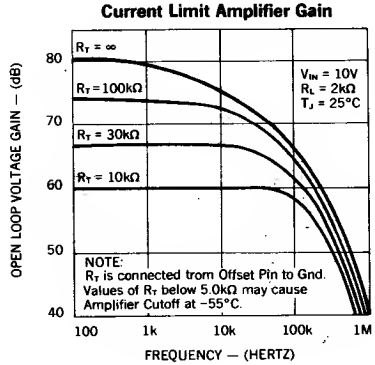
Activation Delay vs Capacitor Value



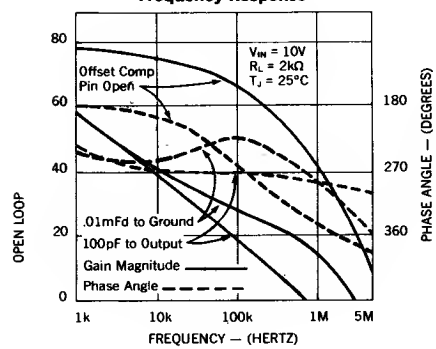
Current Limit Input Threshold



Current Limit Amplifier Gain

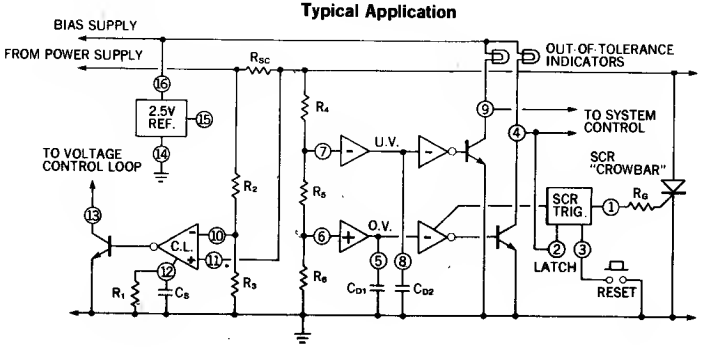


Current Limit Amplifier Frequency Response



APPLICATIONS (Pin Numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{th} \approx \frac{1000}{R_1}$

C_s is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{V_{th}}{R_{SC}} + \frac{V_O}{R_{SC}} \left(\frac{R_2}{R_2 + R_3} \right)$

Short circuit current, $Isc = \frac{V_{th}}{R_{SC}}$

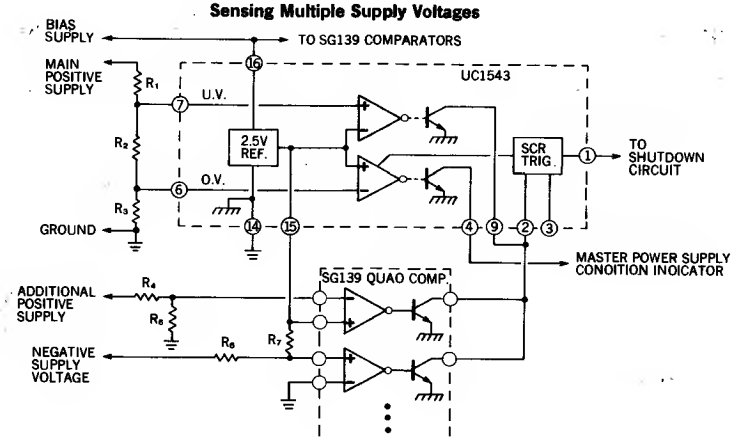
Low output voltage limit, $V_O\,(Low) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit $V_O\,(High) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_6}$

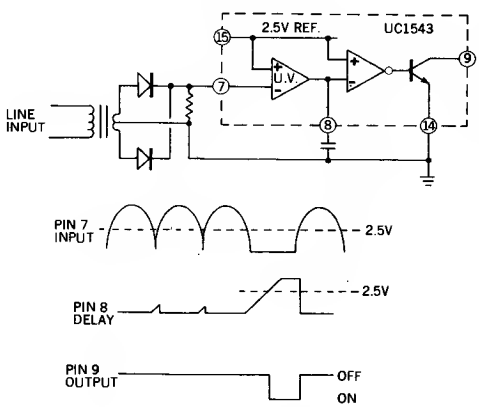
Voltage sensing delay, $t_d = 10{,}000\ Cd$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

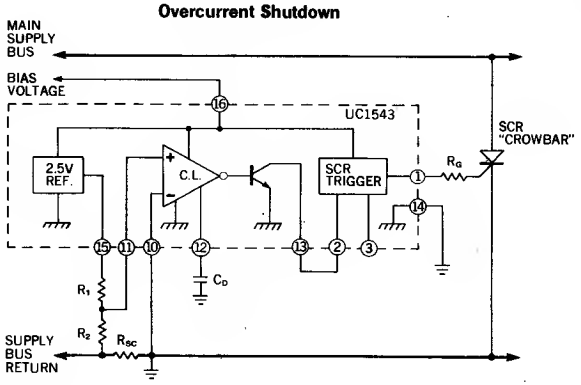
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



UC1610
UC3610

DUAL Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic cerdip and copper-leaded plastic minidip packages. The UC1610 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C ambient temperature range.

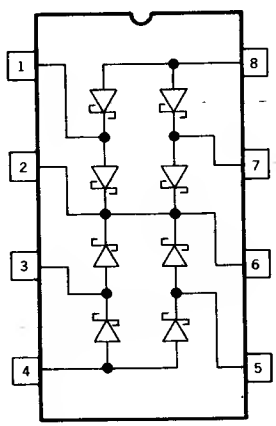
4

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 ..... 1A
  UC3610 ..... 3A
Power Dissipation at T_A = 70°C 1W
  Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE

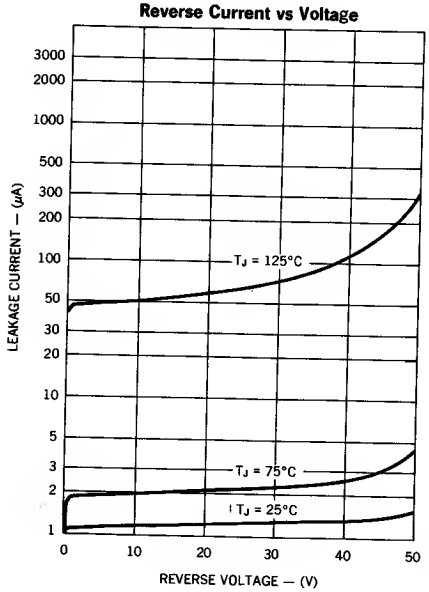


ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = 25°C except as noted.) $T_A = T_J$

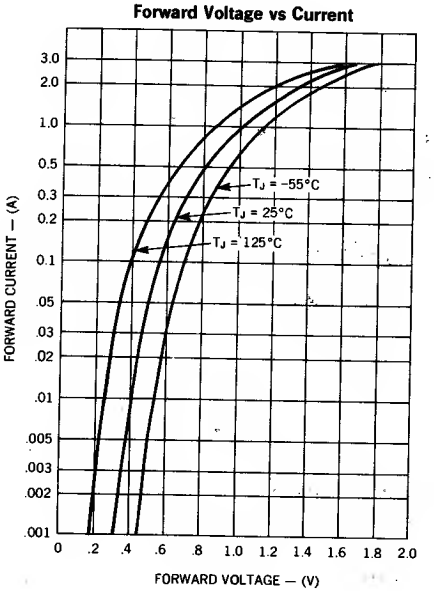
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA I_F = 1A	0.4 0.8	0.5 1.0	0.7 1.3	V
Leakage Current	V_R = 40V V_R = 40V, T_J = 100°C		.01 0.1	0.1 1.0	mA
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

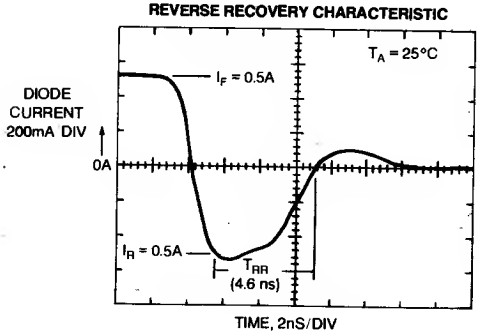
Reverse Current vs Voltage



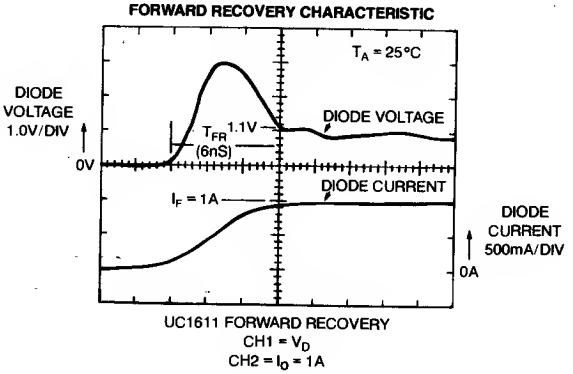
Forward Voltage vs Current



REVERSE RECOVERY CHARACTERISTIC



FORWARD RECOVERY CHARACTERISTIC



Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

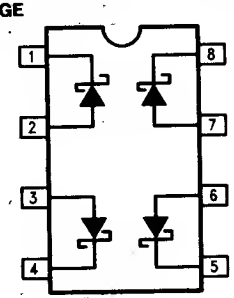
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic MINIDIP packages. The UC1611 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability, while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
  UC1611 ..... 1A
  UC3611 ..... 3A
Power Dissipation at T_A = +70°C 1W
  Derate 12.5 mW/°C above +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

CONNECTION DIAGRAM

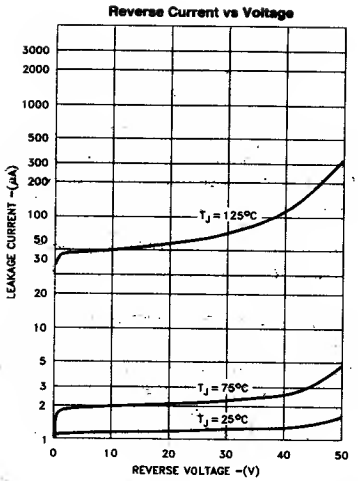
DIL-8 (TOP VIEW)
J or N PACKAGE

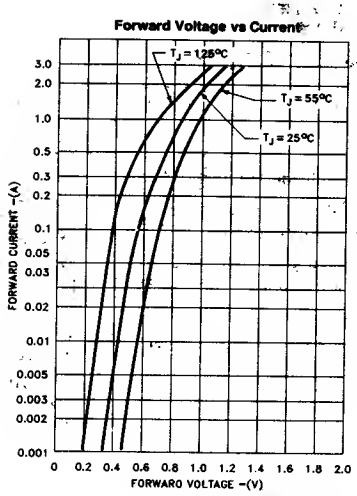


ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = +25°C except as noted.) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100 mA I_F = 1A	0.4	0.5 0.9	0.7 1.2	V
Leakage Current	V_R = 40V V_R = 40V, T_J = +100°C		0.01 0.1	0.1 1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

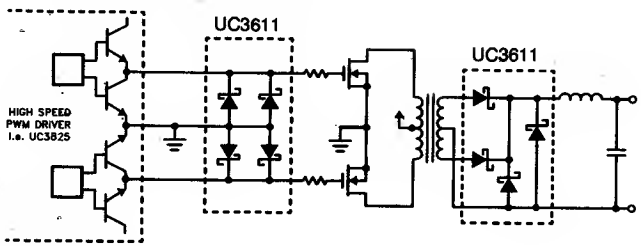




0004-2

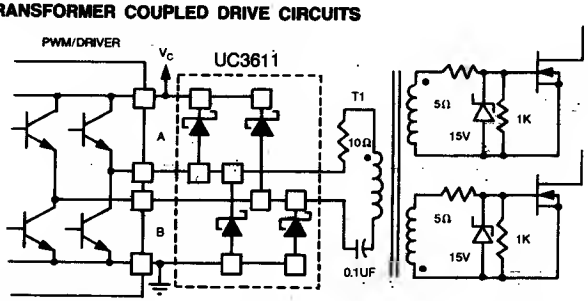
TYPICAL APPLICATIONS

A. CLAMP DIODES - PWMS AND DRIVERS

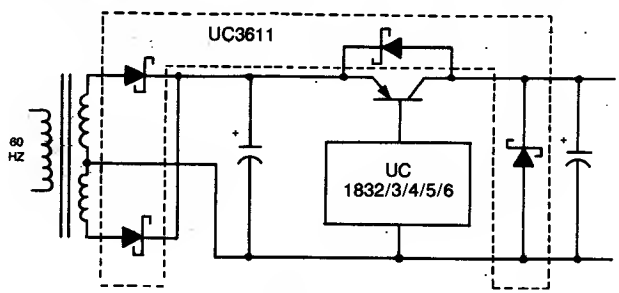


0004-3

B. TRANSFORMER COUPLED DRIVE CIRCUITS



C. LINEAR REGULATORS



Unitrode Integrated Circuits Corporation
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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

High Speed PWM Controller

UC1823
UC2823
UC3823

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V +/- 1%)

DESCRIPTION

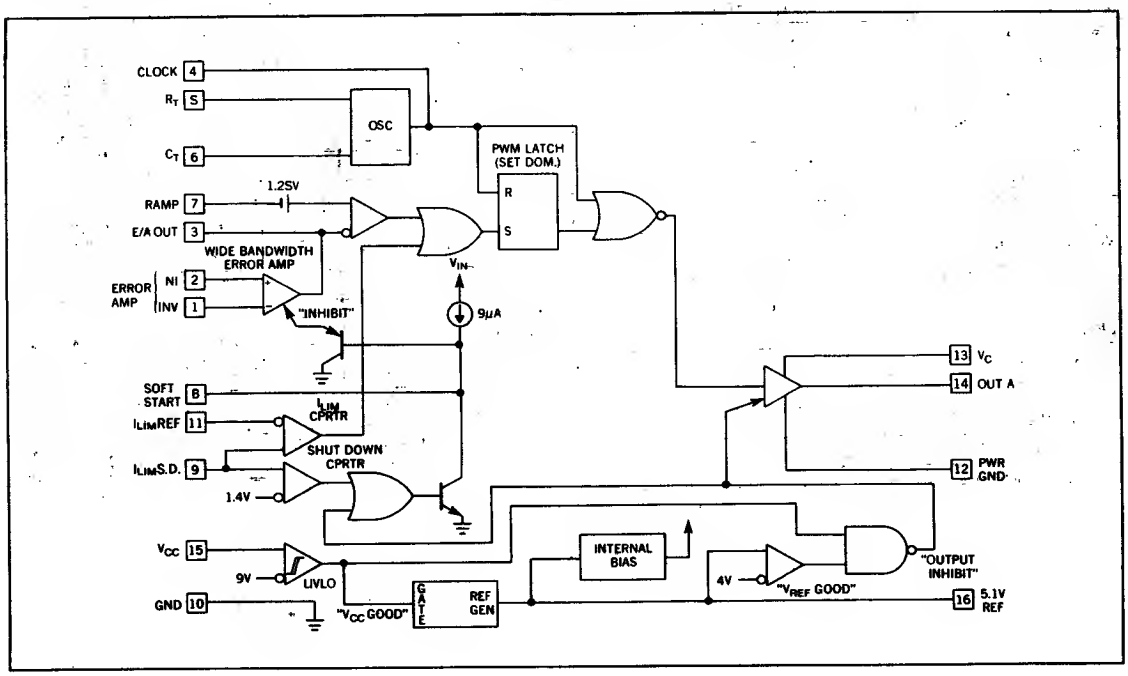
The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

4

BLOCK DIAGRAM



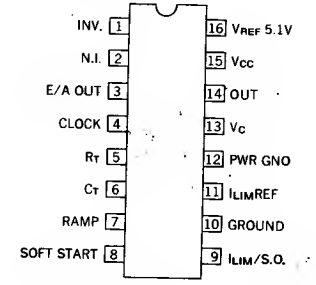
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9) ..... −0.3V to +6V
Clock Output Current (Pin 4) ..... −5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... −5mA
Power Dissipation at T_A = 60°C 1W
Derate 11mW/°C for $T_A > 60°C$
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

NOTE: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, −25°C < T_A < +85°C for the UC2823, and −55°C < T_A < +125°C for the UC1823.) $T_A = T_J$

PARAMETERS	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10KHz		50			50		μV
Long Term Stability*	T_j = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	−15	−50	−100	−15	−50	−100	mA
Oscillator Section								
Initial Accuracy*	T_j = 25°C	360	400	440	360	400	440	KHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	KHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, $0°C < T_A < +70°C$ for the UC3823, $-25°C < T_A < +85°C$ for the UC2823, and $-55°C < T_A < +125°C$ for the UC1823.) $T_A = T_J$

PARAMETERS	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	μA
Input Offset Current			0.1	1		0.1	1	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/μs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	μA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	μA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			±10			±10	μA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		
Collector Leakage	V_C = 30V		100	500		100	500	μA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

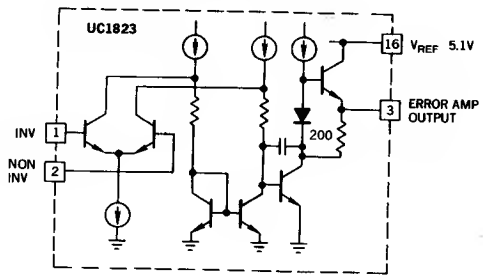
* This parameter not 100% tested in production but guaranteed by design.

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

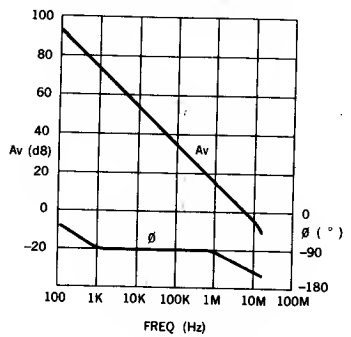
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

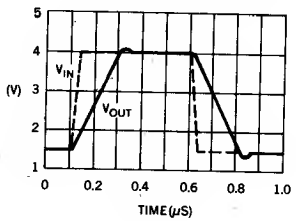
Simplified Schematic



Open Loop Frequency Response

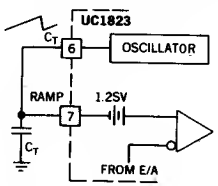


Unity Gain Slew Rate

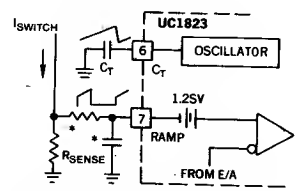


PWM APPEICATIONS

Conventional (Voltage Mode)

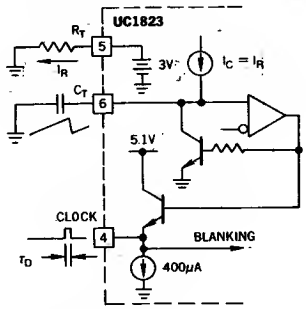


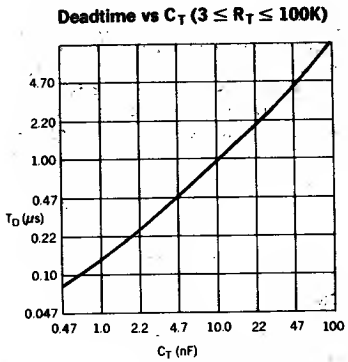
Current-Mode

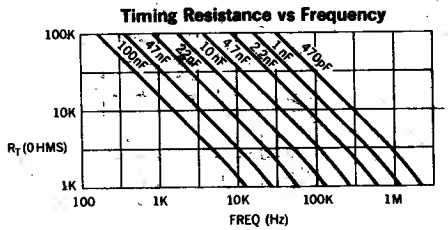


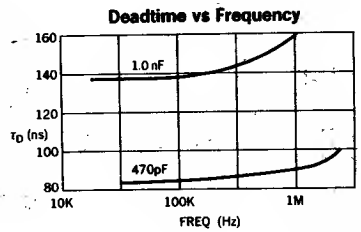
* A SMALL FILTER MAY BE REQUIRED TO SUPPRESS SWITCH NOISE

OSCILLATOR CIRCUIT



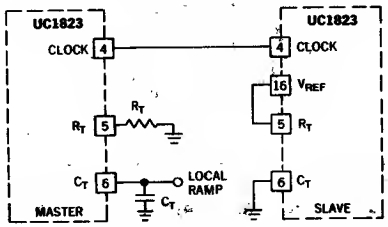




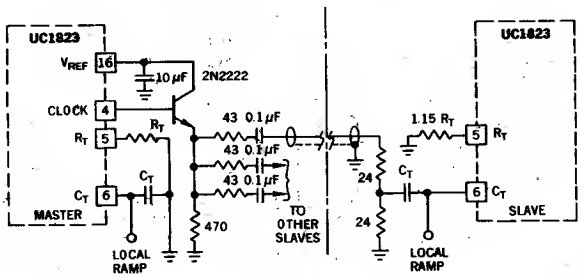


SYNCHRONIZED OPERATION

Two Units in Close Proximity:

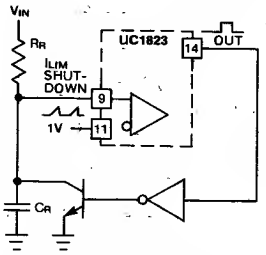


Generalized Synchronization:



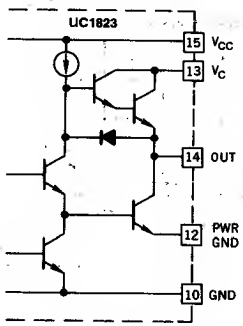
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

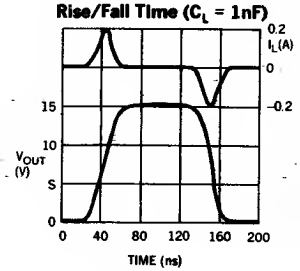


OUTPUT SECTION

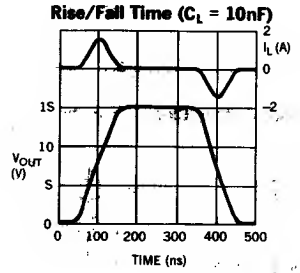
Simplified Schematic



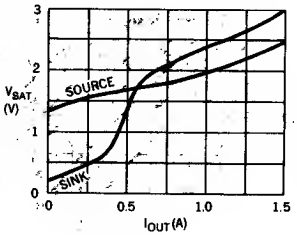
Rise/Fall Time (C_L = 1nF)



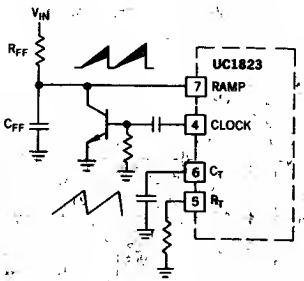
Rise/Fall Time (C_L = 10nF)



Saturation Curves



FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



High Speed PWM Controller

ADVANCED PRODUCT INFORMATION

FEATURES

(Bold type denotes improved or new features)

- Pin For Pin Compatible with the UC1825/UC1823
- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1MHz
- 50ns propagation delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- **Wide Bandwidth Error Amplifier**
- **Trimmed Oscillator Discharge Current for Accurate Frequency & Deed Time Control**
- Fully Latched Logic with Double Pulse Suppression
- Soft Start Control
- Pulse by Pulse Current Limiting Comparator
- **Latched Over-Current Comparator With Full Cycle Reatart**
- **Low Start Up Current—500uA**
- **Under Voltage Lock Out—16V On & 10V Off**
- **Outputs Active Low During UVLO**
- Trimmed Bandgap Reference
- **Adjuatable Blanking For Leading Edge Noise Tolerance**

DESCRIPTION

The UC1825A & UC1823A families of PWM control ICs are improved versions of the standard UC1825 & UC1823A families. They are pin compatible with the earlier versions.

Performance enhancements have been made to some of the circuit blocks. Bandwidth and offset of the error amplifier are improved. The Oscillator discharge current is specified for accurate dead time control. Start up current is reduced for off-line applications and the UVLO thresholds changed to 16/10V. The output drivers are redesigned to actively sink current during UVLO at no expense to the start up current specification.

Functional improvements have been implemented on the UC1825A. The shut down comparator is now a high speed comparator with a threshold of 1.2V. This comparator sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. In the event of continuous faults, the soft start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period.

The Clock pin on the UC1823/25 is a bidirectional clock- output/blanking-input pin. On the A version, it is a high speed Schottky TTL compatible output driver. Clock synchronization is achieved by inserting a short pulse in series with the timing capacitor. The specified oscillator discharge current will allow controlled dead times.

A leading edge blanking circuit has been added to the chip to allow for controlled duty cycles of 5 to 90%. Zero duty cycle is still a valid operation condition. This feature greatly enhances the tolerance of the control chip to leading edge switch noise, requiring minimal, if any, filtering on the current sense input.

Contact the factory for further information.

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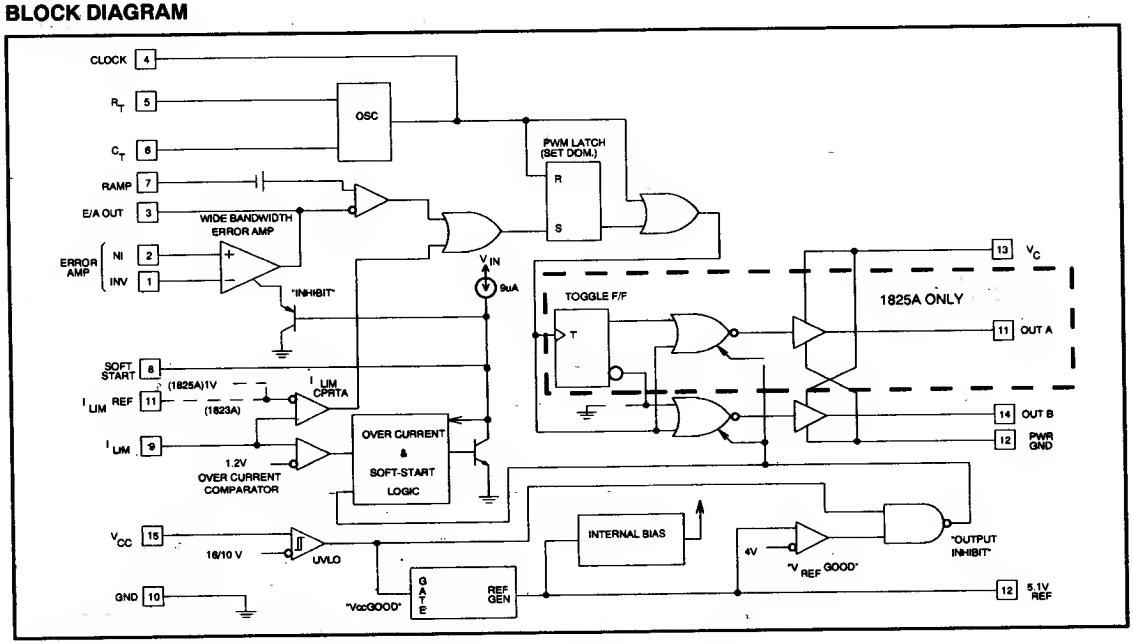
BLOCK DIAGRAM



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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

High Speed PWM Controller

UC1825
UC2825
UC3825

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V +/- 1%)

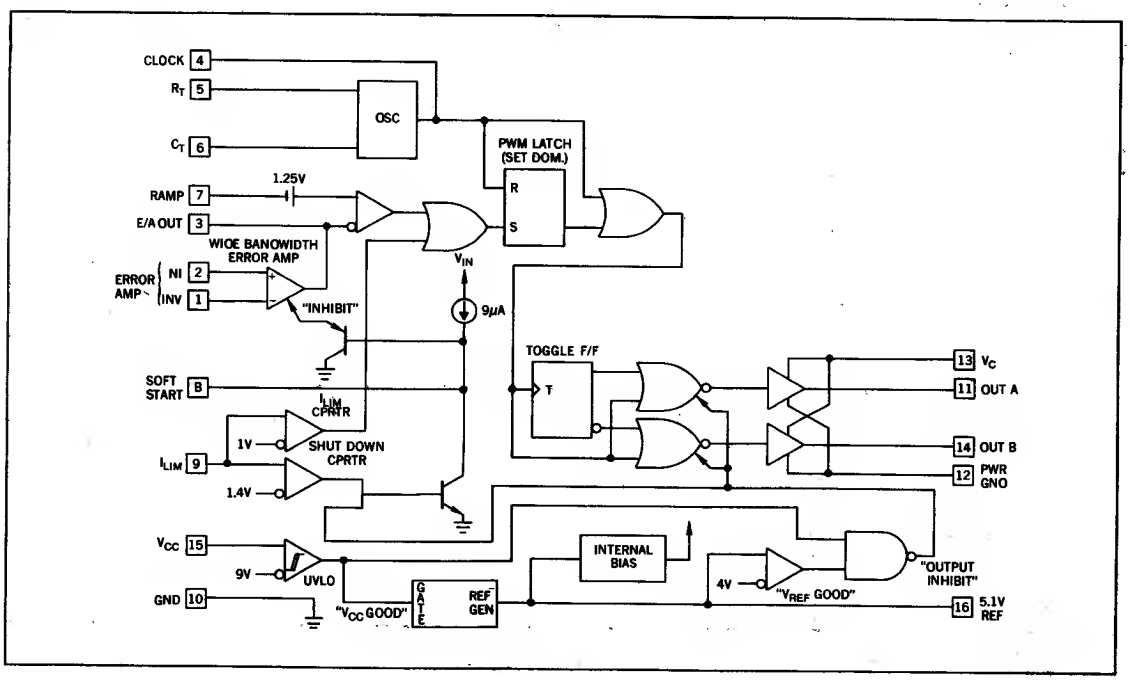
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

BLOCK DIAGRAM



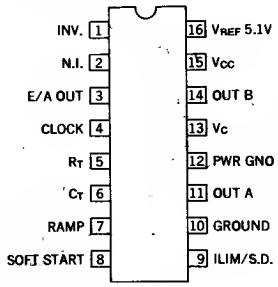
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... -0.3V to 7V
(Pin 9, 8) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation at T_A = 60°C 1W
Derate 11mW/°C for $T_A > 60°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

NOTE: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, $0 < T_A < 70°C$ for the UC3825, $-25°C < T_A < 85°C$ for the UC2825, and $-55°C < T_A < 125°C$ for the UC1825.) $T_A = T_J$

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$10 < V_{CC} < 30V$		2	20		2	20	mV
Load Regulation	$1 < I_O < 10mA$		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10KHz		50			50		μV
Long Term Stability*	T_j = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_j = 25°C	360	400	440	360	400	440	KHz
Voltage Stability*	$10 < V_{CC} < 30V$		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	KHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* This parameter not 100% tested in production but guaranteed by design.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply for R_T = 3.65K, C_T = 1nF, V_{CC} = 15V, $0 < T_A < 70°C$ for the UC3825, $-25°C < T_A < 85°C$ for the UC2825, and $-55°C < T_A < 125°C$ for the UC1825.) $T_A = T_J$

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			±15			±10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		
Collector Leakage	V_C = 30V		100	500		100	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

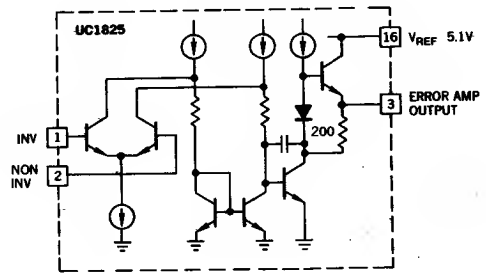
* This parameter not 100% tested in production but guaranteed by design.

UC1825 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

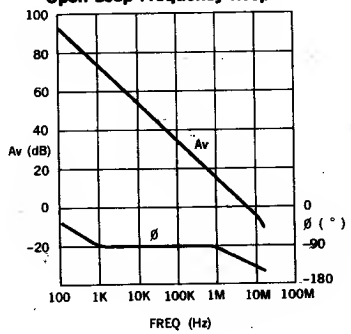
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825, follow these rules. 1) Use a grdund plane. 2) Bamp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

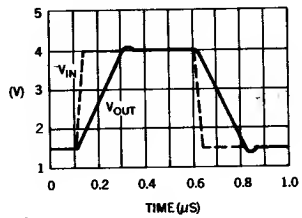
Simplified Schematic



Open Loop Frequency Response

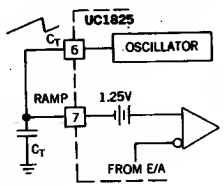


Unity Gain Slew Rate

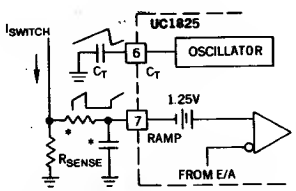


PWM APPLICATIONS

Conventional (Voltage Mode)

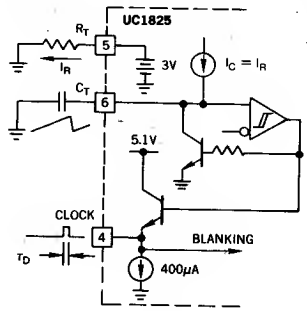


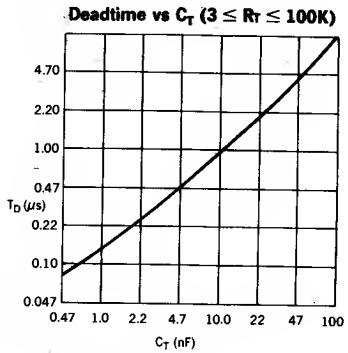
Current-Mode

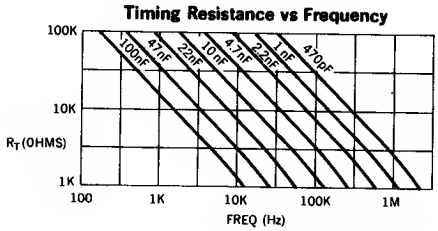


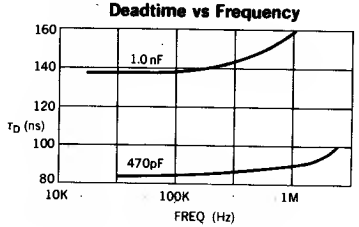
* A SMALL FILTER MAY BE REQUIREO TO SUPPRESS SWITCH NOISE

OSCILLATOR CIRCUIT



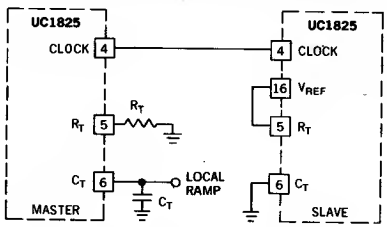




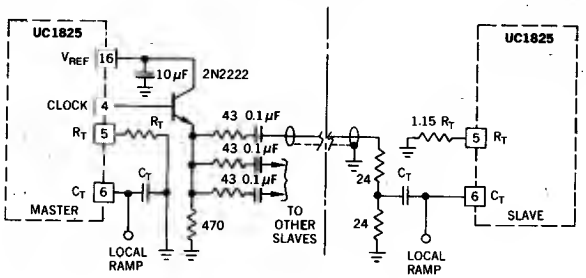


SYNCHRONIZED OPERATION

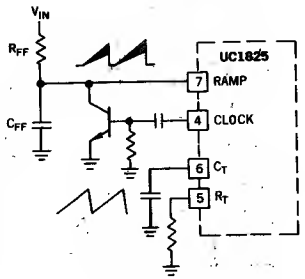
Two Units in Close Proximity:



Generalized Synchronization:

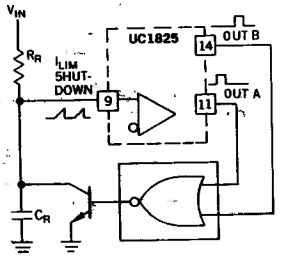


FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



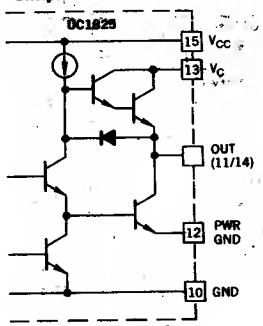
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

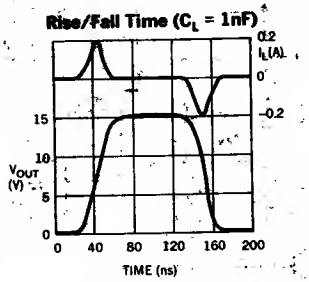


OUTPUT SECTION

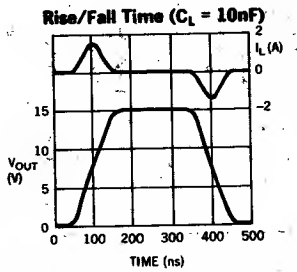
Simplified Schematic



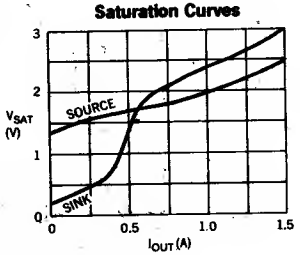
Rise/Fall Time (C_L = 1nF)



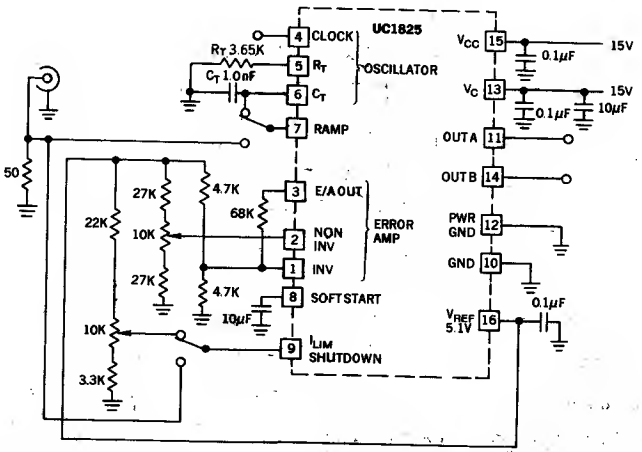
Rise/Fall Time (C_L = 10nF)



Saturation Curves



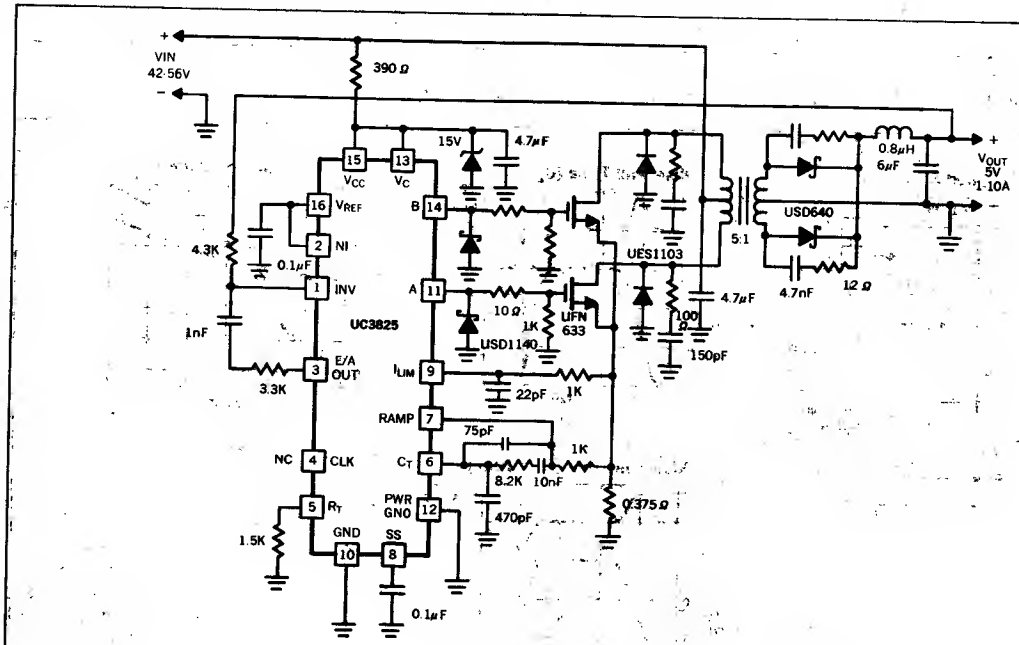
OPEN LOOP LABORATORY TEST FIXTURE



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

DESIGN EXAMPLE: 50W, 48V to 5V DC TO DC CONVERTER — 1.5MHz CLOCK FREQUENCY



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INTEGRATED CIRCUITS

UNITRODE

UC1832 UC1833
UC2832 UC2833
UC3832 UC3833

Precision Low Dropout Linear Controllers

PRELIMINARY

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5V to 36V Operation
- 100mA Output Drive, Source or Sink
- Under-Voltage Lockout

Additional Features of the UC1832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate $+V_{in}$ terminal
- Programmable Driver Current Limit
- Access to V_{REF} and E/A(+)
- Logic-Level Disable Input

DESCRIPTION

The UC1832 and UC1833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCxx32 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

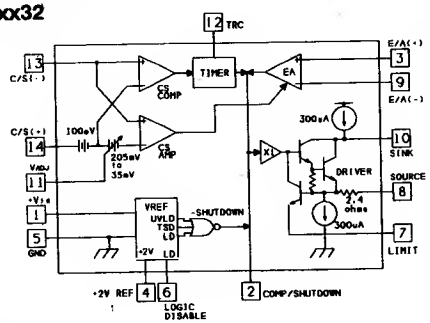
These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The UC1833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC1832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); industrial (–25°C to 85°C), order UC2832/3 (N or J); and military (–55°C to 125°C), order UC1832/3J. Surface mount packaging is also available, please consult the factory for further information.

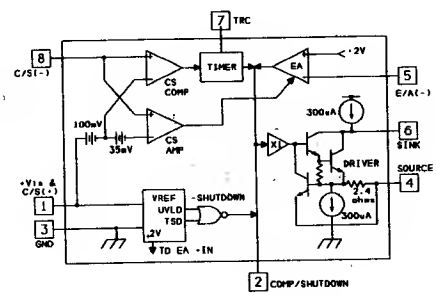
4

BLOCK DIAGRAM

UCxx32



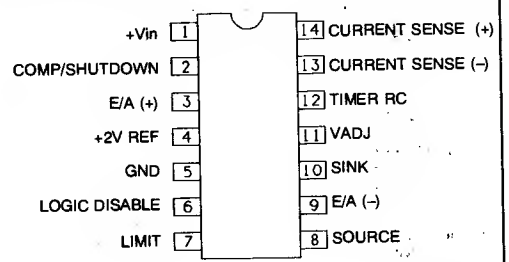
UCxx33



CONNECTION DIAGRAMS:

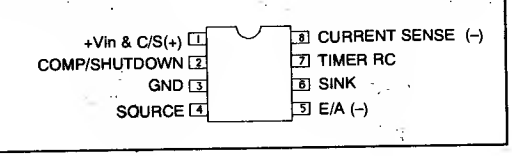
DIL–14 (TOP VIEW)
J or N Package

UC1832
UC2832
UC3832



DIL–8 (TOP VIEW)
J or N Package

UC1833
UC2833
UC3833



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $+V_{in}$ 40V
Driver Output Current (Sink or Source) 450mA
Driver Sink to Source Voltage 40V
TRC Pin Voltage . . . . . −0.3V to 3.2V
Other Input Voltages . . . . . −0.3V to $+V_{in}$
Operating Junction Temperature (note 2) . . . . . −55°C to +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

NOTE 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals

NOTE 2: Consult Unitrode Integrated Circuits databook packaging information section for information regarding thermal specifications and limitations of packages.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for TA = 0°C to 70°C for the UC3832/3, −25°C to 85°C for the UC2832/3, and −55°C to 125°C for the UC1832/3, +Vin = 15V, Driver sink = +Vin, C/S(+) voltage = +Vin TA=Tj.

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
Input Supply					
Supply Current	+Vin = 6V		6.5	10	mA
	+Vin = 36V		9.5	15	mA
	Logic Disable = 2V (UCxx32 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	Tj = 25°C, IDRIVER =10mA	1.98	2.00	2.02	V
	over temperature, IDRIVER =10mA	1.96	2.00	2.04	V
Load Regulation (UCxx32 only)	Iout = 0 to 10mA	−10	−5.0		mV
Line Regulation	+Vin = 4.5 to 36V, IDRIVER = 10mA		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCxx32 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Pin 6 = 0V	−5.0	−1.0		µA
Current Sense Section					
Comparator Offset		95	100	105	mV
Amplifier Offset (UCxx33 only)		110	135	160	mV
Amplifier Offset (UCxx32 only)	Vadj = Open	110	135	160	mV
	Vadj = 1V	180	235	290	mV
	Vadj = 0V	250	305	360	mV
Input Bias Current	Vcm = +Vin	65	100	135	µA
Input Offset Current (UCxx32 only)	Vcm = +Vin	−10		10	µA
Amplifier CMRR (UCxx32 only)	V_{cm}=4.1V to $+V_{in}$+0.3V		80		dB
Transconductance	Icomp = ±100uA		65		mS
Vadj Input Current (UCxx32 only)	Vadj = 0V	−10	−1		µA
Timer					
Inactive Leakage Current	C/S(+) = C/S(−) = +Vin, TRC pin = 2V		0.25	1.0	µA
Active Pullup Current	C/S(+) = +Vin,C/S(−) = +Vin−0.4V, TRC pin = 0V	−345	−270	−210	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, $+V_{in}$ = 15V, Driver sink = $+V_{in}$, C/S(+) voltage = $+V_{in}$ T_A=T_j.

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
Timer (Continued)					
Duty Ratio (note 4)	ontime/period, R_t = 200k, C_t = .27uF		4.8		%
Period (notes 4,5)	ontime+offtime, R_t = 200k, C_t = .27uF		36		msec
Upper Trip Threshold (Vu)			1.8		V
Lower Trip Threshold (Vl)			0.95		V
Trip Threshold Ratio	Vu/Vl		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCxx32 only)	Vcm = Vcomp = 2V	–8.0		8.0	mV
Input Bias Current	Vcm = Vcomp = 2V	–4.5	–1.1		µA
Input Offset Current (UCxx32 only)	Vcm = Vcomp = 2V	–1.5		1.5	µA
AVOL	Vcomp = 1V to 13V	50	70		dB
CMRR (UCxx32 only)	Vcm = 0V to $+V_{in}$–3V	60	80		dB
PSRR (UCxx32 only)	Vcm = 2V, $+V_{in}$ = 4.5 to 36V		90		dB
Transconductance	Icomp = ±10µA		4.3		mS
VOH	Icomp = 0, Volts below $+V_{in}$		.95	1.3	V
VOL	Icomp = 0		.45	0.7	V
IOH	Vcomp = 2V	–700	–500	–100	µA
IOL	Vcomp = 2V, C/S(–) = $+V_{in}$	100	500	700	µA
	Vcomp = 2V, C/S(–) = $+V_{in}$–0.4V	2	6		mA
Driver					
Maximum Curren	Driver Limit & Source pins common, T_j = 25°C	230	300	400	mA
	Over Temperature	100	300	450	mA
Limiting Voltage	Driver Limit to Source voltage at current limit, I_{SOURCE} = –10mA T_J=25°C (Note 6)		.72		V
Internal Current Sense Resistance	T_J=25°C (Note 6)		2.4		ohms
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.4V Driver Sink = $+V_{in}$ – 1V	–800	–300	–100	µA
Pull-Down Current at Driver Source	Compensation/Shutdown = 0.4V Driver Source = 1V	150	300	700	µA
Saturation Voltage Sink to Source	Driver Source=0V Driver Current = 100mA		1.5		V
Maximum Source Voltage	Driver Sink = $+V_{in}$, Driver Current = 100mA, Volts below $+V_{in}$		3.0		V
UVLO Sink Leakage	$+V_{in}$ = C/S(+) = C/S(–) = 2.5V, Driver Sink = 15V, Driver Source = 0V, T_A = 25°C		25		µA
Maximum Reverse Source Voltage	Compensation/Shutdown = 0V Isource = 100µA		1.6		V

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
Driver (Continued)					
ICEO	+Vin = open circuit, Driver Source = 0V Driver Sink = 36V		1.0	10	µA
Thermal Shutdown			160		°C

NOTE 3: On the UCxx33 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving V_{SOURCE} to 2V.

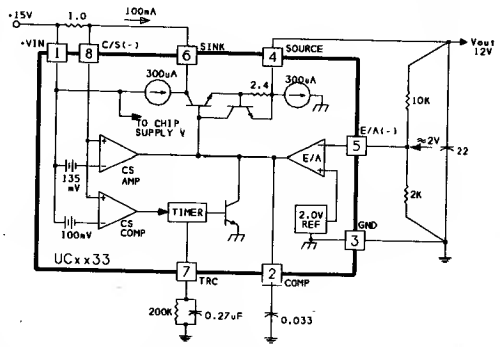
NOTE 4: These parameters are first-order supply-independent, however both may vary with supply for $+V_{in}$ less than about 4V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

NOTE 5: With recommended R_t value of 200k, $T_{off} \approx R_t C_t * \ln(Vu/Vl) \pm 10\%$.

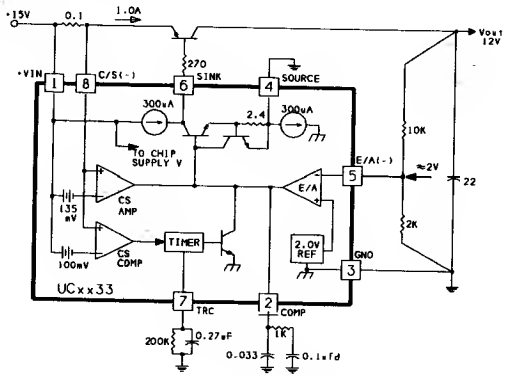
NOTE 6: The internal current limitng voltage has a temperature dependence of approximately –2.0mV/°C, or –2800ppm/°C. The internal 2.4 ohm sense resistor has a temperature dependance of approximately +1500ppm/°C.

APPLICATION AND OPERATION INFORMATION

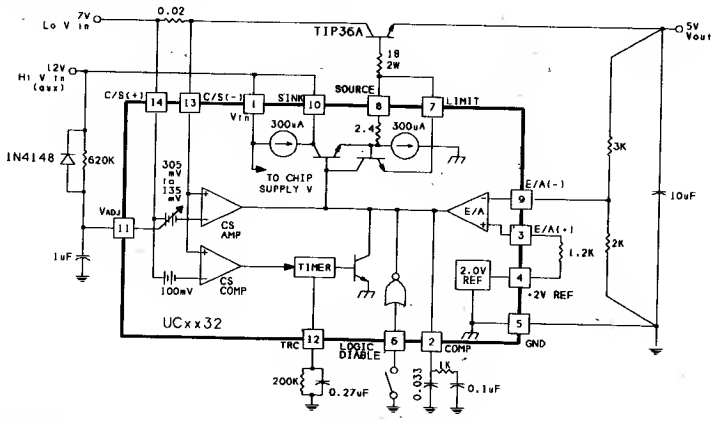
NPN PASS (LOCAL 100mA REGULATOR) (UCxx33)



PNP PASS (LOW DROP-OUT REGULATOR) (UCxx33)



NPN PASS (MEDIUM POWER, LOW DROPOUT REGULATOR)



APPLICATION AND OPERATION INFORMATION (continued)

ESTIMATING MAXIMUM LOAD CAPACITANCE

For any power supply, the rate at which the total output capacitance can be charged depends onthe maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, TON = 0.693 x 10k x CT.

Typically, the IC regulates output current to a maximum of Imax = K x I_{th}, where:

I_{th} is the timer trip-point current,

$K = \frac{\text{Current Sense Amplifer Offset Voltage}}{100mV}$

≈1.35 for UCxx33, is variable from 1.35 to 3.05 with Vadj on UCxx32.

For a worst-case constant-current load of value just less than Ith, C_{max} can be estimated from:

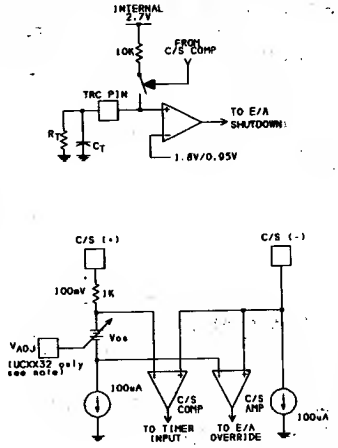
$$C_{max} = ((K-1)\, I_{th})(TON/V_{out}),$$

where V_{out} is the nominal regulator output voltage.

For a resistive load of value RL, the value of C_{max} can be estimated from:

$$C_{max} = \frac{TON}{RL} \cdot \frac{1}{ln\left[\left(1 - \frac{V_{out}}{K\, I_{th}\, RL}\right)^{-1}\right]}$$

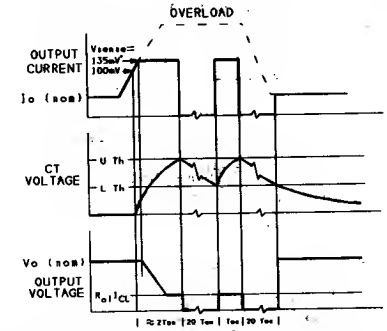
UCxx32/xx33 TIMER FUNCTION



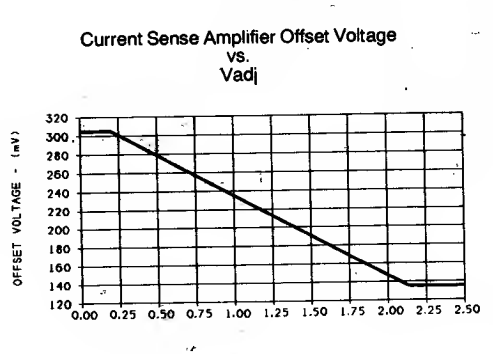
Note: Vos = 35mV for UCxx33

Vos = 205 to 35mV for UCxx32

UCxx32/UCxx33 CURRENT SENSE INPUT CONFIGURATION



Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.



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INTEGRATED CIRCUITS

UNITRODE

High Efficiency Linear Regulator

UC1834
UC2834
UC3834

FEATURES

- Minimum V_{IN} - V_{OUT} less than 0.5V at 5A load with external pass device
- Equally usable for either positive or negative regulator design
- Adjustable low threshold current sense amplifier
- Under and over-voltage fault alert with programmable delay
- Over-voltage fault latch with 100mA crowbar drive output

DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

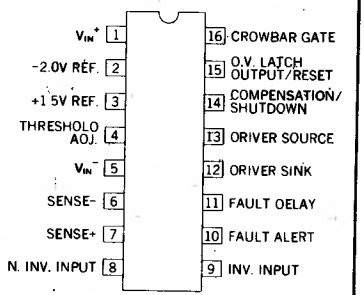
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN}^+	40V
Driver Current	400mA
Driver Source to Sink Voltage	40V
Crowbar Current	-200mA
+1.5V Reference Output Current	-10mA
Fault Alert Voltage	40V
Fault Alert Current	15mA
Error Amplifier Inputs	-0.5V to 35V
Current Sense Inputs	-0.5V to 40V
O.V. Latch Output Voltage	-0.5V to 40V
O.V. Latch Output Current	15mA
Power Dissipation at T_A = 25°C	1000mW
Derate at 10mW/°C above T_A = 50°C	
Power Dissipation at T_C = 25°C	2000mW
Derate at 16mW/°C above T_C = 25°C	
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

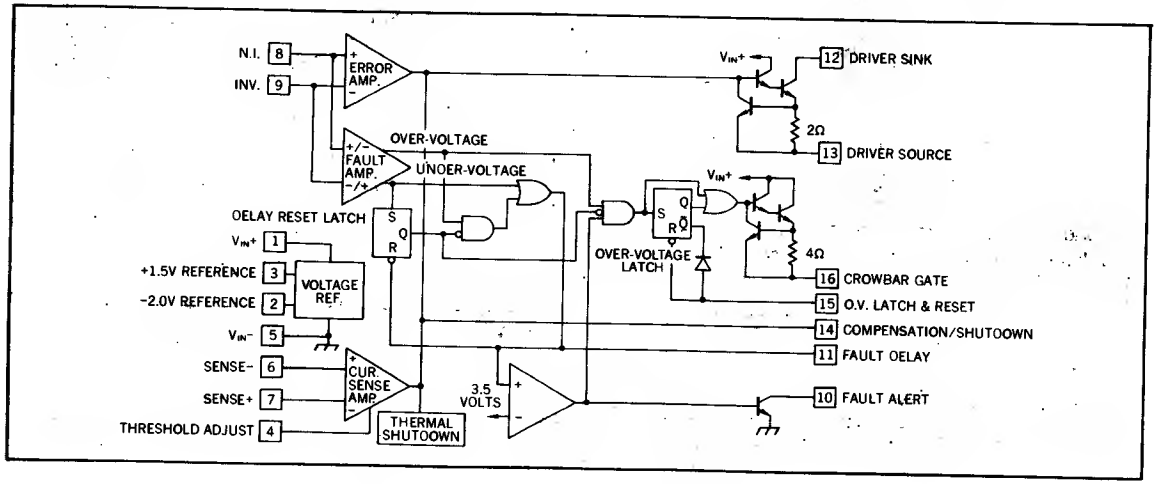
Note: 1. Voltages are reference to V_{IN}^-, Pin 5.
Currents are positive into, negative out of the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1834; −25°C to +85°C for the UC2834; and 0°C to +70°C for the UC3834; V_{IN}^+ = 15V, V_{IN}^- = 0V.) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	T_j = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{j(MIN)} \le T_j \le T_{j(MAX)}$	1.47		1.53	1.455		1.545	
Line Regulation	V_{IN}^+ = 5 to 35V		1	10		1	15	mV
Load Regulation	I_{OUT} = 0 to 2mA		1	10		1	15	mV
−2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN}^+)	T_j = 25°C	2.04	−2	1.96	2.06	−2	1.94	V
	$T_{j(MIN)} \le T_j \le T_{j(MAX)}$	2.06		1.94	2.08		1.92	
Line Regulation	V_{IN}^+ = 5 to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		kΩ
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 1.5V		1	6		1	10	mV
Input Bias Current	V_{CM} = 1.5V		−1	−4		−1	−8	μA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	μA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN}^+ Pin 13, 20Ω to V_{IN}^-	50	65		50	65		dB
CMRR	V_{CM} = 0.5 to 33V, V_{IN}^+ = 35V	60	80		60	80		dB
PSRR	V_{IN}^+ = 5 to 35V, V_{CM} = 1.5V	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	I_{OUT} = 100mA		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V, Pin 13 = V_{IN}^-, Pin 14 = V_{IN}^-		0.1	50		0.1	50	μA
Shutdown Input Voltage at Pin 14	$I_{OUT} \le 100\mu A$, Pin 13 = V_{IN}^-, Pin 12 = V_{IN}^+	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN}^-, Pin 12 = V_{IN}^+, $I_{OUT} \le 100\mu A$, Pin 13 = V_{IN}^-		−100	−150		−100	−150	μA
Thermal Shutdown (Note 3)			165			165		°C
Fault Amplifier Section								
Under- and Over- Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	V_{IN}+ = 35V, V_{CM} = 1.5 to 33V		−0.4	−0.8		−0.4	−1.0	%/V
Supply Sensitivity	V_{CM} =1.5V, V_{IN}^+ = 5 to 35V		−0.5	−1.0		−0.5	−1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/μF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	I_{OUT} =1mA		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	I_{OUT} = 1mA		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		−100	−175		−100	−175		mA
Crowbar Gate Leakage Current	V_{IN}^+ = 35V, Pin 16 = V_{IN}^-		−0.5	−50		−0.5	−50	μA

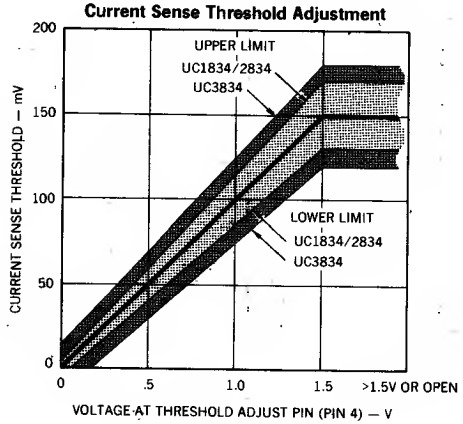
Note: 2. When using both the 1.5V and −2.0V references the current out of Pin 3 should be balanced by an equivalent current into Pin 2. The −2.0V output will change −2.3mV per μA of inbalance.

3. Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown), the O.V. Latch will be reset.

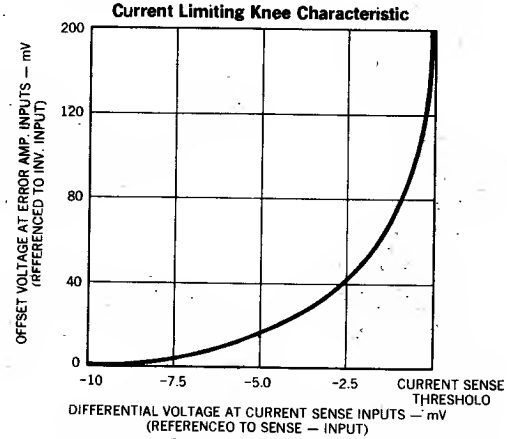
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1834; −25°C to +85°C for the UC2834; and 0°C to +70°C for the UC3834; V_{IN}^+ = 15V, V_{IN}^- = 0V.) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1834/UC2834			UC3834			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, V_{CM} = V_{IN}^+ or V_{IN}^-	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, V_{CM} = V_{IN}^+ or V_{IN}^-	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, V_{CM} = V_{IN}^-, V_{IN}^+ = 5 to 35V		−0.1	−0.3		−0.1	−0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		−2	−10		−2	−10	μA
Sense Input Bias Current	V_{CM} = V_{IN}^+		100	200		100	200	μA
	V_{CM} = V_{IN}^-		−100	−200		−100	−200	

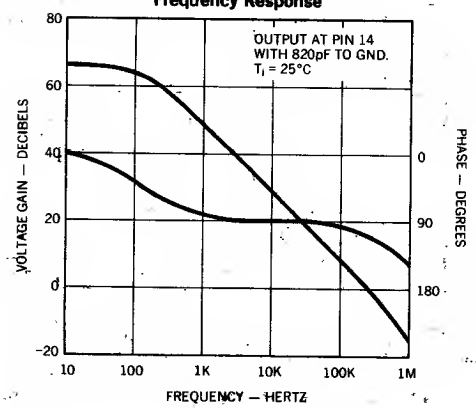
Current Sense Threshold Adjustment



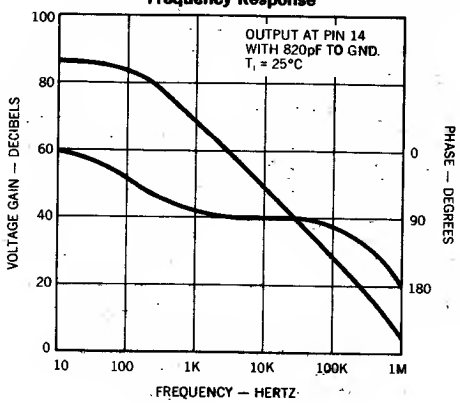
Current Limiting Knee Characteristic



Error Amplifier Gain and Phase Frequency Response

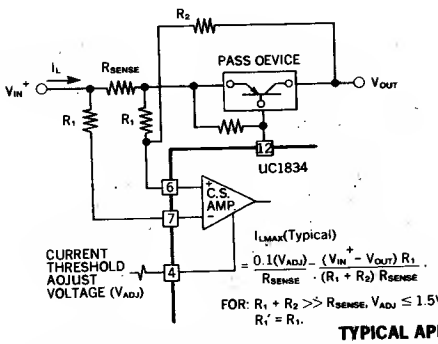


Current Sense Amplifier Gain and Phase Frequency Response



APPLICATION INFORMATION

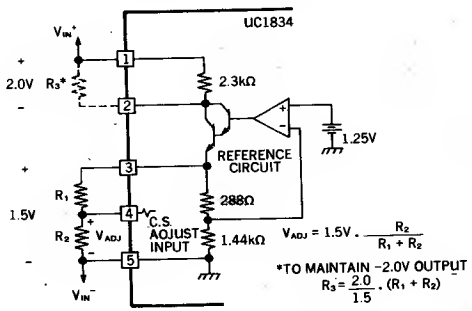
Foldback Current Limiting



$$I_{LMAX}(Typical) = \frac{0.1(V_{ADJ}) - (V_{IN}^{+} - V_{OUT})\,R_1}{R_{SENSE}} \cdot \frac{}{(R_1 + R_2)\,R_{SENSE}}$$

FOR: $R_1 + R_2 >> R_{SENSE}$, $V_{ADJ} \leq 1.5V$, $R_1' = R_1$.

Setting The Threshold Adjust Voltage (V_{ADJ})



TYPICAL APPLICATIONS

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedence at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V\ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V\ C.S./A} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500kHz$ and $|Z_L(f)| \leq 1M\Omega$,

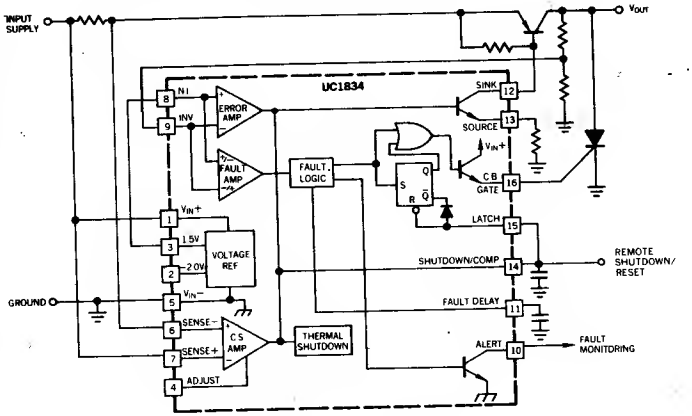
where:

A_V = small signal voltage gain to Pin 14,
$Z_L(f)$ = load impedence at Pin 14.

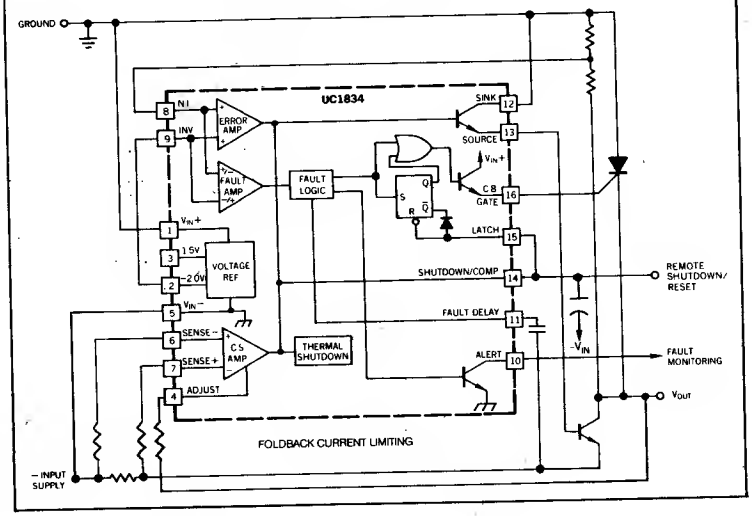
The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-volatge condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its $\overline{Q}$ output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

5-10 AMP Positive Regulator



5-10 AMP Negative Regulator



INTEGRATED CIRCUITS

UNITRODE

High Efficiency Regulator Controller

UC1835 UC1836
UC2835 UC2836
UC3835 UC3836

FEATURES

- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- Packaged in an 8-Pin Mini-Dip

DESCRIPTION

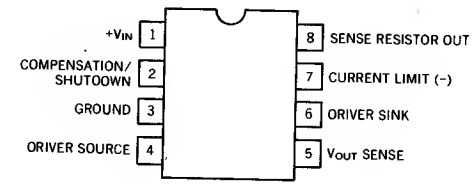
The UC1835/6 families of linear controllers, packaged in 8-pin mini-dips, are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained. These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (UC1835), or adjustable, (UC1836), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE

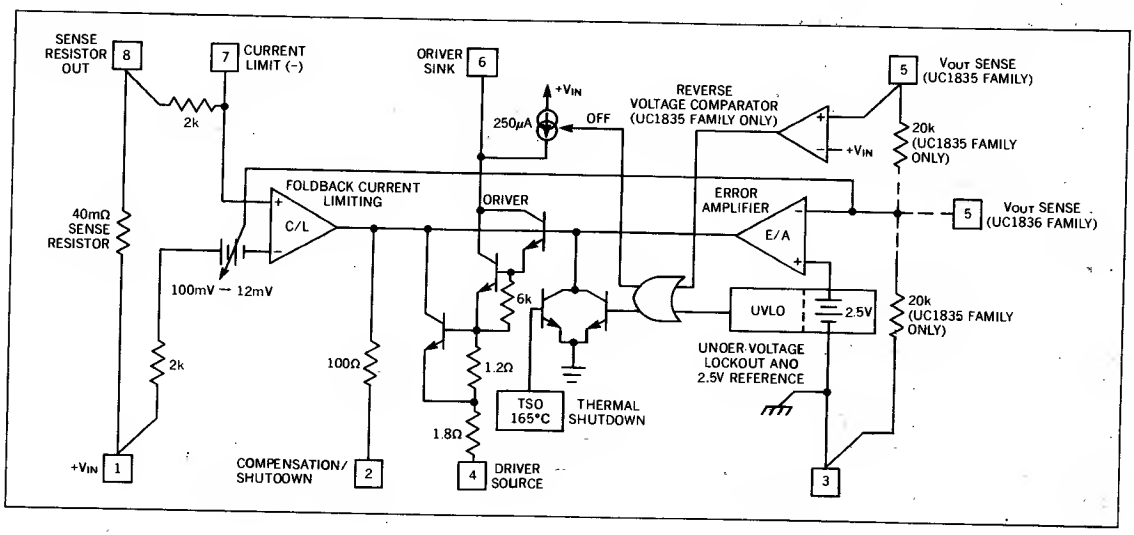


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (+V_{IN}) ..... -1.0V to +40V
Driver Output Current (Sink or Source) 600mA
Driver Source to Sink Voltage ..... +40V
Maximum Current Through Sense Resistor 4A
V_{OUT} Sense Input Voltage ..... -.3V to +40V
Power Dissipation at T_A = 25°C 1000mW
  Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
  Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3835/6, −25°C to +85°C for the UC2835/6 and −55°C to +125°C for the UC1835/6, $+V_{IN}$ = 6V, Driver source = 0V, Driver sink = 5V.) $T_A = T_J$

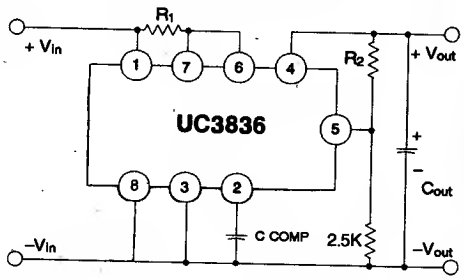
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 6V		2.75	4.0	mA
	$+V_{IN}$ = 40V		3.75	6.0	mA
UVLO Threshold	$+V_{IN}$ Low to High, V_{OUT} Sense = 0V	3.9	4.4	4.9	V
Threshold Hysteresis			0.1	0.35	V
Reverse Current	$+V_{IN}$ = −1.0V, Driver Sink Open		6.0	20	mA
Regulating Voltage and Error Amplifier (UC1835 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	4.94	5.0	5.06	V
	Over Temperature	4.9		5.1	V
Line Regulation	$+V_{IN}$ = 5.2V to 35V		15	40	mV
Load Regulation	Driver Current = 0 to 250mA		6.0	25	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense = 5.0V	75	125	210	µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Regulating Voltage and Error Amplifier (UC1836 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	2.47	2.5	2.53	V
	Over Temperature	2.45		2.55	V
Line Regulation	$+V_{IN}$ = 5.2V to 35V		6.0	20	mV
Load Regulation	Driver Current = 0 to 250mA		3.0	15	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense = 2.5V	−1.0	−0.2		µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Driver					
Maximum Current		250	500		mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	V
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.45V	140	250	300	µA
Driver Sink Leakage	In UVLO			10	µA
	In Reverse Voltage (UC1835 Family Only)			10	µA
Thermal Shutdown			165		°C
Foldback Current Limit					
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	A
Current Limit Amp Transconductance	±100µA at Compensation/Shutdown, V_{OUT} Sense = (0.9) V_{REG}	12	24	42	mS
Limiting Voltage at Current Limit (−) (Note 2)	V_{OUT} Sense = (0.9) V_{REG} Volts Below $+V_{IN}$, T_J = 25°C	80	100	140	mV
Sense Resistor Value (Note 3)	V_{OUT} Sense = (0.9) V_{REG} I_{OUT} = 1A, T_J = 25°C		40		mΩ

Note: 2. This voltage has a positive temperature coefficient of approximately 3500ppm/°C.
3. This resistance has a positive temperature coefficient of approximately 3500ppm/°C. The total resistance from Pin 1 to Pin 8 will include an additional 60 to 100mΩ of package resistance.

UC3835/36 Typical Applications

See appendix for component selection

LOW CURRENT APPLICATION
using the UC3836 internal drive transistor

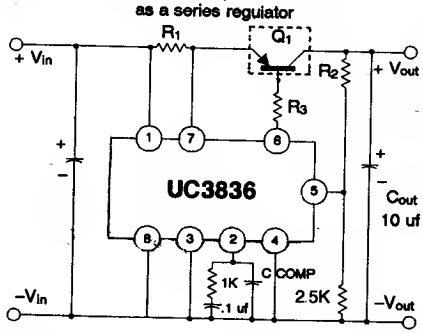


TYPICAL OUTPUT CURRENT vs. V_{in} and V_{out}
of the UC3836 internal drive transistor
for P_{diss} = 0.5 W (approx.)

		V_{in}					
	Volts	5	9	12	15	18	24
V_{out}	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

Fig. 3

LINEAR REGULATOR
using an external power transistor
as a series regulator



P CHANNEL POWER MOSFETs
can also be used as the series pass transistor Q_1

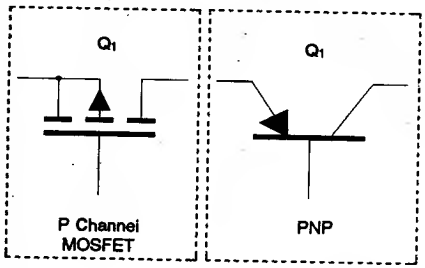
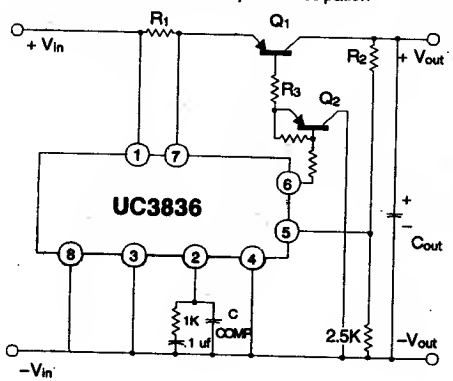


Fig. 4

HIGH CURRENT APPLICATION
using drive transistor Q_2 to increase Q_1 base drive
and reduce UC3836 power dissipation



PARALLEL PASS TRANSISTORS
can be added for high current
or high power dissipation applications

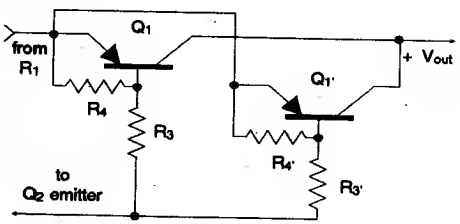


Fig.5

Design Equations and Component Selection

R_1 - Current Sense Resistor

$R_1 = 0.100\ V/I_{OUT}$ (max)

LOW CURRENT	
I_{OUT} mA	R_1 ohms
10	10
20	5
30	3.3
40	2.5
50	2.0
60	1.7
70	1.4
80	1.2
90	1.1

GENERAL USE	
I_{OUT} A	R_1 ohms
0.10	1.0
0.25	0.40
0.50	0.20
0.75	0.13
1.0	0.10
2.0	0.050
3.0	0.033
4.0	0.025
5.0	0.020

HIGH CURRENT	
I_{OUT} A	R_1 mohm
5	20
6	16.7
7	14.3
8	12.5
9	11.1
10	10.0
15	6.0
20	5.0
25	4.0

R_2 - Output Voltage Divider Resistor

$R_2 = (V_{OUT} - 2.5V/1mA)$

FIXED	
V_{OUT}	R_2
5.0	2.5K
9.0	6.5K
12.0	7.5K
15.0	12.5K
18.0	15.5K
24.0	21.5K

ADJUSTABLE	
$V_{OUT(MAX)}$	R_2
7.5V	5K POT
12.5V	10K POT
22.5V	20K POT

R_3 - Drive Current Limit Resistor

$R_3 = ((V_{in} - V_{BE} - V_{sat})*Beta\ (min))/I_{OUT}$ (max)

I_{OUT} A	V_{in} 9V	V_{in} 15V	V_{in} 24V
0.10	1.8K	3.2K	5.6K
0.25	680	1.2K	2.2K
0.50	330	650	1.1K
0.75	220	430	750
1.0	180	330	560
2.0	82	160	270
3.0	57	100	180
4.0	43	82	120

For circuit diagram of Fig. 4,
Beta (min) = 25, V_{BE} = 0.7V, V_{SAT} = 1.5V

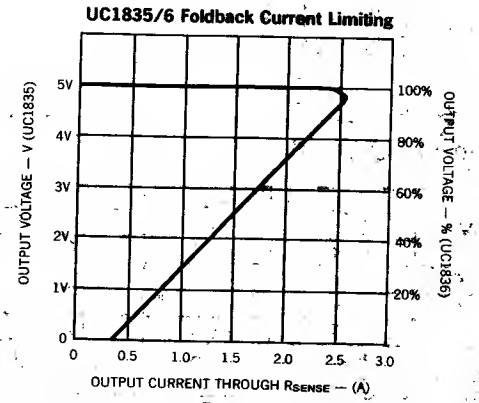
I_{OUT} A	V_{in} 9V	V_{in} 15V	V_{in} 24V
1.0	200	350	560
2.0	100	175	270
4.0	50	87	140
5.0	40	70	110
7.5	27	47	75
10.0	20	35	57
15.0	13	24	38
20.0	10	17	27

For circuit diagram of Fig. 5,
Beta (min) = 25, V_{BE} = 0.7V,
$V_{SAT} \approx V_{BE}(Q_2) + V_{SAT}$ (UC3836) $\approx$ 1.5V

Q1 - Pass Transistor

I_{OUT} A	PNP Transistor	P Channel MOSFET	N Channel MOSFET
< 1.0	TIP30 D41D4	IRF9511 RFP5P12	IRF511
2.5	TIP32,34 D45C2	IRF9521 RFP6P08	IRF521
5.0	D45H5,8 MJE6040	IRF9531 RFP12P08	IRF531 IRFZ10
7.5	TIP36 2N6666*	IRF9541	IRF541 IRFZ20
10.0	TIP36,145* 2N6648*	IRF9541 RFK25P08	IRF540 IRFZ20
15.0		IRF9Z30 RFK25P08	IRFZ30
20.0	2N6285*	RFK25P08	IRFZ40

* Darlington transistor



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INTEGRATED CIRCUITS

UNITRODE

Magnetic Amplifier Controller

UC1838A
UC2838A
UC3838A

4

FEATURES

- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with -120V Capability
- 5V to 40V Analog Operation
- 5W DIL Package

DESCRIPTION

The UC1838A family of magnetic amplifier controllers ontains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source will provide the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2A to 20A.

By controlling the reset current to a magnetic amplifier, this device will define the amount of volt-seconds the magnetic amplifier will block before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width-modulated input voltage, a magnetic amplifier will block a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC 1838A, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

The UC1838A contains a precision 2.5V reference, two uncommitted high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of magnetic amplifier reset current and with -120 volt capability.

These devices are available in a plastic "bat-wing" DIP for operation over a -20°C to +85°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation.

This improved "A" version replaces the non "A" version formerly introduced.

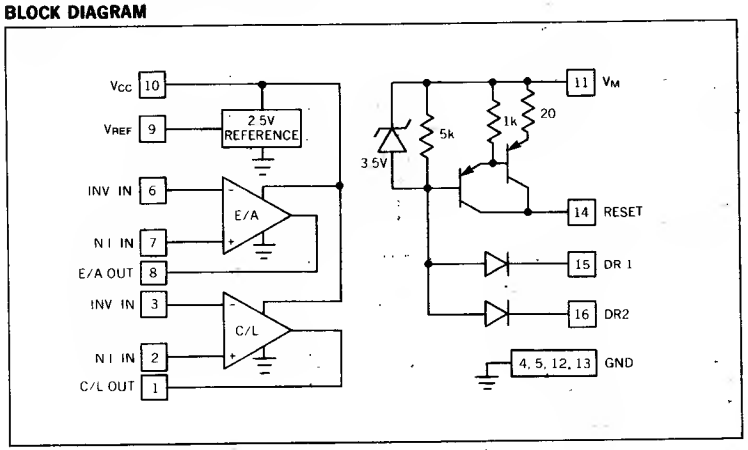
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	40V
Magnetic Amp. Source Voltage, V_M	40V
Reset Output Voltage, V_R	-120V
Total Current Source Voltage, $V_M - V_R$	-140V
Amplifier Input Range	-.3V to V_{CC}
Reset Input Current, I_{DR}	-10mA

	Plastic	Cerdip
Power Dissipation at T_A = 25°C	2W	1W
Derate Above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (leads/case) = 25°C	5W	2W
Derate for Ground Lead Temperature Above 70°C	70mW/°C	—
Derate for Case Temperature Above 25°C	—	16mW/°C
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

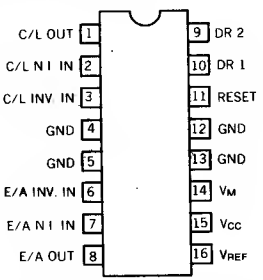
NOTE: All voltages are with respect to ground pins.
All currents are positive into the specified terminal.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



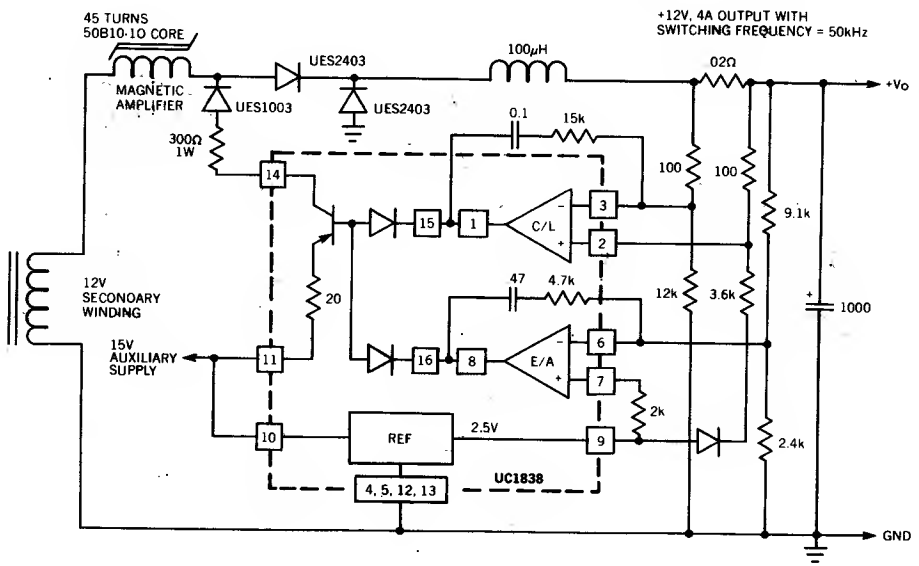
NOTE: All four ground pins must be connected to a common ground.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1838A -20°C to +85°C for the UC2838A and 0°C to +70°C for the UC3838A, V_{CC} = 20V, V_M = 5V.) T_A=T_J

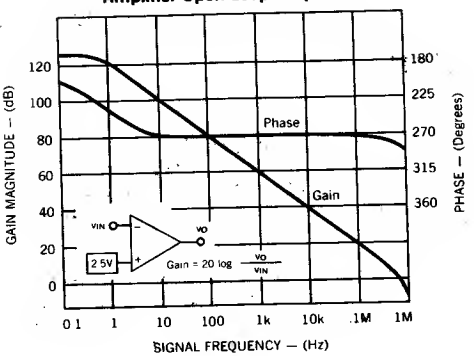
PARAMETER	TEST CONDITIONS	UC1838A/UC2838A			UC3838A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Supply Current	V_{CC} = V_M = 40V	—	4	8	—	4	8	mA
Reference Output	T_A = 25°C	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	V_{CC} = 5 to 30V	—	1	5	—	1	10	mV
Load Regulation	I_O = 0 to -2mA	—	5	20	—	5	20	mV
Short Circuit Current	V_{REF} = 0V	—	-30	-60	—	-30	-60	mA
Temperature Stability*	Over Operating Temp. Range	—	15	25	—	10	25	mV
Amplifier Section (Each Amplifier)								
Offset Voltage	V_{CM} = 2.5V	—	—	5	—	—	10	mV
Input Bias Current	V_{IN} = 0V	—	—	-1	—	—	-1	μA
Input Offset Current		—	—	100	—	—	100	nA
Minimum Output Swing		0.4	—	18	0.4	—	18	V
Output Sink Current	V_O = 5V	1	10	30	1	10	30	mA
Output Source Current	V_O = 0V	-1	-10	-20	-1	-10	-20	mA
A_{VOL}	V_O = 1 to 11V	100	120	—	100	120	—	dB
CMRR	V_{IN} = 1 to 11V	70	80	—	70	80	—	dB
PSRR	V_{CC} = 10 to 20V	70	100	—	70	100	—	dB
Gain Bandwidth*		0.6	0.8	—	0.6	0.8	—	MHz
Reset Drive Section								
Input Leakage	V_{DR} = 40V	—	—	10	—	—	10	μA
Output Leakage	V_R = -120V	—	—	-100	—	—	-100	μA
Input Current	I_R = -50mA	—	-1	-2	—	-1	-2	mA
Maximum Reset Current	I_{DR} = -3mA	-100	-120	-200	-100	-120	-200	mA
Transconductance	I_R = -10 to -50mA	.03	.042	.055	.03	.042	.055	A/V

Note: *These parameters guaranteed by design and not 100% tested in production.

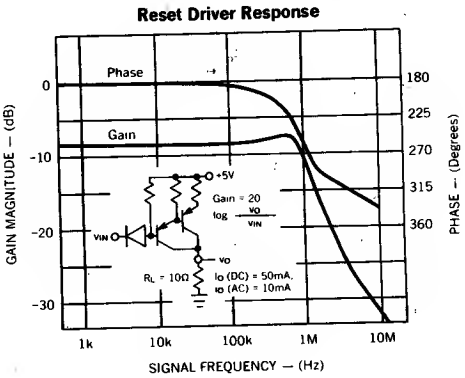
TYPICAL APPLICATION



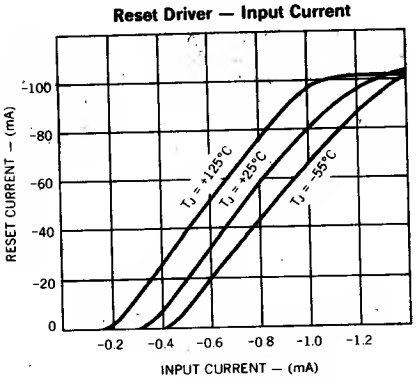
Amplifier Open-Loop Response



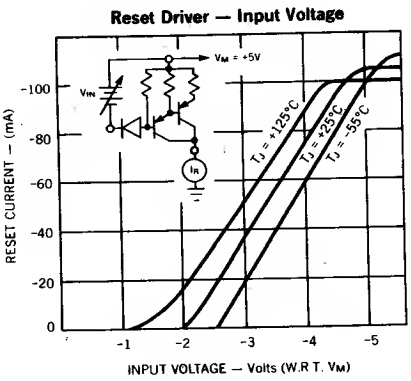
Reset Driver Response



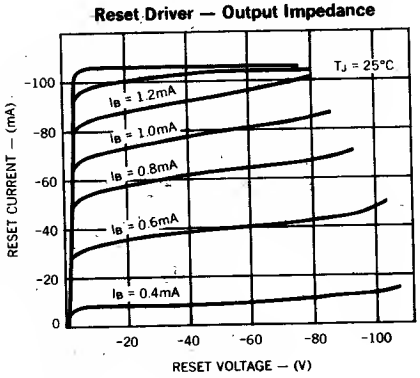
Reset Driver — Input Current



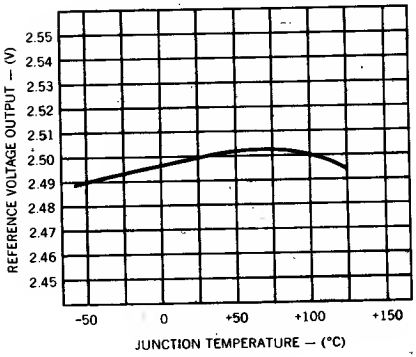
Reset Driver — Input Voltage



Reset Driver — Output Impedance



Reference Temperature Coefficient



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INTEGRATED CIRCUITS

UNITRODE

Programmable, Off-Line, PWM Controller

UC1840
UC2840
UC3840

FEATURES

- All control, driving, monitoring, and protection functions included
- Low-current, off-line start circuit
- Feed-forward line regulation over 4 to 1 input range
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- No start-up or shutdown transients
- Slow turn-on and maximum duty-cycle clamp
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- Remote, pulse-commandable start/stop
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 18-pin DIL package

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

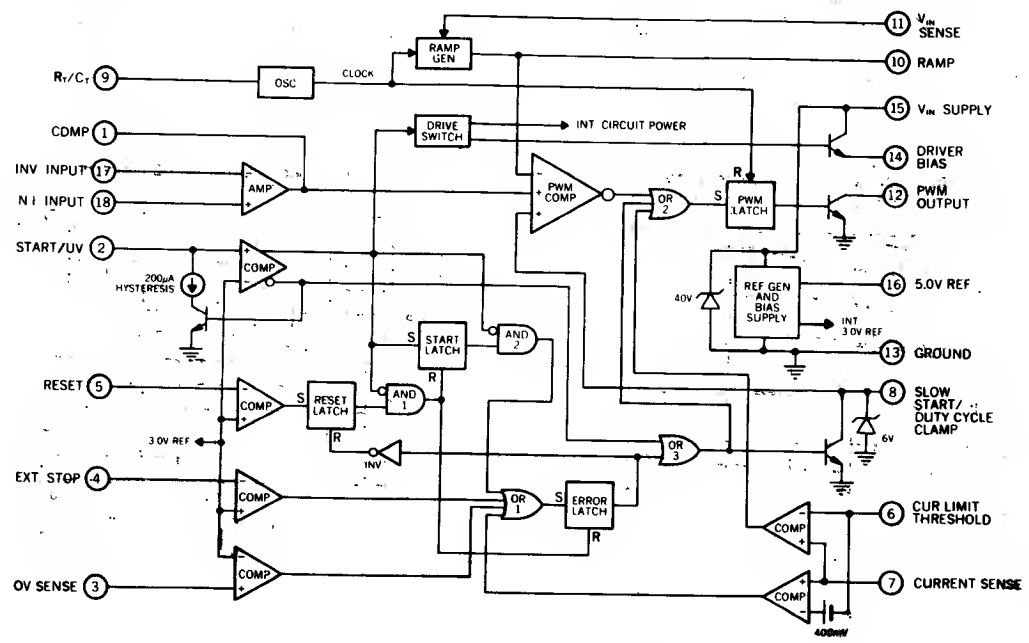
In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn-off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of −55°C to +125°C. The UC2840 and UC3840 are designed for operation from −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



Note: Positive true logic, latch outputs high with set, reset has priority.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, $+V_{IN}$ (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Comparator Inputs (Pins 2, 3, 4, 5, 17, 18) ..... -0.3 to +32V
Power Dissipation at T_A = 25°C 1000mW
- Derate at 10 mW/°C for T_A above 50°C

Power Dissipation at T_C = 25°C 2000mW
- Derate at 16 mW/°C for T_C above 25°C

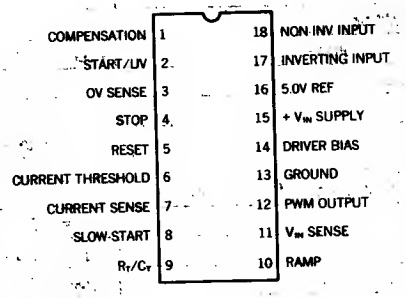
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

Notes: 1. All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE

UC1840
UC2840
UC3840



4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1840, -25°C to +85°C for the UC2840, and 0°C to 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V, T_J = 25°C		4	5.5		4	5.5	mA
Start-Up Current T.C.*	V_{IN} = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
Temperature Coefficient*	Over operating temperature range			±0.4			±0.4	mV/°C
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient*	Over operating temperature range			±.08			±.08	%/°C
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

*Guaranteed by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1840, −25°C to +85°C for the UC2840, and 0°C to 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1840 UC2840			UC3840			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak − 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80	80	dB
Short Circuit Current	V_{COMP} = 0V		−4	−10		−4	−10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak < 4.2V	5		95	5		95	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
Output Saturation	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	μA
Comparator Delay*	Pin 8 to Pin 12 T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		−1.0	−3.0		−1.0	−3.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V, T_J = 25°C	180	200	220	170	200	230	μA
Input Leakage	Input V = 20V		0.1	10		0.1	10	μA
Driver Bias Saturation Voltage, $V_{IN} - V_{OH}$	I_B = −50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		−0.1	−10		−0.1	−10	μA
Slow-Start Saturation	I_S = 2mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		−2	−5		−2	−5	μA
Common Mode Range*		−0.4		3.0	−0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

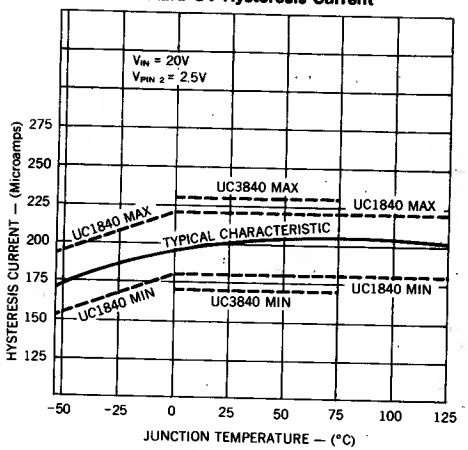
*Guaranteed by design. Not 100% tested in production.

FUNCTIONAL DESCRIPTION

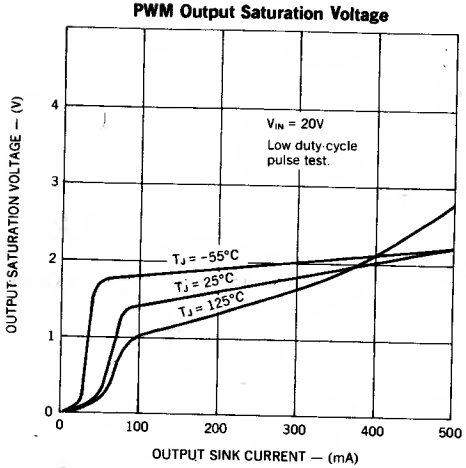
PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency $= \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	This comparator performs three functions— With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200μA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
5. Start Latch:	Keeps low input voltage at initial turn-on from being defined as a UV fault. Sets at start level to monitor for UV fault.
6. Reset Latch:	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the UV low threshold, allowing a restart.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold. Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.

4

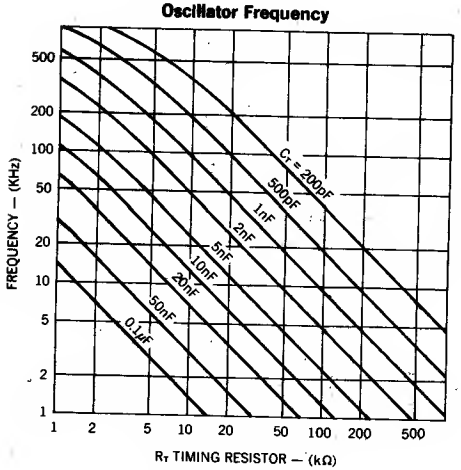
Start/UV Hysteresis Current



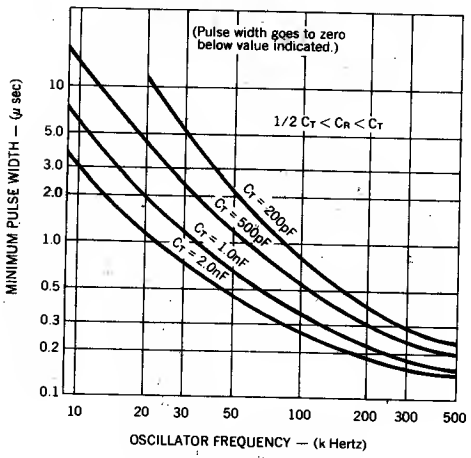
PWM Output Saturation Voltage



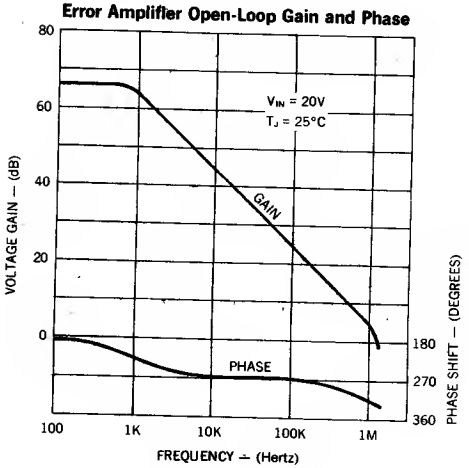
Oscillator Frequency



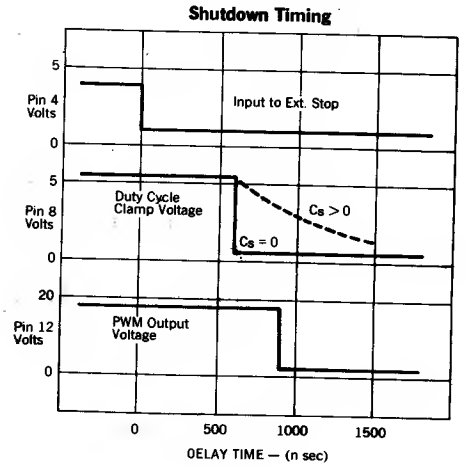
PWM Output Minimum Pulse Width



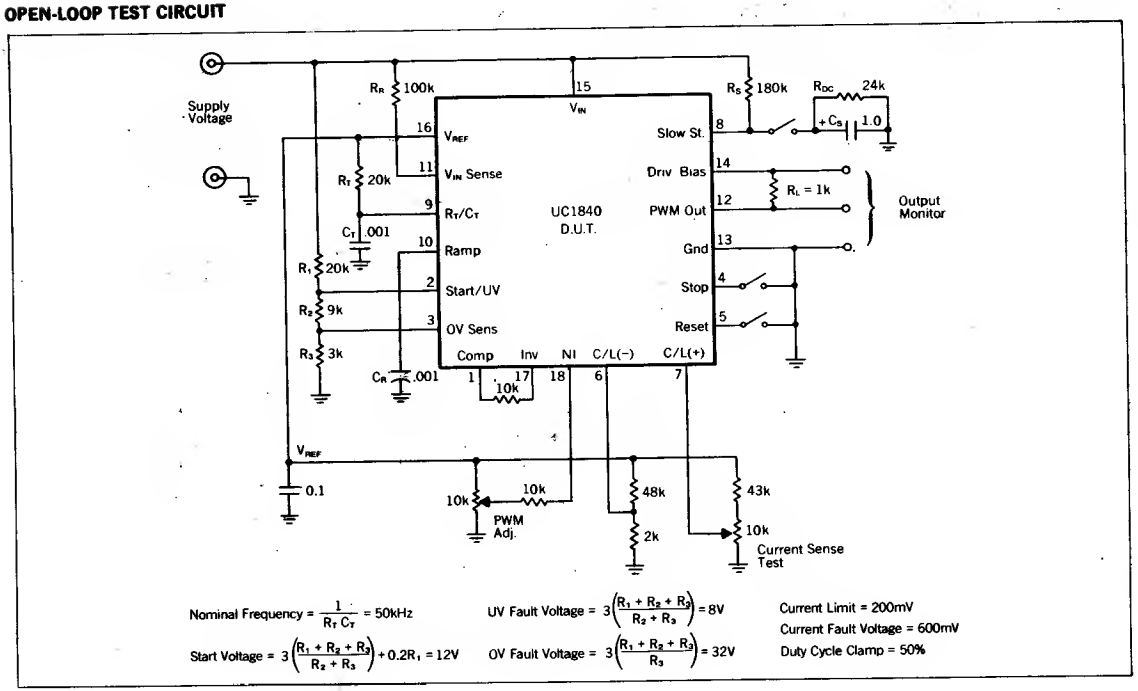
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



OPEN-LOOP TEST CIRCUIT



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line regulation.

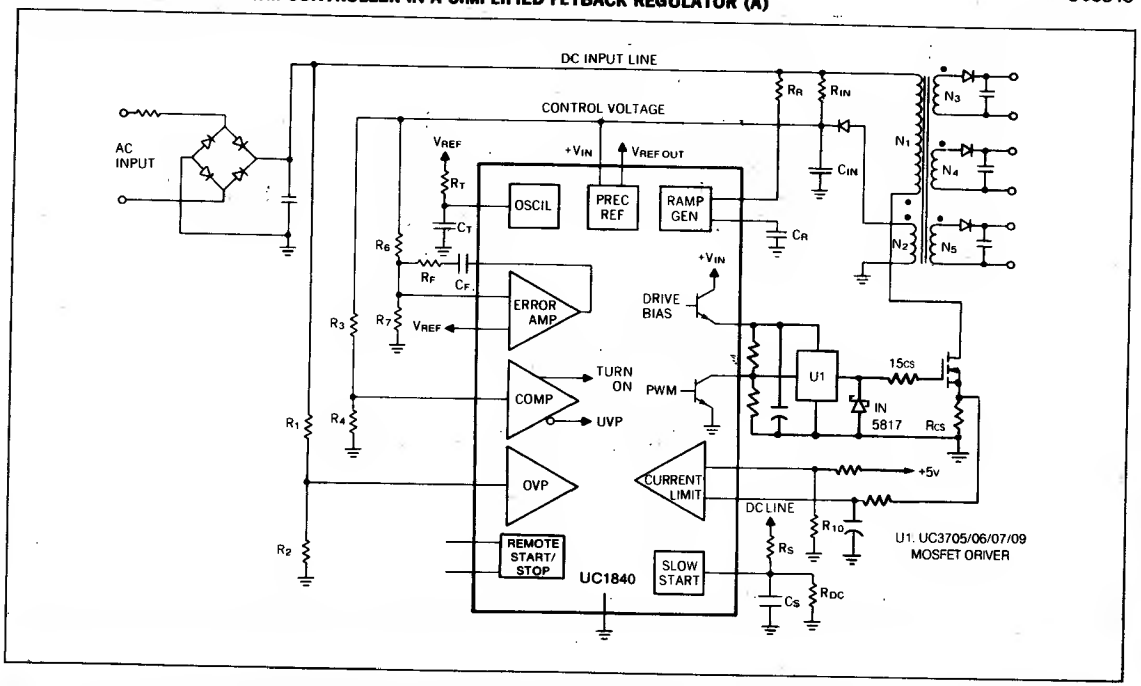
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output. The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

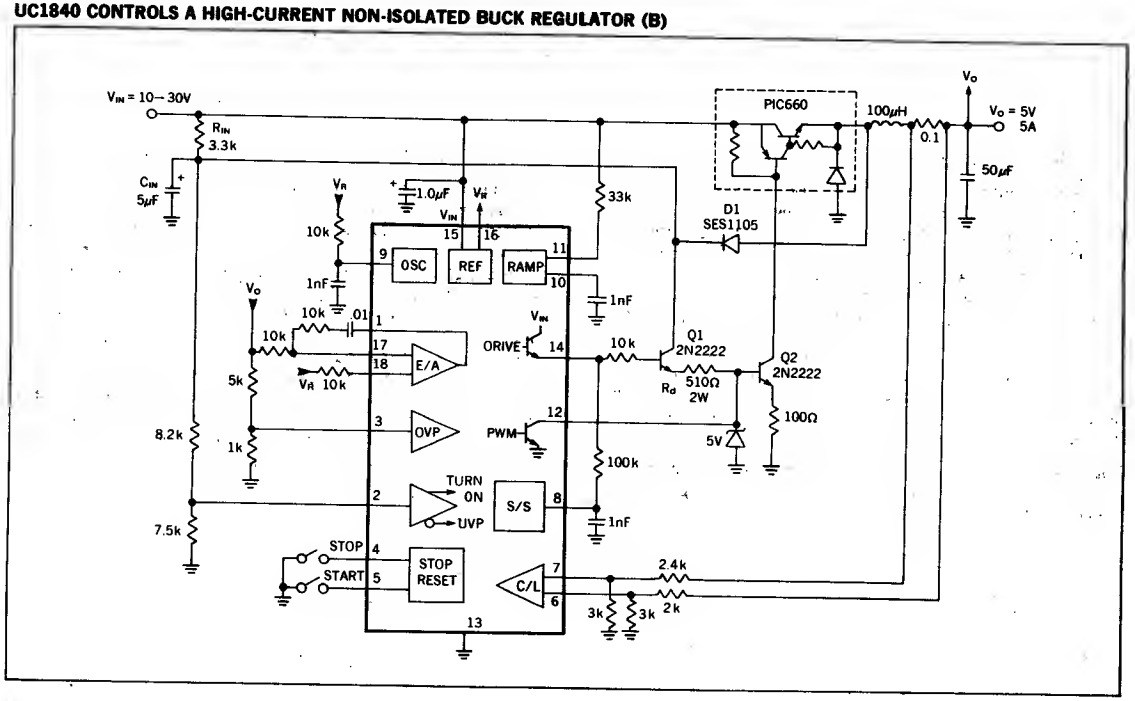
REGULATOR APPLICATION (B)

Although primarily intended for transformer-coupled power systems, the UC1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the UC1840 requires recycling the voltage sensed by the Start/UV Comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown in Figure B (next page). In this simple, non-isolated, buck regulator; diode D1 provides a low-impedence bootstrapped drive power source after start-up is achieved through R_{IN} and C_{IN}. When a fault shutdown terminates switching action, the loading of Q1 and R_d will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

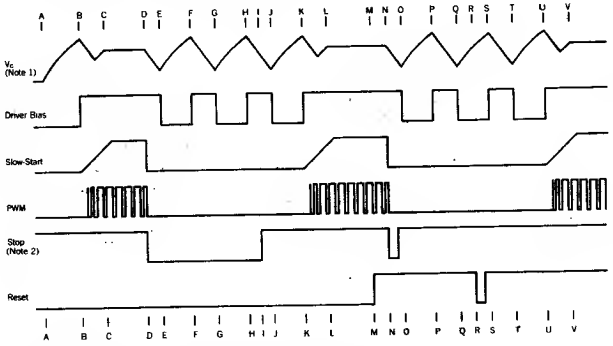
UC1840 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR (A)



UC1840 CONTROLS A HIGH-CURRENT NON-ISOLATED BUCK REGULATOR (B)



UC1840 POWER SEQUENCING FUNCTIONS



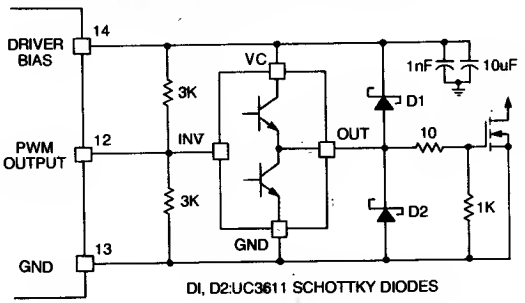
TIME	EVENT
A	Initial turn-on, V_C rises with light load
B	Start threshold. Driver Bias loads V_C
C	Operating PWM regulates V_C
D	Stop input sets Error Latch turning off PWM
E	UV low threshold, Error Latch remains set
F	Start turns on Driver Bias but Error Latch still set
G, H	V_C and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
D	Error Latch does not reset as Reset Latch is reset
P, Q	V_C and Driver Bias recycle with no turn-on.
R	Reset Latch set is set with momentary Reset signal
S	V_C must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

Notes:

1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, V_{IN}, for the UC1840.
2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

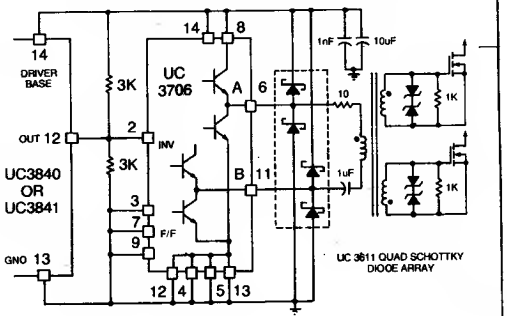
4

POWER MOSFET DRIVE CIRCUIT
USING UC 3705/3706/3707 or 3709 DRIVERS



DI, D2:UC3611 SCHOTTKY DIODES

UC 3706 CONVERTS SINGLE OUTPUT PWMS TO
HIGH CURRENT PUSH-PULL CONFIGURATION



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INTEGRATED CIRCUITS

UNITRODE

Programmable, Off-Line, PWM Controller

UC1841
UC2841
UC3841

FEATURES

- All control, driving, monitoring, and protection functions included
- Low-current, off-line start circuit
- Voltage feed forward or current mode control
- Guaranteed duty cycle clamp
- PWM latch for single pulse per period
- Pulse-by-pulse current limiting plus shutdown for over-current fault
- No start-up or shutdown transients
- Slow turn-on both initially and after fault shutdown
- Shutdown upon over- or under-voltage sensing
- Latch off or continuous retry after fault
- PWM output switch usable to 1A peak current
- 1% reference accuracy
- 500kHz operation
- 18-pin DIL package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

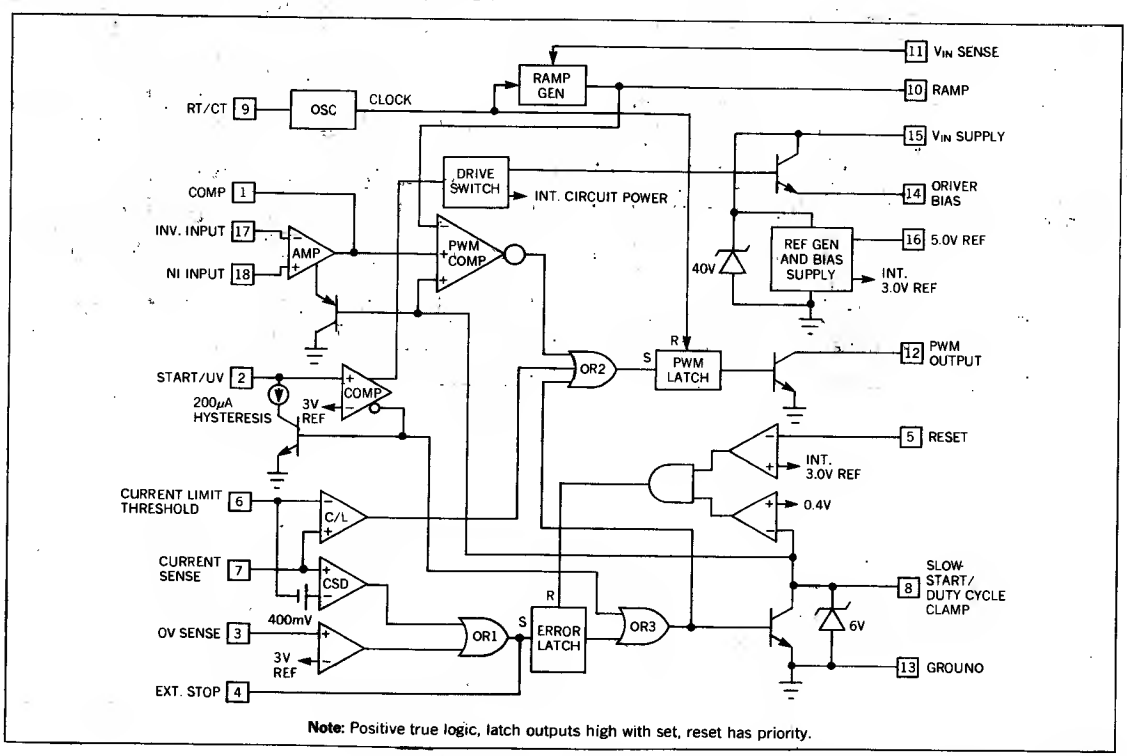
In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages with the UC1841 characterized for −55°C to +125°C operation while the UC2841 and UC3841 are designed for −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM (Pin numbers shown for DIL-18 package)



Note: Positive true logic, latch outputs high with set, reset has priority.

ABSOLUTE MAXIMUM RATINGS (Note 1)

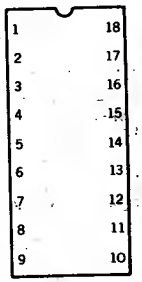
Supply Voltage, $+V_{IN}$ (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... −200mA
Reference Output Current (Pin 16) ..... −50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... −0.5 to +5.5V
Stop Input (Pin 4) ..... −0.3 to +5.5V
Comparator Inputs
(Pins 1, 7, 9-11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

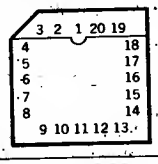
Notes: 1. All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.
2. All pin numbers are referenced to DIL-18 package.

CONNECTION DIAGRAMS

TOP VIEWS
DIL-18, J or N PACKAGE



PLCC-20
Q PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DIL	PLCC
COMP	1	1
START/UV	2	2
OV SENSE	3	3
STOP	4	4
RESET	5	3
CUR THRESH	6	7
CUR SENSE	7	8
SLOW START	8	9
RT/CT	9	10
RAMP	10	11
V_{IN} SENSE	11	12
PWM OUT	12	13
GROUND	13	14
DRIV BIAS	14	15
+V_{IN} SUPPLY	15	17
5.0V REF	16	18
INV INPUT	17	19
N.I. INPUT	18	20

4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1841, −25°C to +85°C for the UC2841, and 0°C to 70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1841 UC2841			UC3841			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V,		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		10	14		10	14	mA
Supply OV Clamp	V_{IN} = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over operating temperature range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		−80	−100		−80	−100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over operating temperature range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = −10μA		−11	−14		−11	−14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	−0.9	−.95		−0.9	−.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1841, −25°C to +85°C for the UC2841, and 0°C to 70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1841 UC2841			UC3841			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak − 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		−4	−10		−4	−10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak < 4.2V	4		95	4		95	%
50% Duty Cycle Clamp	R_{SENSE} to V_{REF} = 10k	42	47	52	42	47	52	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
Output Saturation	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	μA
Comparator Delay*	Pin 8 to Pin 12 T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		−1.0	−4.0		−1.0	−4.0	μA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V,	170	200	220	170	200	230	μA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		−120	−200		−120	−200	μA
Driver Bias Saturation Voltage, V_{IN} − V_{OH}	I_B = −50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		−0.1	−10		−0.1	−10	μA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		−2	−5		−2	−5	μA
Common Mode Range*		−0.4		3.0	−0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

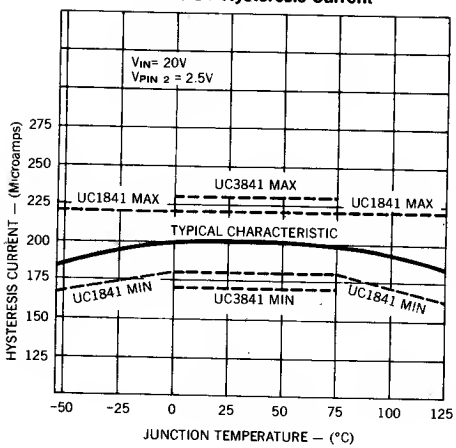
*Guaranteed by design. Not 100% tested in production.

FUNCTIONAL DESCRIPTION

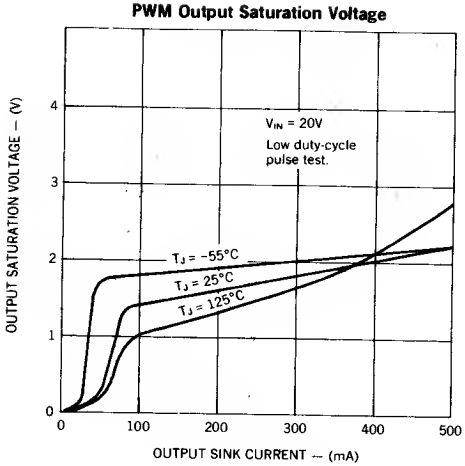
PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop-gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200μA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2 V (Typically 3 V) b. Stop > 2.4 V (Typically 1.6V) c. Current Sense 400mV over threshold. Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8 V. With Pin 5 > 3.2 V. Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (Typical) above threshold, a shutdown signal is sent to Error Latch.
3. Ext. Stop:	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical delay of 13ms/μF.

4

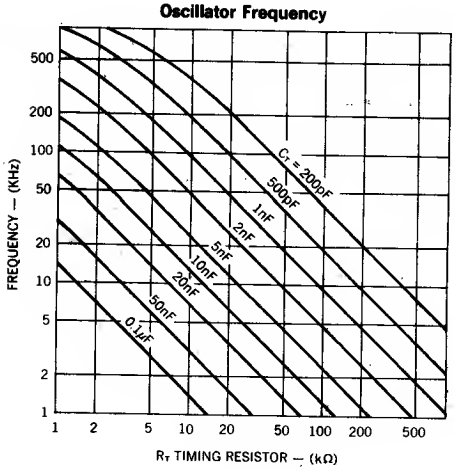
Start/UV Hysteresis Current



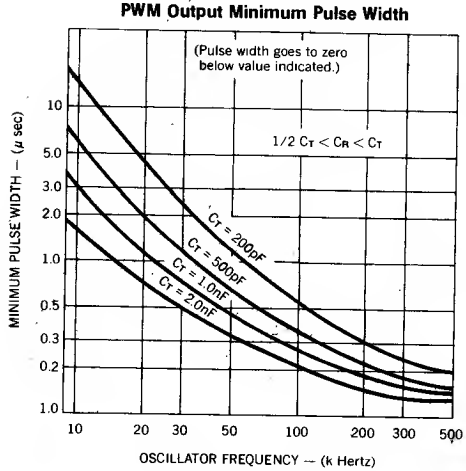
PWM Output Saturation Voltage



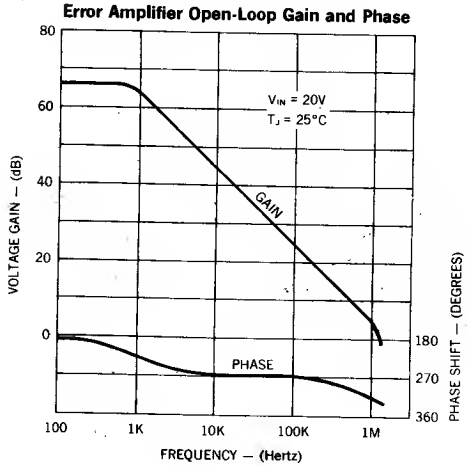
Oscillator Frequency



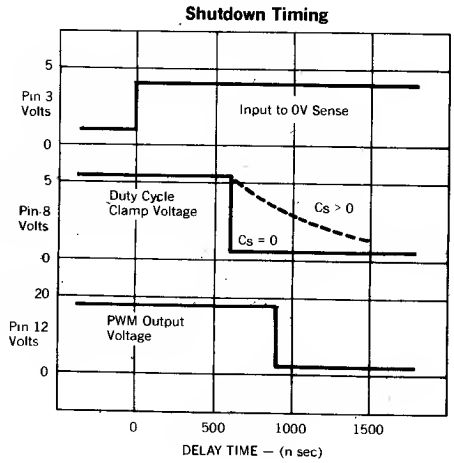
PWM Output Minimum Pulse Width



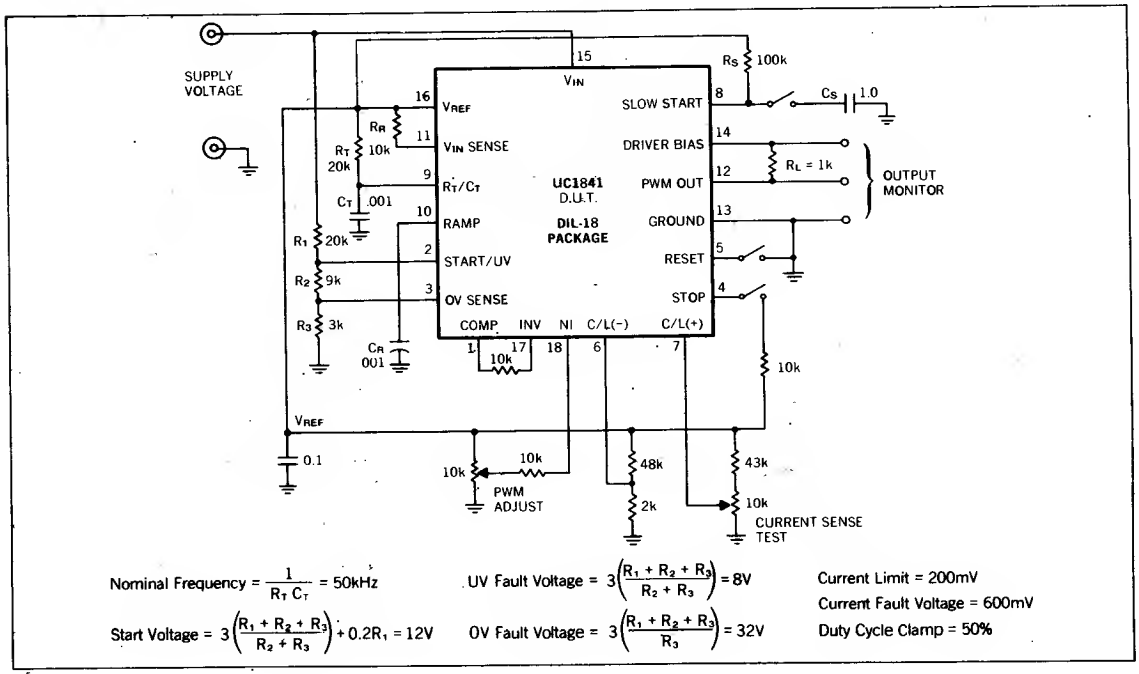
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



OPEN-LOOP TEST CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50kHz

UV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right)$ = 8V

Current Limit = 200mV

Current Fault Voltage = 600mV

Start Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right) + 0.2R_1$ = 12V

OV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_3}\right)$ = 32V

Duty Cycle Clamp = 50%

FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1841's feed-forward line regulation.

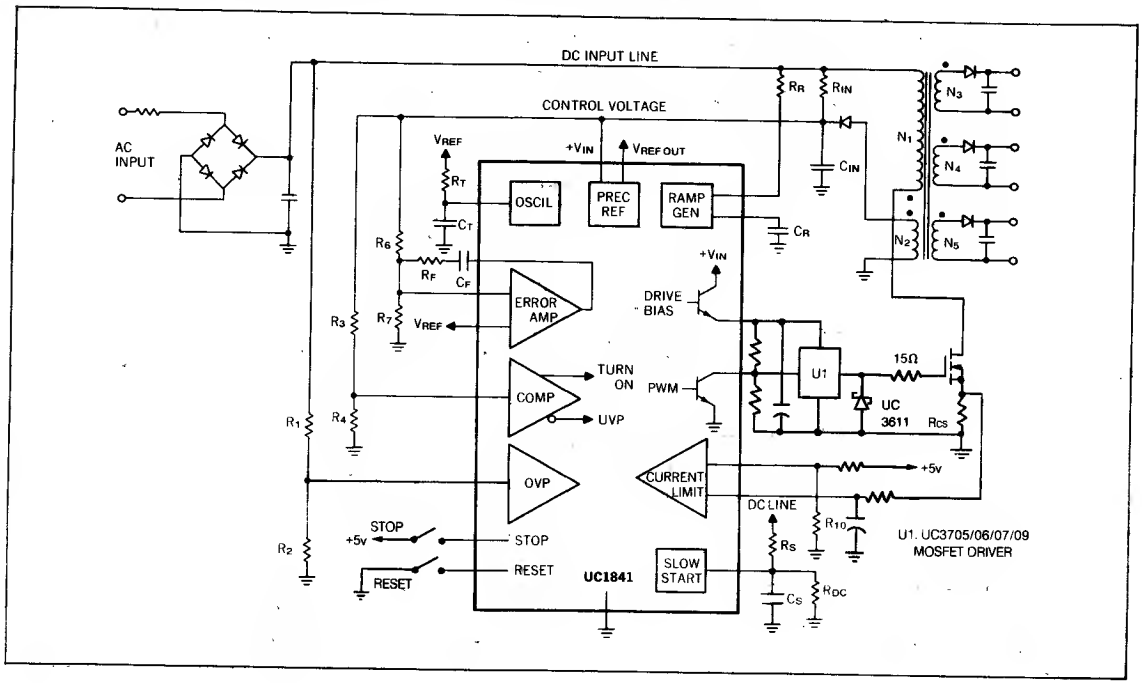
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

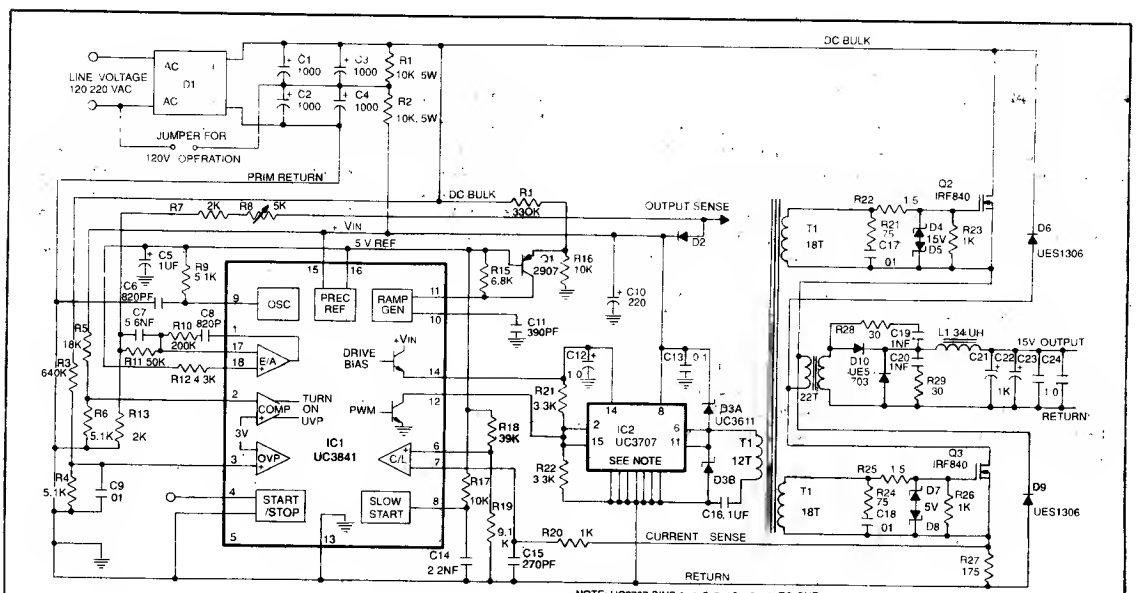
Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to work with high input line voltages — in this case, up to 60V — with internal protective clamping.

UC1841 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR (A)

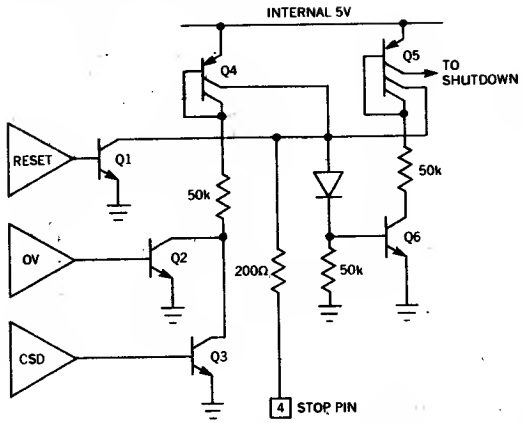




Overall schematic for a 300 watt, off-line power converter using the UC 3841 for control

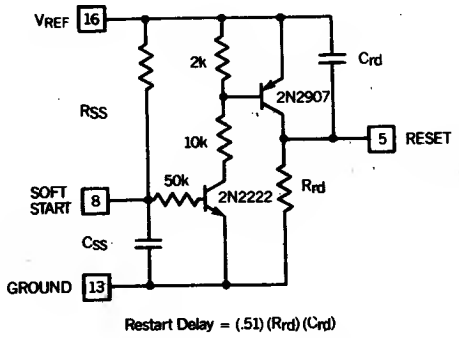
SEE APPLICATION NOTE U-114 FOR COMPLETE CIRCUIT

ERROR LATCH INTERNAL CIRCUITRY

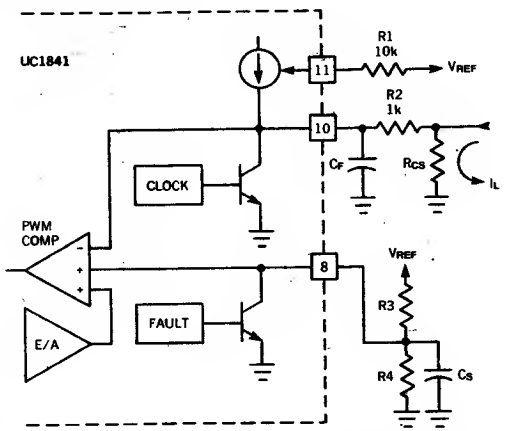


The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the ≈ 100μA collector current from Q4.

PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT

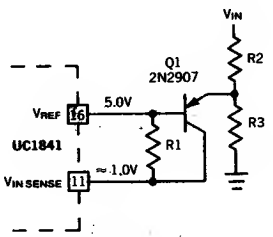


CURRENT MODE CONTROL



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through R_{CS}. Resistor R1 sets a 400mV offset across R2 (assuming $R2 \gg R_{CS}$) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with C_F as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R1 is used in conjunction with C_R (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing V_{IN}.

The minimum ramp current is:

$$I_R\,(MIN) = \frac{V_{REF} - V_{IN\,SENSE}}{R1} \approx \frac{4V}{R1}$$

The threshold where V_{IN} begins to add extra ramp current is:

$$V_{IN} \approx 5.6V \left(\frac{R2 + R3}{R3}\right)$$

Above the threshold, the ramp current will be:

$$I_R\,(VARIAB) \approx \frac{4}{R1} + \frac{V_{IN} - 5.6}{R2} - \frac{5.6}{R3}$$

4

INTEGRATED CIRCUITS

UNITRODE

Current Mode PWM Controller

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

FEATURES

- Optimized for off-line and DC to DC converters
- Low start up current (<1mA)
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500KHz operation
- Low Ro error amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

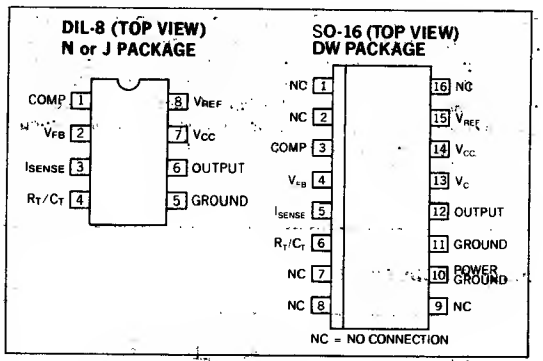
Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to < 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

ABSOLUTE MAXIMUM RATINGS (Note 1)

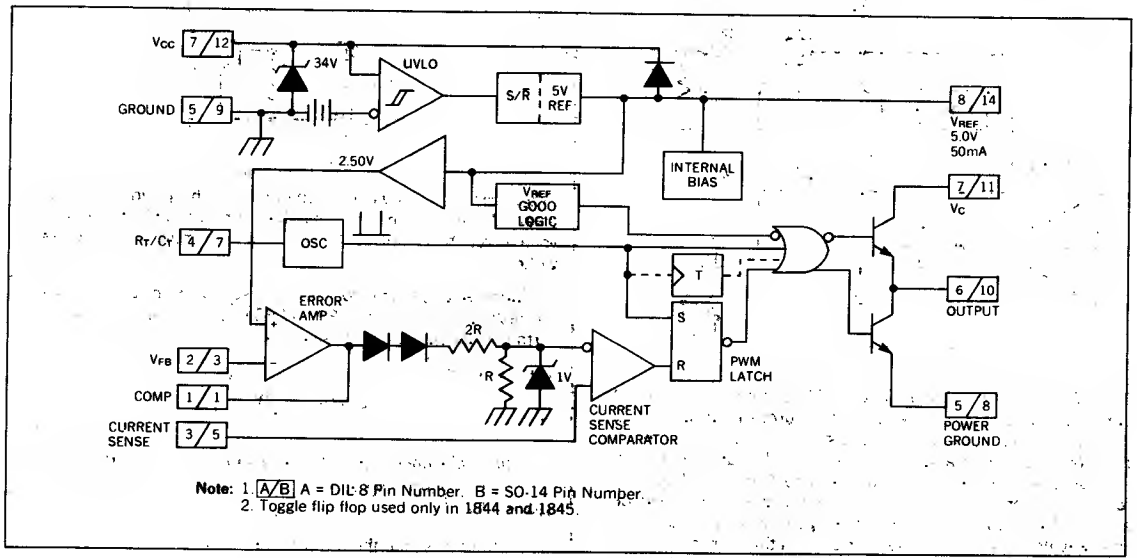
Supply Voltage (Low Impedence Source) 30V
Supply Voltage (I_{CC} < 30mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5μJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Derate 5.8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

CONNECTION DIAGRAM



BLOCK DIAGRAM



Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.

ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \le T_A \le 125°C$ for UC184X; $-25 \le T_A \le 85°C$ for UC284X; $0 \le T_A \le 70°C$ for UC384X; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \le V_{IN} \le 25V$		6	20		6	20	mV
Load Regulation	$1 \le I_O \le 20mA$		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	$10Hz \le f \le 10KHz$, T_j = 25°C (Note 2)		50			50		μV
Long Term Stability	T_A = 125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_j = 25°C (Note 6)	47	52	57	47	52	57	KHz
Voltage Stability	$12 \le V_{CC} \le 25V$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \le T_A \le T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	$2 \le V_O \le 4V$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	$12 \le V_{CC} \le 25V$	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15K to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15K to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \le V_{CC} \le 25V$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	$V_{PIN\ 3}$ = 0 to 2V		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; 0 \le V_{PIN\ 3} \le 0.8V.$$

5. Adjust V_{CC} above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ELECTRICAL SPECIFICATIONS (Unless otherwise stated, these specifications apply for $-55 \le T_A \le 125°C$ for UC184X; $-25 \le T_A \le 85°C$ for UC284X; $0 \le T_A \le 70°C$ for UC384X; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF.) $T_A = T_J$

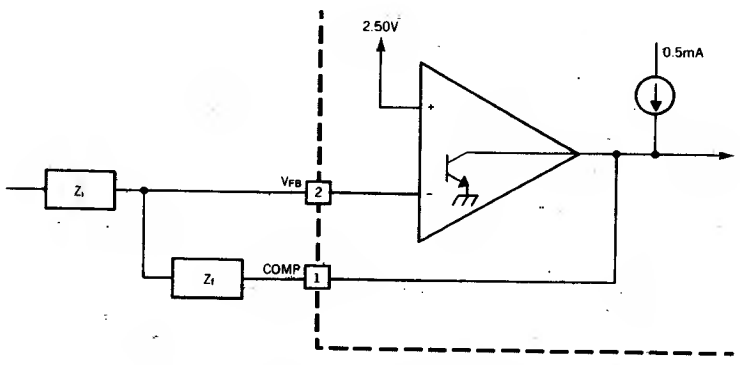
PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA		34			34		V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; 0 \le V_{PIN\ 3} \le 0.8V.$$

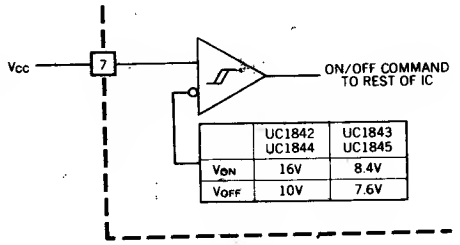
5. Adjust V_{CC} above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

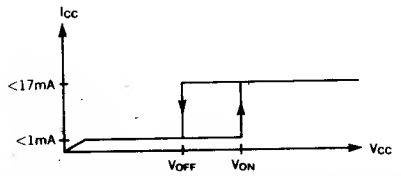


ERROR AMP CAN SOURCE OR SINK UP TO 0.5mA

UNDER-VOLTAGE LOCKOUT

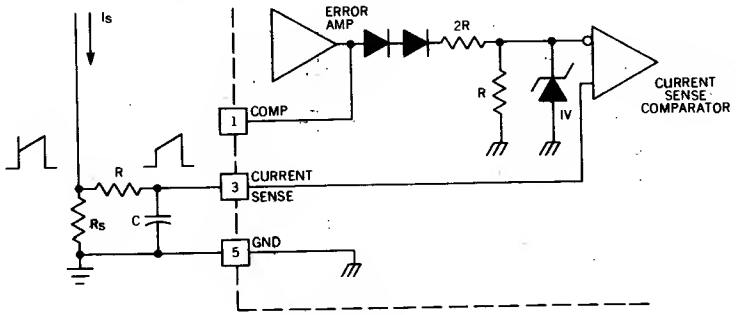


	UC1842 UC1844	UC1843 UC1845
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

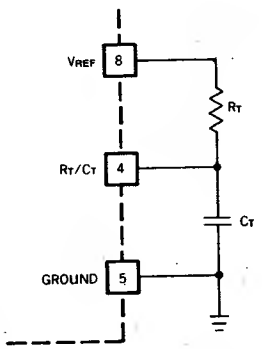


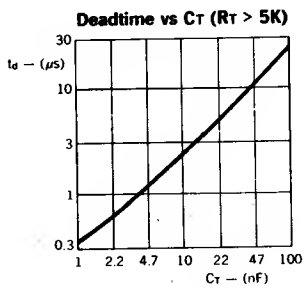
PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

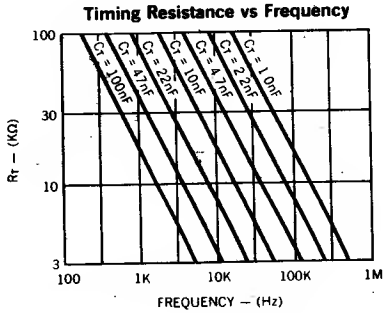
$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS

OSCILLATOR SECTION

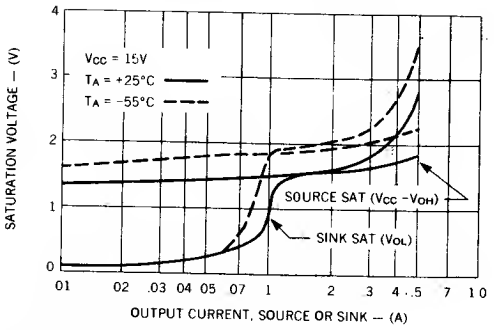




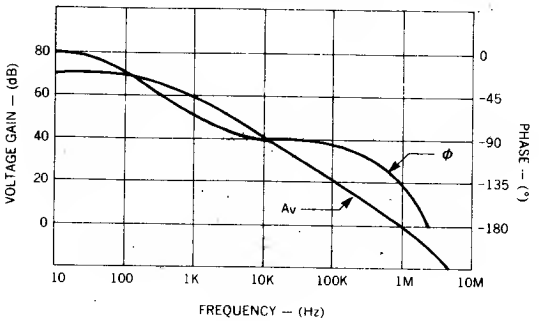


For $R_T > 5K$ $f \approx \frac{1.72}{R_T C_T}$

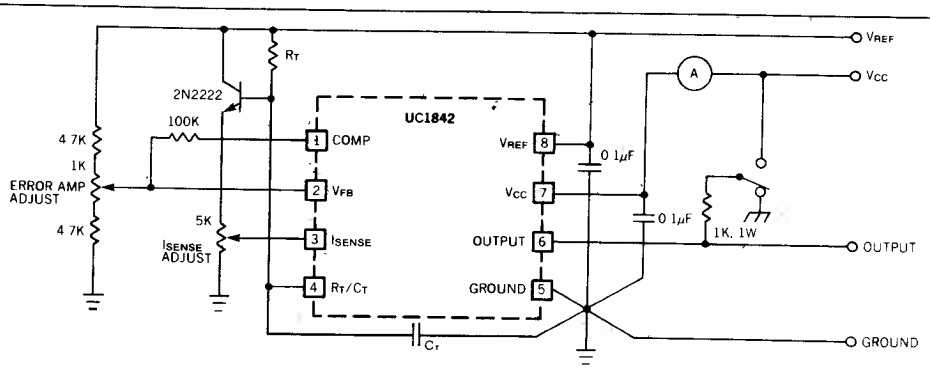
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response



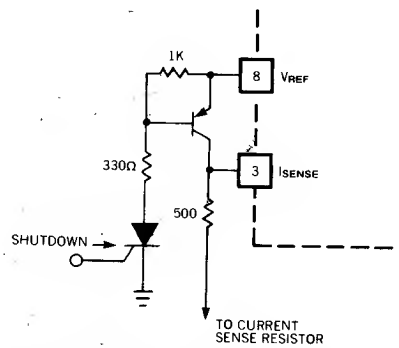
OPEN-LOOP LABORATORY TEST FIXTURE



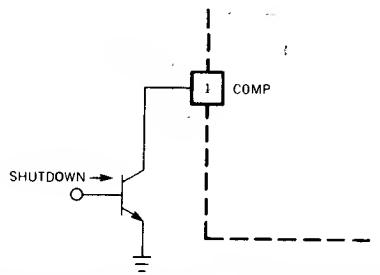
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUTDOWN TECHNIQUES

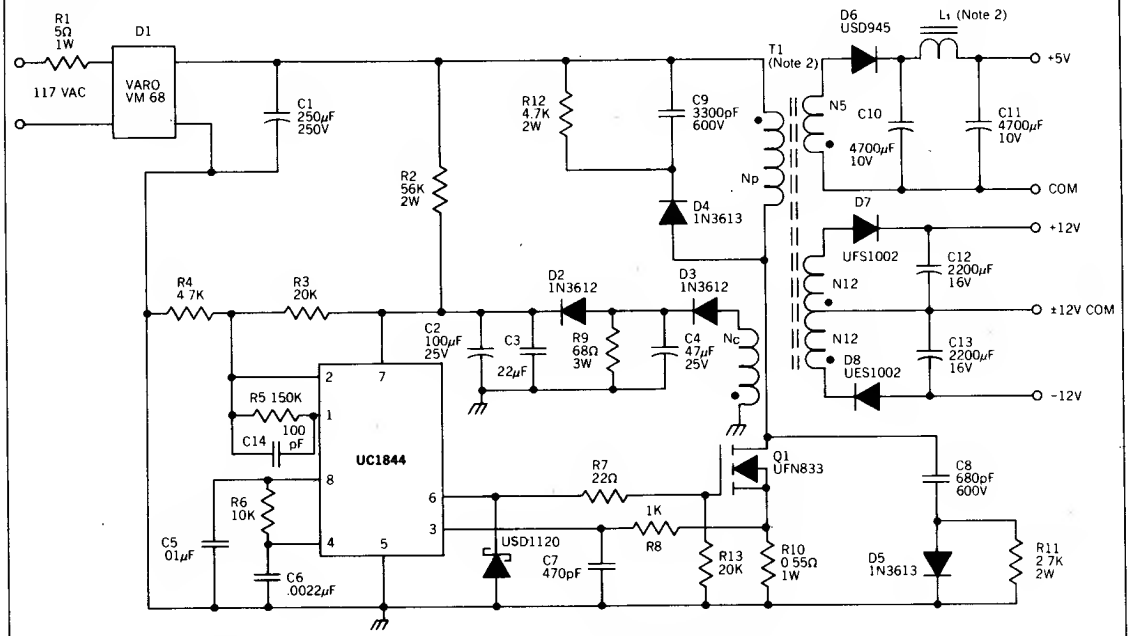


Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM



comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

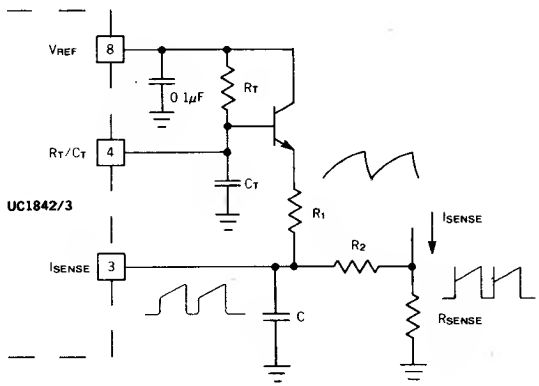
OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50mV P-P Max.
   - B. +12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.
   - C. −12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

Current Mode PWM Controller

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

FEATURES

- Optimized for off-line and DC to DC converters
- Low start up current (<0.5 mA)
- Trimmed oscillator discharge current
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500KHz operation
- Low R_O error amp

DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During under voltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

The difference between members of this family are shown in the table below.

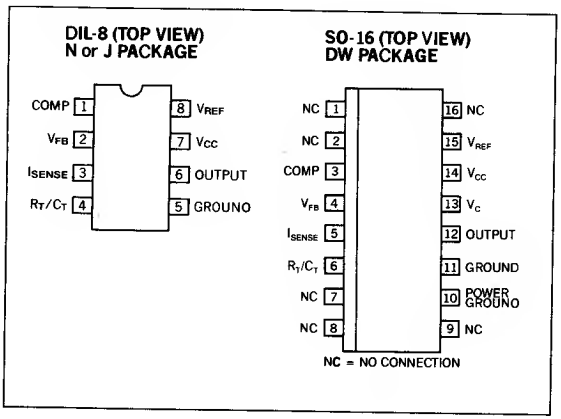
Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0 V	10.0 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16.0 V	10.0 V	<50%
UC1845A	8.5 V	7.9 V	<50%

ABSOLUTE MAXIMUM RATINGS (Note 1)

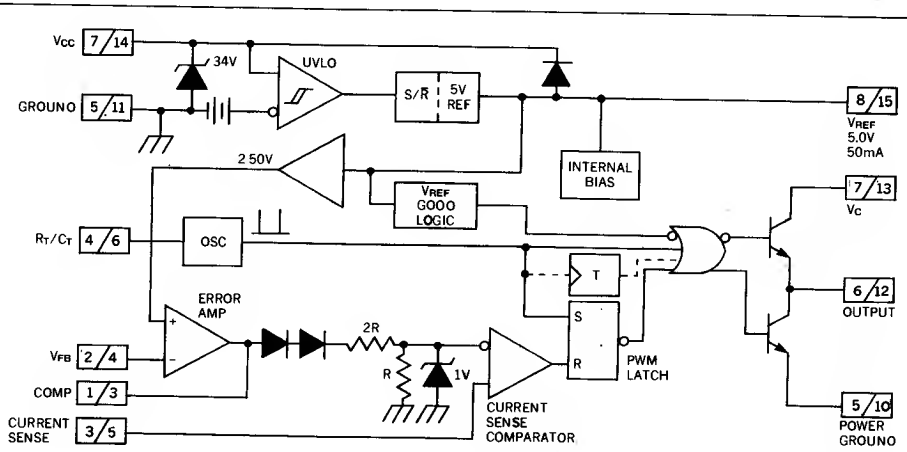
Supply Voltage (Low Impedence Source) 30V
Supply Voltage (I_{CC} < 30mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Power Dissipation at $T_A \leq 25°C$ (SO-16) 725mW
Derate 5.8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.

CONNECTION DIAGRAM



BLOCK DIAGRAM



Note: 1. A/B A = DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125°C$ for the UC184XA; $-25 \leq T_A \leq 85°C$ for the UC284XA; $0 \leq T_A \leq 70°C$ for the UC384XA; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF; $T_A = T_J$; Pin numbers refer to DIL-8.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25V$		6	20		6	20	mV
Load Regulation	$1 \leq I_O \leq 20mA$		6	25		6	25	mV
Temp. Stability	(Note 2) (Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	$10Hz \leq f \leq 10KHz$, T_j = 25°C (Note 2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		−30	−100	−180	−30	−100	−180	mA
Oscillator Section								
Initial Accuracy	T_j = 25°C (Note 6)	47	52	57	47	52	57	KHz
Voltage Stability	$12 \leq V_{CC} \leq 25V$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak		1.7			1.7		V
Discharge Current	T_j = 25°C $V_{PIN\ 4}$ = 2V	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$V_{PIN\ 4}$ = 2V	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			−0.3	−1		−0.3	−2	µA
A_{VOL}	$2 \leq V_O \leq 4V$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25V$	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	−0.5	−0.8		−0.5	−0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15K to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15K to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25V$ (Note 3)		70			70		dB
Input Bias Current			−2	−10		−2	−10	µA
Delay to Output	(Note 2) $V_{PIN\ 3}$ = 0 to 2V		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_j = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	V_{CC} = 5V I_{SINK} = 10mA		0.7	1.2		0.7	1.2	V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.

4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; \quad 0 \leq V_{PIN\ 3} \leq 0.8V.$$

5. Adjust V_{CC} above the start threshold before setting at 15V.

6. Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

7. "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{\text{Vref (max)} - \text{Vref (min)}}{\text{Tj (max)} - \text{Tj (min)}}$$

Vref (max) & Vref (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_A \leq 125°C$ for the UC184XA; $-25 \leq T_A \leq 85°C$ for the UC284XA; $0 \leq T_A \leq 70°C$ for the UC384XA; V_{CC} = 15V (Note 5); R_T = 10K; C_T = 3.3nF; $T_A = T_J$; Pin numbers refer to DIL-8.) $T_A = T_J$

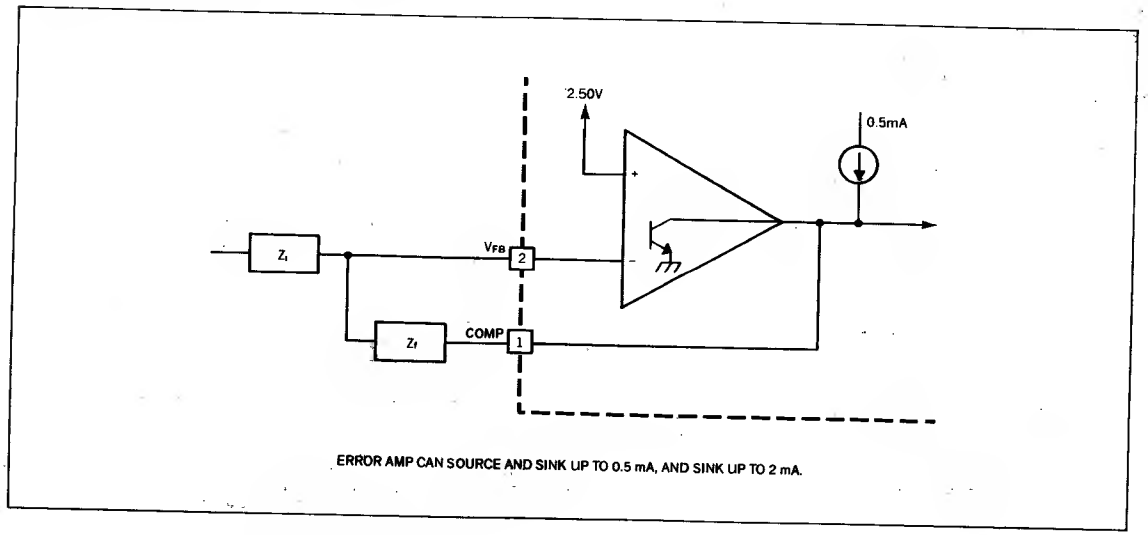
PARAMETER	TEST CONDITIONS	UC184X UC284X			UC384X			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	X842A/4A	15	16	17	14.5	16	17.5	V
	X843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842A/4A	9	10	11	8.5	10	11.5	V
	X843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842A/3A	94	96	100	94	96	100	%
	X844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3}$ = 0V		11	17		11	17	mA
Vcc Zener Voltage	I_{CC} = 25mA		34			34		V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2} = 0$.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}; \quad 0 \leq V_{PIN\ 3} \leq 0.8V.$$

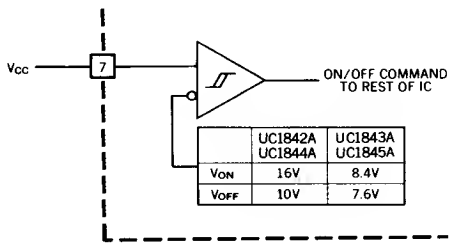
5. Adjust V_{CC} above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

ERROR AMP CONFIGURATION

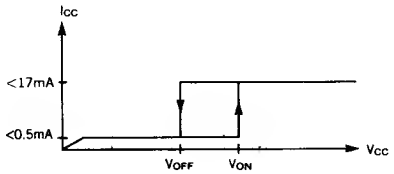


ERROR AMP CAN SOURCE AND SINK UP TO 0.5 mA, AND SINK UP TO 2 mA.

UNDER-VOLTAGE LOCKOUT

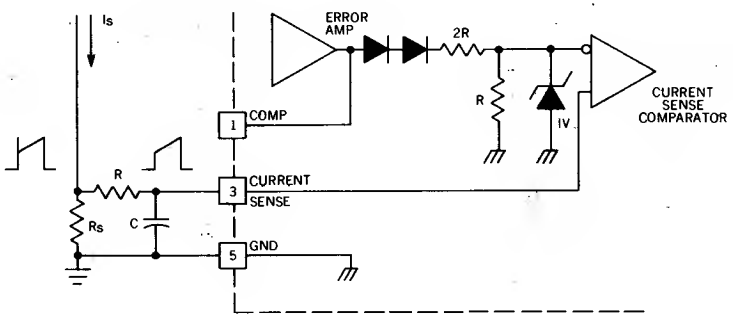


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

CURRENT SENSE CIRCUIT

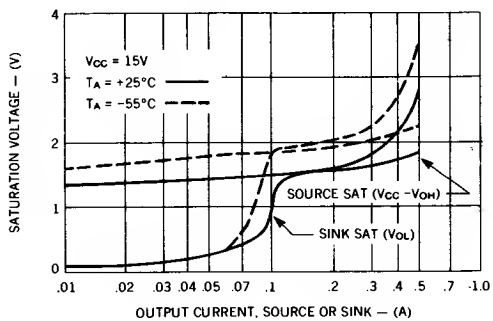


PEAK CURRENT (I_S) IS OETERMINEO BY THE FORMULA:

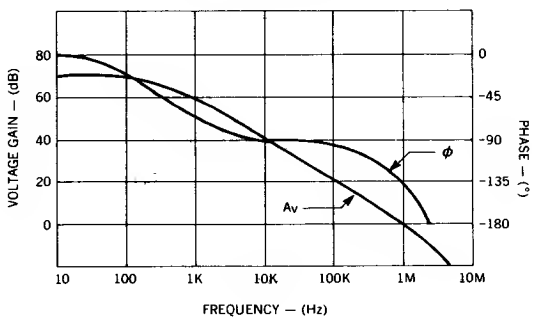
$$I_{Smax} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIREO TO SUPPRESS SWITCH TRANSIENTS.

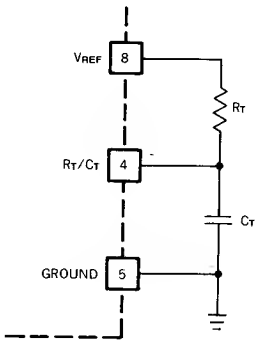
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response

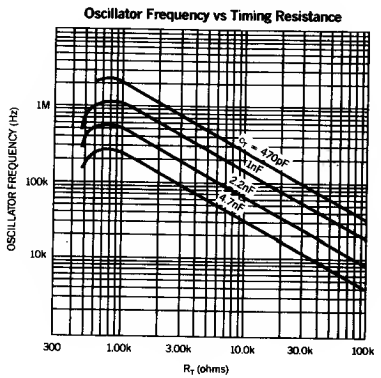


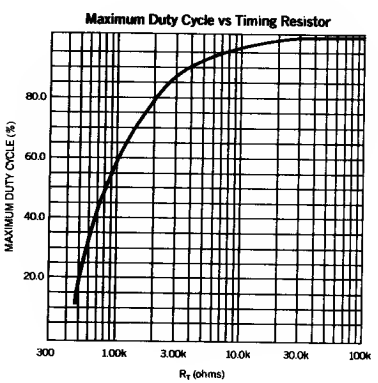
OSCILLATOR SECTION



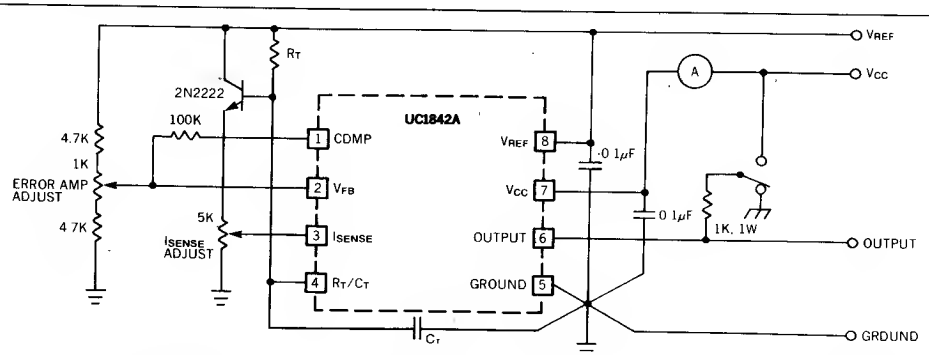
For $R_T > 5K$

$$f \approx \frac{1.72}{R_T C_T}$$





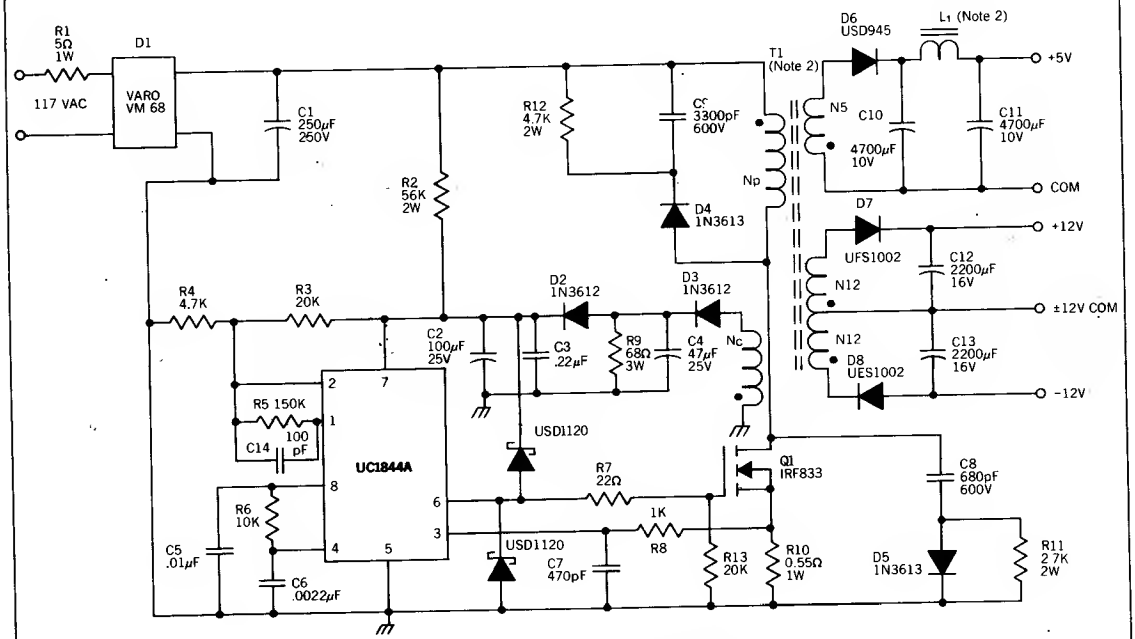
OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

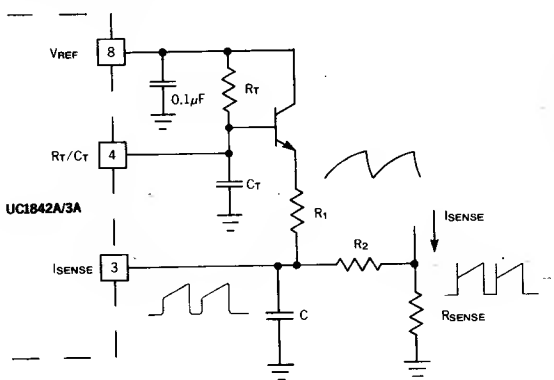
OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50mV P-P Max.
   - B. +12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.
   - C. -12V, ±3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

INTEGRATED CIRCUITS

UNITRODE

Current Mode PWM Controller

UC1846 UC1847
UC2846 UC2847
UC3846 UC3847

FEATURES

- Automatic feed forward compensation
- Programmable pulse by pulse current limiting
- Automatic symmetry correction in push-pull configuration
- Enhanced load response characteristics
- Parallel operation capability for modular power systems
- Differential current sense amplifier with wide common mode range
- Double pulse suppression
- 500mA (peak) totem-pole outputs
- ±1% bandgap reference
- Under-voltage lockout
- Soft start capability
- Shutdown terminal
- 500kHz operation

DESCRIPTION

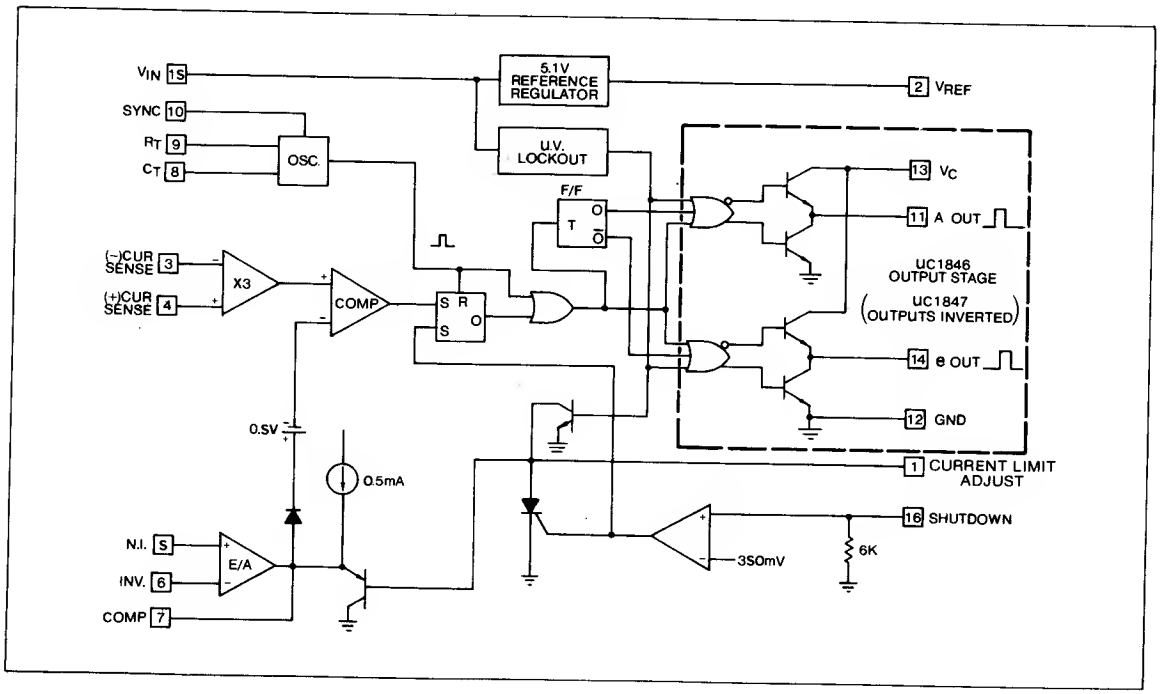
The UC1846/1847 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadtime adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



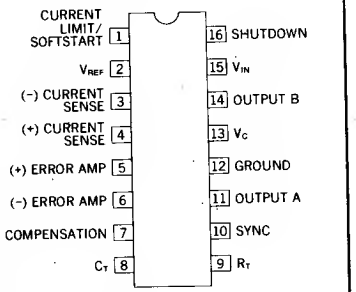
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... −0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... −30mA
Sync Output Current (Pin 10) ..... −5mA
Error Amplifier Output Current (Pin 7) ..... −5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note: 1. All voltages are with respect to Ground, Pin 13.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for UC1846/UC1847; −25°C to +85°C for the UC2846/UC2847; and 0°C to +70°C for the UC3846/3847; V_{IN} = 15V, R_T = 10k, C_T = 4.7nF) T_A = T_J

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 40V		5	20		5	20	mV
Load Regulation	I_L = 1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_j = 25°C (Note 2)		100			100		μV
Long Term Stability	T_j =125°C, 1000Hrs., (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF} = 0V	−10	−45		−10	−45		mA
Oscillator Section								
Initial Accuracy	T_j = 25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN} = 8 to 40V		−1	2		−1	2	%
Temperature Stability	Over Operating Range (Note 2)		−1			−1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0V			2.5			2.5	V
Sync Input Current	Sync Voltage = 3.9V, Pin 8 = 0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			−0.6	−1		−0.6	−2	μA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8 to 40V	0		V_{IN}−2V	0		V_{IN}−2V	V
Open Loop Voltage Gain	ΔV_O = 1.2 to 3V, V_{CM} = 2V	80	105		80	105		dB
Unity Gain Bandwidth	T_j = 25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0 to 38V, V_{IN} = 40V	75	100		75	100		dB
PSRR	V_{IN} = 8 to 40V	80	105		80	105		dB
Output Sink Current	V_{ID} = −15mV to −5V, $V_{Pin\ 7}$ = 1.2V	2	6		2	6		mA
Output Source Current	V_{ID} = 15mV to 5V, $V_{Pin\ 7}$ = 2.5V	−0.4	−0.5		−0.4	−0.5		mA

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for UC1846/UC1847; -25°C to +85°C for the UC2846/UC2847; and 0°C to +70°C for the UC3846/3847; V_{IN} = 15V, R_T = 10k, C_T = 4.7nF) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amp Section (continued)								
High Level Output Voltage	R_L = (Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = (Pin 7) 15kΩ		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{Pin\ 3}$ = 0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{Pin\ 4}$-$V_{Pin\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7) = 15kΩ	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{Pin\ 1}$ = 0.5V Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM} = 1 to 12V	60	83		60	83		dB
PSRR	V_{IN} = 8 to 40V	60	84		60	84		dB
Input Bias Current	$V_{Pin\ 1}$ = 0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	μA
Input Offset Current	$V_{Pin\ 1}$ = 0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	μA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_j = 25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{Pin\ 3}$ = 0V, $V_{Pin\ 4}$ = 0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{Pin\ 5}$ = V_{REF}, $V_{Pin\ 6}$ = 0V		-10	-30		-10	-30	μA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{Pin\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching Current ($I_{Pin\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_j = 25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40V (Note 5)			200			200	μA
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100mA		0.4	2.1		0.4	2.1	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	C_L = 1nF, T_j = 25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L = 1nF, T_j = 25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		
Total Standby Current								
Supply Current			17	21		17	21	mA

Notes:

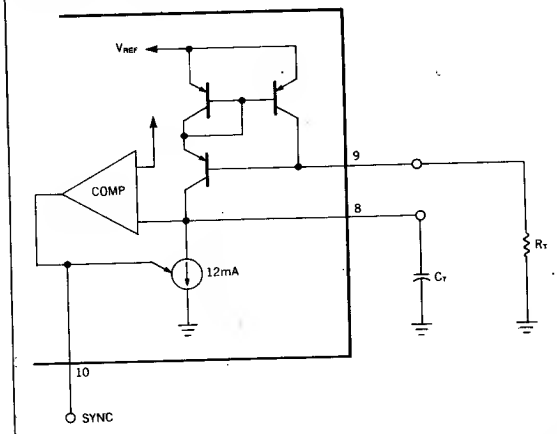
2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{Pin\ 5}$ = V_{REF}, $V_{Pin\ 6}$ = 0V.
4. Amplifier gain defined as:

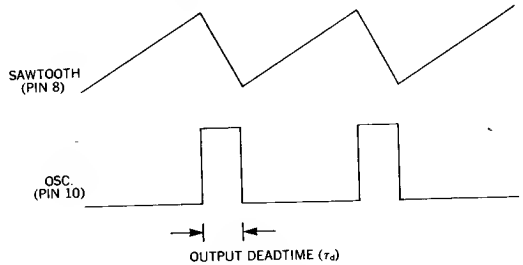
$$G = \frac{\Delta V_{Pin\ 7}}{\Delta V_{Pin\ 4}} \text{ ; } \Delta V_{Pin\ 4} = 0 \text{ to } 1.0V$$

5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



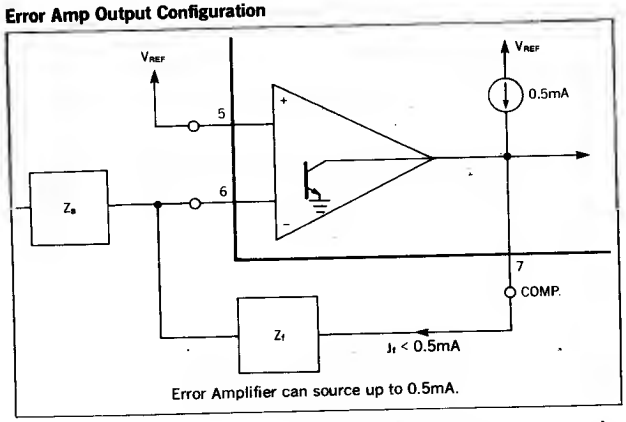


Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau_d\ (\mu s) = 145 C_T\ (\mu f) \left(\frac{12}{12 - \frac{3.6}{R_T\ (k\Omega)}} \right)$

For large values of R_T: $\tau_d\ (\mu s) \approx 145 C_T\ (\mu f)$

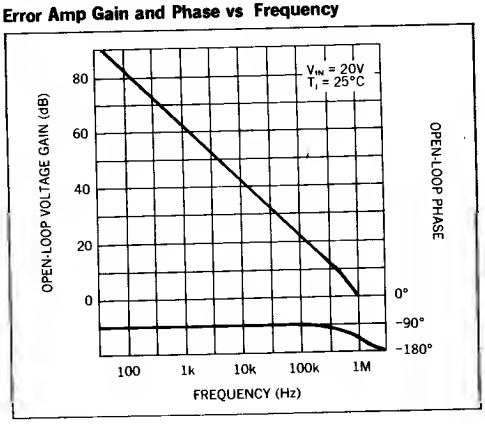
Oscillator frequency is approximated by the formula: $f_T\ (kHz) \approx \frac{2.2}{R_T\ (k\Omega)\ C_T\ (\mu f)}$

Error Amp Output Configuration

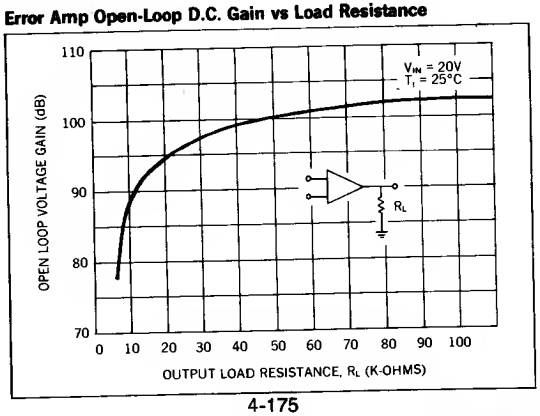


Error Amplifier can source up to 0.5mA.

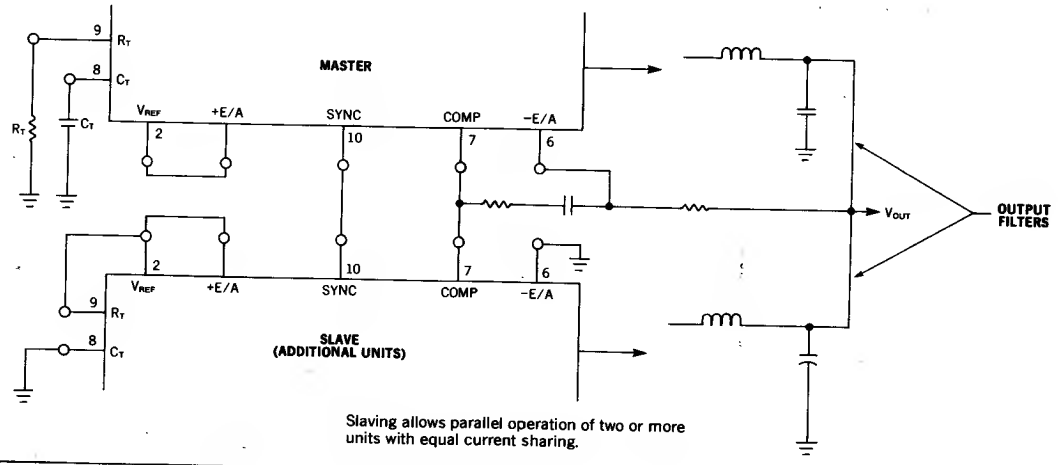
Error Amp Gain and Phase vs Frequency



Error Amp Open-Loop D.C. Gain vs Load Resistance

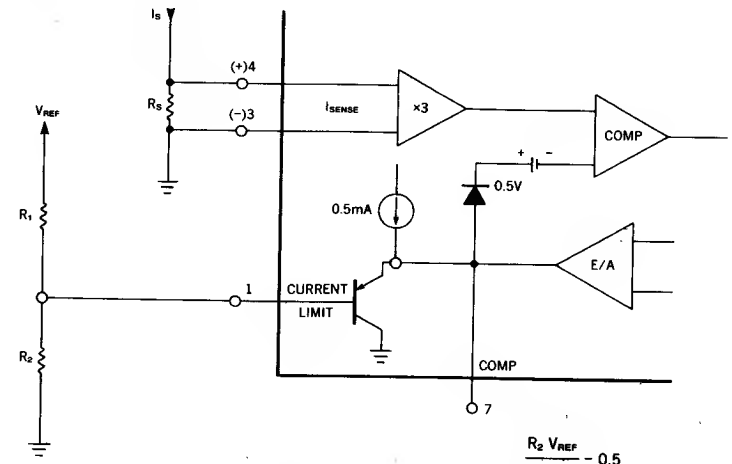


Parallel Operation



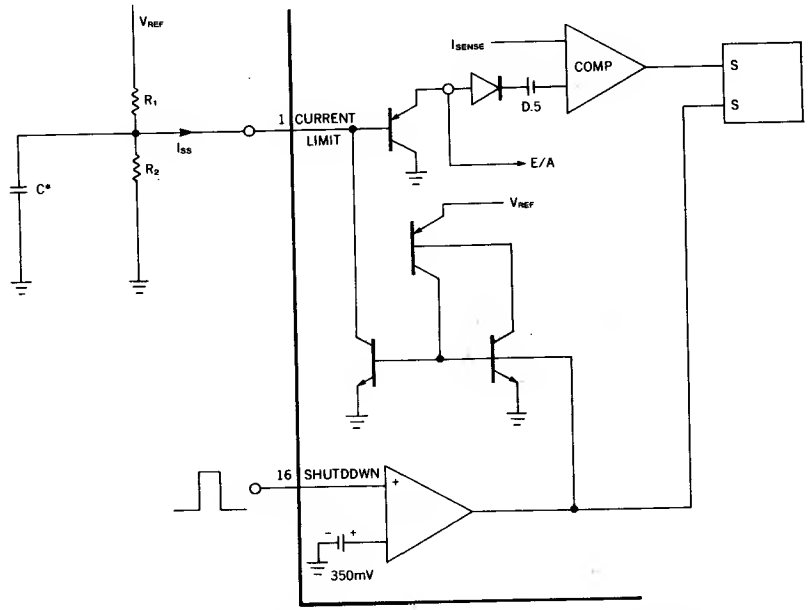
Slaving allows parallel operation of two or more units with equal current sharing.

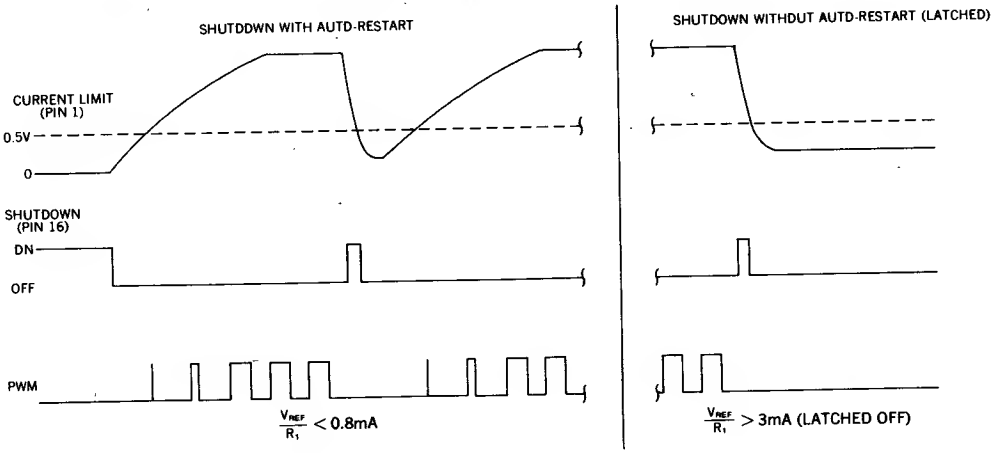
Pulse by Pulse Current Limiting



Peak Current (I_S) is determined by the formula: $I_S = \dfrac{\dfrac{R_2 V_{REF}}{R_1 + R_2} - 0.5}{3R_S}$

Soft Start and Shutdown/Restart Functions

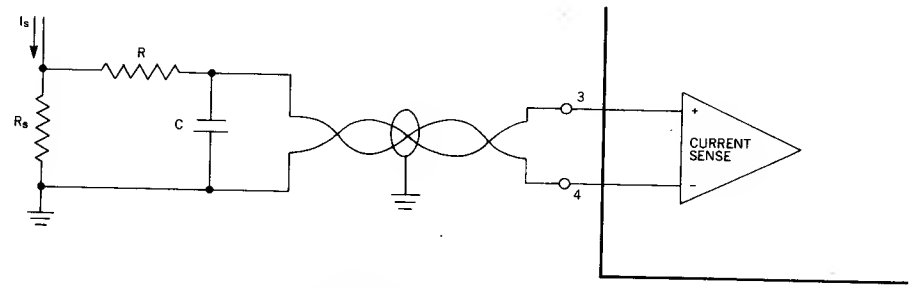




If $\frac{V_{REF}}{R_1} < 0.8mA$, the shutdown latch will commutate when I_{ss} = 0.8mA and a restart cycle will be initiated.

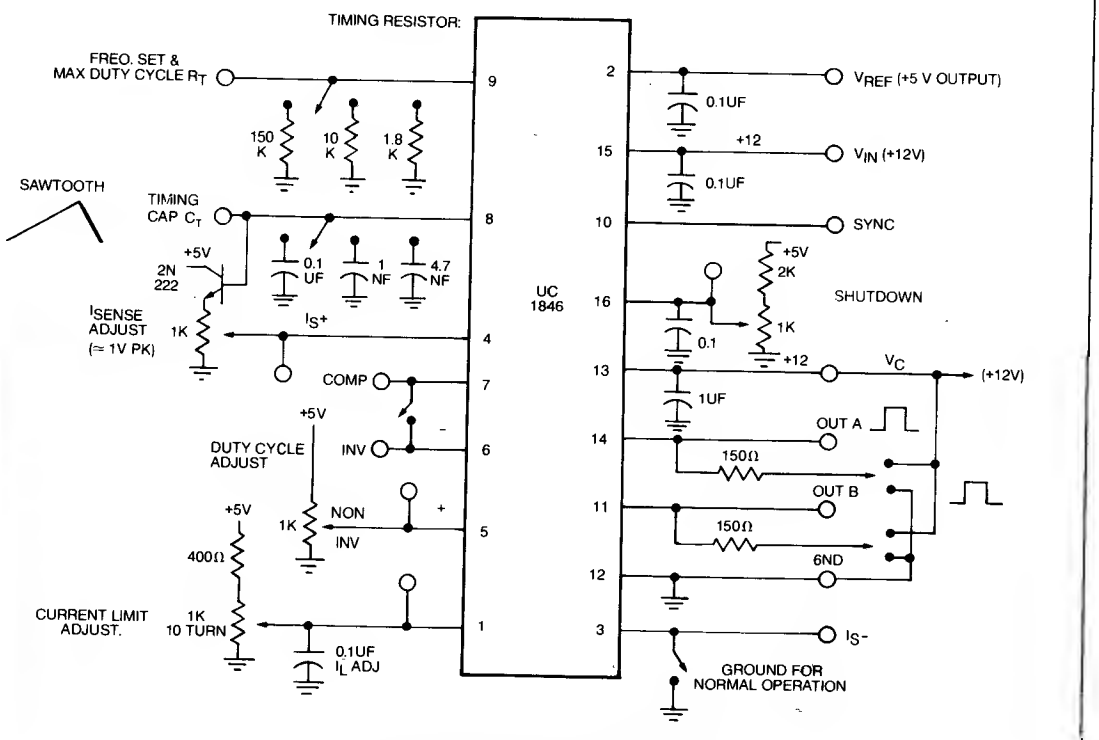
If $\frac{V_{REF}}{R_1} > 3mA$, the device will latch off until power is recycled.

Current Sense Amp Connections



A small RC filter may be required in some applications to reduce switch transients.
Differential input allows remote, noise free sensing.

UC1846 OPEN LOOP TEST CIRCUIT



—BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE.
—SHORT PINS 6 & 7 FOR UNITY GAIN TESTING.

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INTEGRATED CIRCUITS

UNITRODE

UC1846A
UC2846A
UC3846A

Improved Current Mode PWM Controller

ADVANCED INFORMATION

FEATURES

- High current dual totem pole outputs (1.5A peak)
- Improved current sense amplifier with reduced noise sensitivity
- 100ns delay from shutdown, oscillator, and current sense inputs to output
- Differential current sense amplifier with 3 volts common mode range
- Trimmed oscillator discharge current—10ma, 6% guaranteed
- Accurate shutdown threshold—1 volt, 5% guaranteed
- TTL compatible oscillator sync pin thresholds

DESCRIPTION

The UC1846A is a high performance version of the popular UC1846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized with no increase in quiescent current. Fast, 1.5 amp peak output stages have been added to allow rapid switching of power FETs.

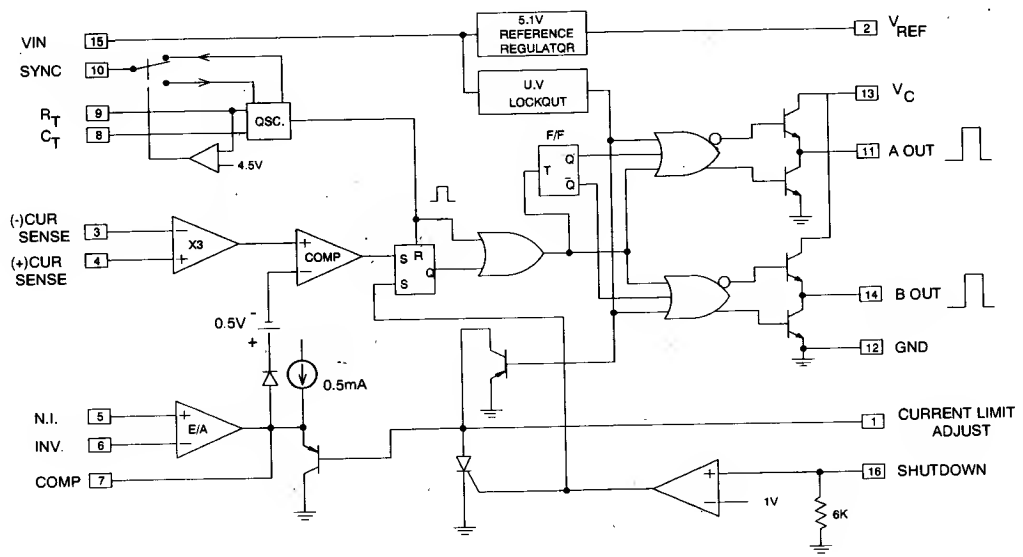
Internal chip grounding has been improved to eliminate internal "noise" caused when driving large capacitive loads. This, in conjunction with an improved differential current sense amplifier, results in enhanced noise immunity.

A dual function sync pin with TTL thresholds functions as a sync output in the normal mode, and as a sync input if R_t (pin 5) is tied to V_{ref} (pin 16).

Other features include a trimmed oscillator discharge current (5%) for accurate frequency and dead time control, a 5%, 1 volt shutdown threshold, and 2kv minimum ESD protection on all pins.

4

BLOCK DIAGRAM



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INTEGRATED CIRCUITS

UNITRODE

Programmable, Off-Line, PWM Controller

UC1851
UC2851
UC3851

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

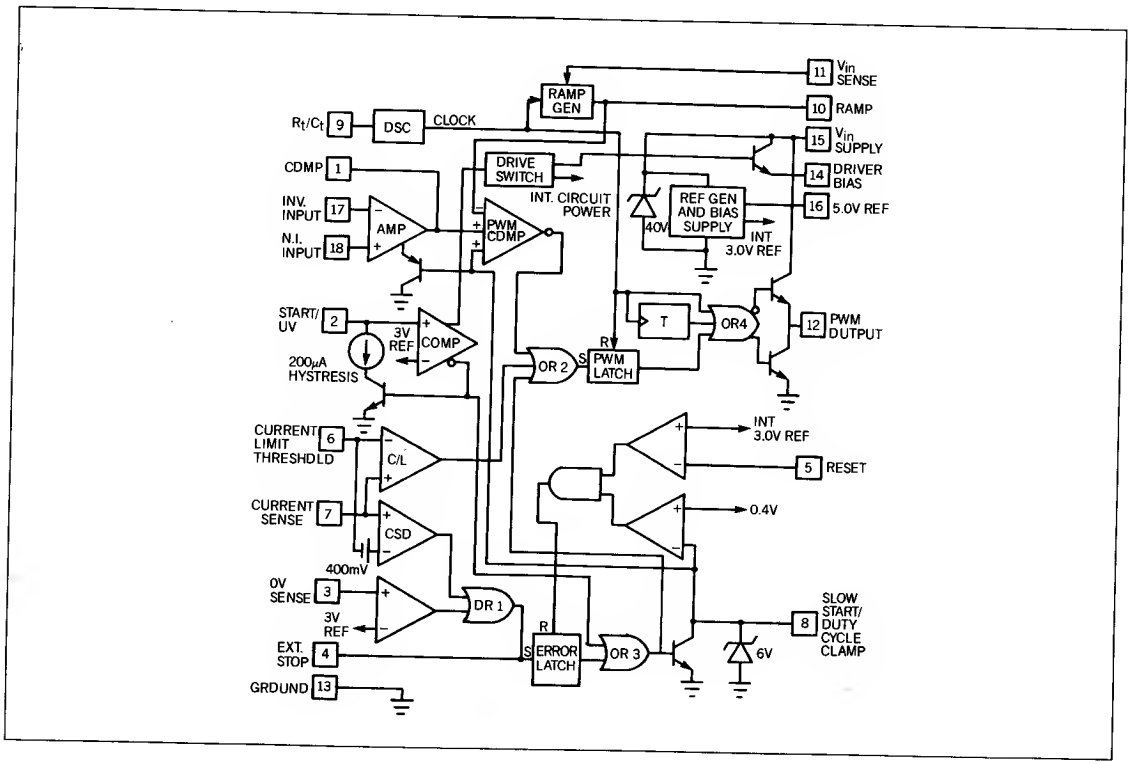
DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for −55°C to +125°C operation while the UC2851 and UC3851 are designed for −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

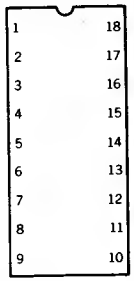
Supply Voltage, $+V_{IN}$ (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... −200mA
Reference Output Current (Pin 16) ..... −50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... −0.5 to +5.5V
Stop Input (Pin 4) ..... −0.3 to +5.5V
Comparator Inputs
(Pins 1–7, 9–11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

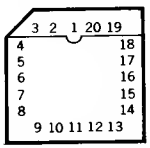
Notes: 1. All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal.
2. All pin numbers are referenced to DIL-18 package.

CONNECTION DIAGRAMS

TOP VIEWS
DIL-18, J or N PACKAGE



PLCC-20
Q PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DIL	PLCC
COMP	1	1
START/UV	2	2
OV SENSE	3	5
STOP	4	4
RESET	5	5
CUR THRESH	6	7
CUR SENSE	7	8
SLOW START	8	9
RT/CT	9	10
RAMP	10	11
V_{IN} SENSE	11	12
PWM OUT	12	13
GROUND	13	14
DRIV BIAS	14	15
$+V_{IN}$ SUPPLY	15	17
5.0V REF	16	18
INV INPUT	17	19
N.I. INPUT	18	20

4

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1851, −25°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV). $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1851 UC2851			UC3851			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V,		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	V_{IN} = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over operating temperature range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		−80	−100		−80	−100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over operating temperature range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = −10μA		−11	−14		−11	−14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	−0.9	−.95		−0.9	−.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the UC1851, $-25°C$ to $+85°C$ for the UC2851, and $0°C$ to $70°C$ for the UC3851; $V_{IN} = 20V$, $R_T = 20k\Omega$, $C_T = .001mfd$, $R_R = 10k\Omega$, $C_R = .001mfd$, Current Limit Threshold $= 200mV$). $T_A = T_J$

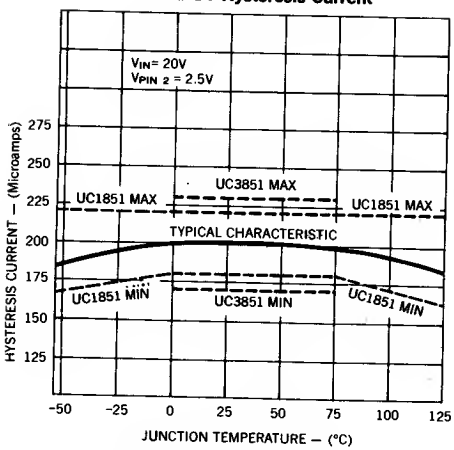
PARAMETER	TEST CONDITIONS	UC1851 UC2851			UC3851			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amplifier								
Input Offset Voltage	$V_{CM} = 5.0V$		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	$\Delta V_O = 1$ to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak − 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	$V_{CM} = 1.5$ to 5.5V	70	80		70	80		dB
PSRR	$V_{IN} = 8$ to 30V	70	80		70	80		dB
Short Circuit Current	$V_{COMP} = 0V$		−4	−10		−4	−10	mA
Gain Bandwidth*	$T_J = 25°C$, $A_{VOL} = 0dB$	1	2		1	2		MHz
Slew Rate*	$T_J = 25°C$, $A_{VCL} = 0dB$		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	$I_{SOURCE} = 20mA$	18	18.5		18	18.5		V
	$I_{SOURCE} = 200mA$	17	18.5		17	18.5		V
Rise Time *	$T_j = 25°C$, $C_L = 1nF$		50	150		50	150	ns
Fall Time *	$T_j = 25°C$, $C_L = 1nF$		50	150		50	150	ns
Output Saturation	$I_{OUT} = 20mA$		0.2	0.4		0.2	0.4	V
Output Saturation	$I_{OUT} = 200mA$		1.7	2.2		1.7	2.2	V
Comparator Delay*	Pin 8 to Pin 12 $T_J = 25°C$, $R_L = 1k\Omega$		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		−1.0	−4.0		−1.0	−4.0	μA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V,	170	200	220	170	200	230	μA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		−120	−200		−120	−200	μA
Driver Bias Saturation Voltage, $V_{IN} - V_{OH}$	$I_B = -50mA$		2	3		2	3	V
Driver Bias Leakage	$V_B = 0V$		−0.1	−10		−0.1	−10	μA
Slow-Start Saturation	$I_S = 10mA$		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	$V_S = 4.5V$		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		−2	−5		−2	−5	μA
Common Mode Range*		−0.4		3.0	−0.4		3.0	V
Current Limit Delay*	$T_J = 25°C$, Pin 7 to 12, $R_L = 1k$		200	400		200	400	ns

*Guaranteed by design. Not 100% tested in production.

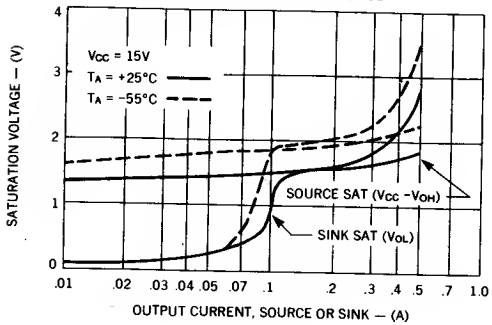
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator:	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier:	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is a high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200μA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5> 3.2V. Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. Ext. Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/μF.

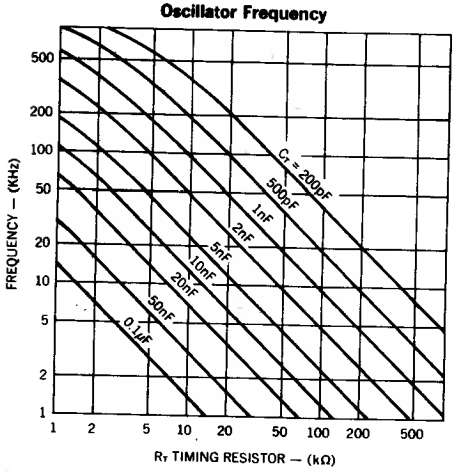
Start/UV Hysteresis Current



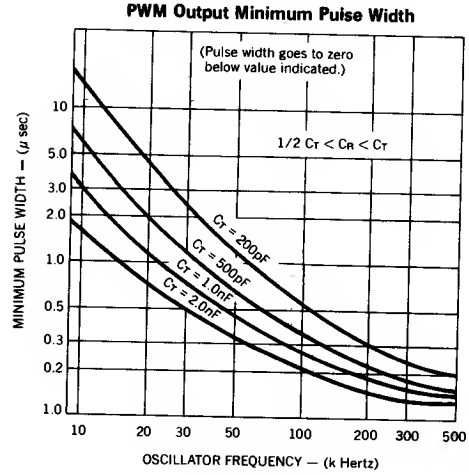
Output Saturation Characteristics



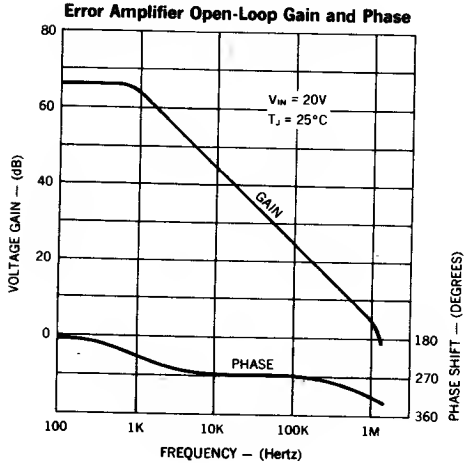
Oscillator Frequency



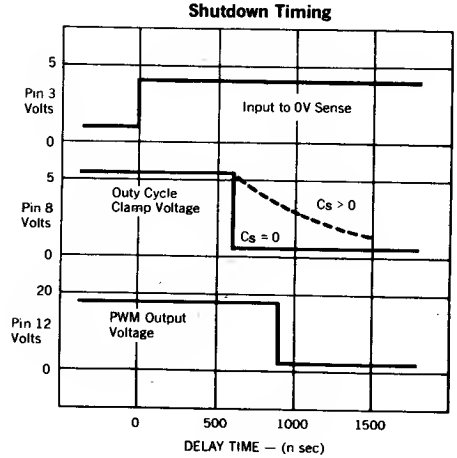
PWM Output Minimum Pulse Width



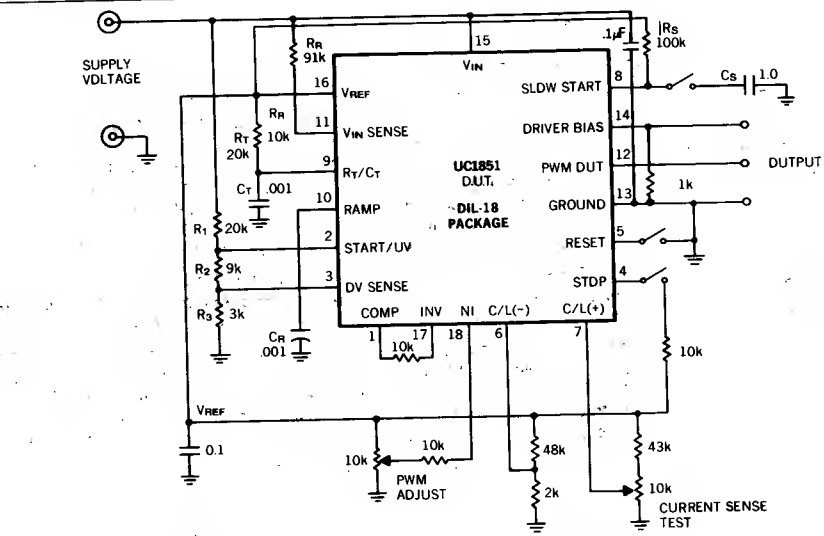
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



OPEN-LOOP TEST CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50kHz

Start Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right) + 0.2R_1 = 12V$

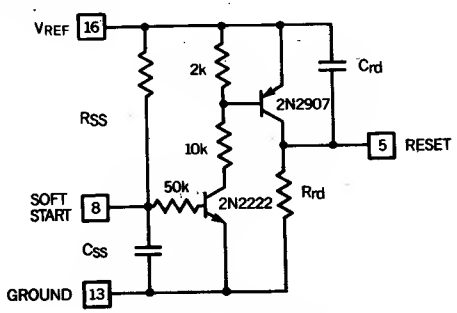
UV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_2 + R_3}\right) = 8V$

OV Fault Voltage = $3\left(\frac{R_1 + R_2 + R_3}{R_3}\right) = 32V$

Current Limit = 200mV
Current Fault Voltage = 600mV
@V_{in} = 15V, Duty Cycle ≈ 48%
@V_{in} = 30V, Duty Cycle ≈ 24%

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

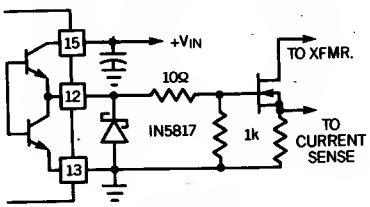
PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT



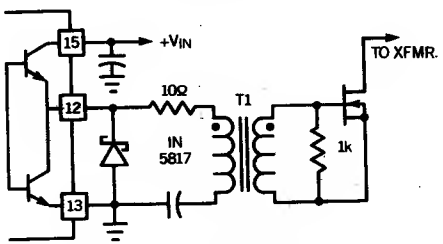
Restart Delay = (.51) (Rrd) (Crd)

For further application information see UC1840/UC1841 Data Sheets.

UC1851 POWER MOSFET DRIVE INTERFACE



A) DIRECT DRIVE



B) TRANSFORMER COUPLED

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

4

INTEGRATED CIRCUITS

UNITRODE

High Power Factor Preregulator

UC1854
UC2854
UC3854

PRELIMINARY

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion to <5%
- World-wide Operation Without Switches
- Feed-forward Line Regulation
- Low Noise Sensitivity
- Low Start-up Supply Current
- Fixed-frequency PWM Drive
- Low-offset Analog Multiplier/Divider
- 1 Amp Totem-Pole Gate Driver
- Precision Voltage Reference

DESCRIPTION

The UC1854 family of integrated circuits provide active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. These parts implement all the control functions necessary to build a power supply preregulator capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, a precision analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC1854 contains a power MOSFET gate driver, 7.5V reference, line anticipator, load-enable comparator, low supply detector, and over current comparator.

The UC1854 family use average current mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current mode control, average current control accurately maintains sinusoidal line current without slope compensation.

The UC1854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC1854 can be used in systems with line voltages that vary from 75 to 275 volts and with line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 family features low start-up supply current.

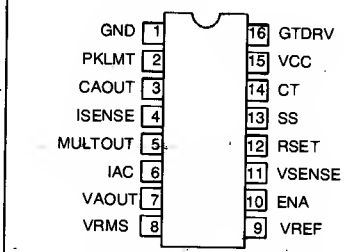
These devices are available packaged in 16-pin plastic and ceramic dual in-line packages.

ABSOLUTE MAXIMUM RATINGS

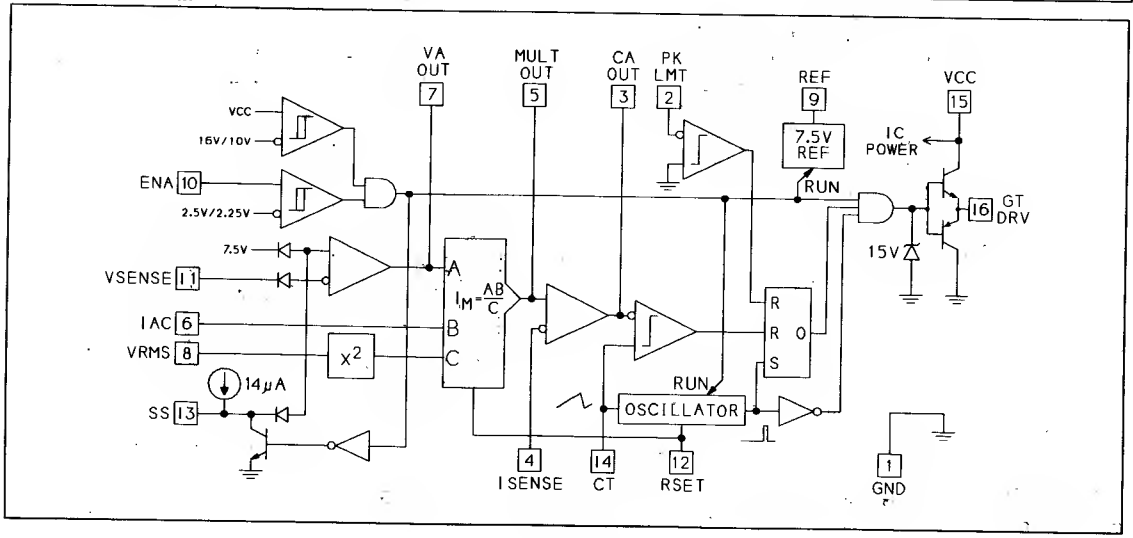
Supply Voltage VCC 35V
GTDRV Current, Continuous 0.5A
GTDRV Current, 50% Duty Cycle 1.5A
Input Voltage, VSENSE, VRMS 11V
Input Voltage, ENA, ISENSE, MULTOUT 11V
Input Voltage, PKLMT 5V
Input Current, RSET, IAC, PKLMT 10mA
Power Dissipation at TA≤25°C 1W
Derate 8mW/°C for TA>25°C
Storage Temperature . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C
NOTE 1: All voltages with respect to GND (Pin 1).
NOTE 2: All currents are positive into the specified terminal.

CONNECTION DIAGRAM

DIL–16 (TOP VIEW)
J or N Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=18V, RSET=15K to ground, CT=1.5nF to ground, PKLMT=1V, ENA=7.5V, VRMS=1.25V, IAC=100μA, ISENSE=0V, CAOUT=3.5V, VAOUT=5V, VSENSE=7.5V, no load on any output, and $-55^{\circ}C<T_A<125^{\circ}C$ for the UC1854, $-25^{\circ}C<T_A<125^{\circ}C$ for the UC2854, and $0^{\circ}C<T_A<70^{\circ}C$ for the UC3854. $T_A=T_j$

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
OVERALL					
Supply Current, Off	ENA=0V		1.5	2.0	mA
Supply Current, On			10	16	mA
VCC Turn-On Threshold		15	16	17	V
VCC Turn-Off Threshold		9	10	11	V
ENA Threshold, Rising		2.4	2.55	2.7	V
ENA Threshold Hysteresis		0.2	0.25	0.3	V
ENA Input Current	ENA=0V	-5.0	-0.2	5.0	μA
VOLTAGE AMPLIFIER					
Voltage Amp Offset Voltage	VAOUT=3.5V	-8		8	mV
VSENSE Bias Current	VSENSE=0V	-500	-25	500	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Output Swing		0.5 to 16			V
Voltage Amp Short Circuit Current	VAOUT=0V	5	12	30	mA
SS Current	SS=2.5V	6	14	20	μA
CURRENT AMPLIFIER					
Current Amp Offset Voltege		-1		1	mV
ISENSE Bias Current		-500	-100	500	nA
Current Amp Gein		80	110		dB
Current Amp Output Swing		0.5 to 16			V
Current Amp Short Circuit Current	CAOUT=0V	5	12	30	mA
Input Range, ISENSE, MULTOUT		-0.3 to 1.0			V
REFERENCE					
Reference Output Voltage	IRef=0mA, TA=25oC	7.425	7.50	7.575	V
VREF Loed Regulation	-10mA<IRef<0mA	-15	5	15	mV
VREF Line Regulation	15V<VCC<35V	-10	2	10	mV
VREF Short Circuit Current	REF=0V	12	28	45	mA
CURRENT LIMIT					
PKLMT Offset Voltage		-10		10	mV
PKLMT Input Current	PKLMT=-0.1V	-200	-100		μA
PKLMT to GTDRV Prop. Delay	PKLMT falling from 50mV TO -50mV		175		ns
GATE DRIVER					
Maximum GTDRV Output Voltage	0mA loed on GTDRV, 18V<VCC<35V	13	14.5	16	V
GTDRV Output Voltage High	-200mA load on GTDRV, VCC=15V	12	12.8		V
GTDRV Output Voltage Low, OFF	VCC=0V, 50mA load on GTDRV		0.9	1.5	V
GTDRV Output Voltage Low	200mA load on GTDRV		1.0	2.2	V
Peak GTDRV Current	10nF from GTDRV to GND		1		A
GTDRV Rise/Fell Time	1nF from GTDRV to GND		35		ns
GTDRV Maximum Duty Cycle			95		%

4

MULTIPLIER					
Multiplier Output Current Full Scale	IAC=100μA, RSET=10K	–220	–200	–180	μA
Multiplier Output Current Zero	IAC=0μA, RSET=15K	–2.0	–.2	2.0	μA
Multiplier Maximum Output Current	IAC=450μA, RSET=15K	–280	–255	–220	μA
Multiplier Output Current	IAC=50μA, VRMS=2V, VA = 4V	–33	–42	–50	μA
Multiplier Output Current	IAC=100μA, VRMS=2V, VA = 2V	–17	–27	–37	μA
Multiplier Output Current	IAC=200μA, VRMS=2V, VA = 4V	–135	–150	–165	μA
Multiplier Output Current	IAC=300μA, VRMS=1V, VA = 2V	–200	–225	–250	μA
Multiplier Output Current	IAC=100μA, VRMS=1V, VA = 2V	–60	–80	–95	μA
Multiplier Gain Constant	See Note 3		–1.0		V
OSCILLATOR					
Oscillator Frequency		46	55	62	kHz
CT Ramp Peak-to-Peak Amplitude		4.8	5.2	5.6	V
CT Ramp Valley Voltage		0.8	1.1	1.3	V

Note 3: Multiplier Gain Constant (K) is defined by the following equation: $I_{MULTOUT} = \frac{K * IAC * (VAOUT-1)}{VRMS^2}$

PIN DESCRIPTIONS

GND (Pin 1) (ground): All voltages are measured with respect to GND. VCC and REF should be bypassed directly to GND with an 0.1uF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND should also be as short and as direct as possible.

PKLMT (Pin 2) (peak limit): The threshold for PKLMT is GND. Connect this input to the negative voltage on the current sense resistor as shown in Figure 1. Use a resistor to REF to offset the negative current sense signal up to GND.

CAOUT (Pin 3) (current amplifier output): This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled.

ISENSE (Pin 4) (current sense minus): This is the inverting input to the current amplifier. This input and the non-inverting input MULTOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below –0.5V, because they are protected with diodes to GND.

MULTOUT (Pin 5) (multiplier output and current sense plus): The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MULTOUT. The cautions about taking ISENSE below –0.5V also apply to MULTOUT. As the multiplier output is a current, this is a high impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject GND noise. Figure 1. shows an example of using the current amplifier differentially.

IAC (Pin 6) (input AC current): This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MULTOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6V, so in addition to a resistor from IAC to rectified 60Hz, connect a resistor from IAC to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

VAOUT (Pin 7) (voltage amplifier output): This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will also stay active even if the IC is disabled with either ENA or VCC. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output.

VRMS (Pin 8) (RMS line voltage): The output of a boost PWM is proportional to the Input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the VRMS input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage should stay between 1V and 5V.

PIN DESCRIPTIONS

REF (Pin 9) (voltage reference output): REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when VCC is low or when ENA is low. Bypass REF to GND with an 0.1mF or larger ceramic capacitor for best stability.

ENA (Pin 10) (enable): ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22K resistor.

VSENSE (Pin 11) (voltage amplifier inverting input): This is normally connected to a feedback network and to the boost converter output through a divider network.

RSET (Pin 12) (oscillator charging current and multiplier limit set): A resistor from RSET to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from RSET to ground.

SS (Pin 13) (soft start): SS will remain at GND as long as the IC is disabled or VCC is too low. SS will pull up to over 8V by an internal 14μA current source when both VCC becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

CT (Pin 14) (oscillator timing capacitor): A capacitor from CT to GND will set the PWM oscillator frequency according to this relationship:

$$F = \frac{1.25}{RSET\ CT}$$

VCC (Pin 15) (positive supply voltage): Connect VCC to a stable source of at least 20mA above 17V for normal operation. Also bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GTDRV signals, these devices will be inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

GTDRV (Pin 16) (gate drive): The output of the PWM is a totem pole MOSFET gate driver on GTDRV. This output is internally clamped to 15V so that the IC can be operated with VCC as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.

4

APPLICATIONS INFORMATION

A 250W PREREGULATOR

The circuit of Figure 1 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the UC3854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the UC3854 provides PWM pulses (GT DRV, Pin 16) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN #	FUNCTION
VSENS	11	Output DC Voltage
IAC	6	Line Voltage Waveform
ISENS/MULT OUT	4/5	Line Current
VRMS	8	RMS Line Voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions, as follows:

INPUT	PIN #	FUNCTION
ENA	10	Start-Up Delay
SS	13	Soft Start
PK LIM	2	Maximum Current Limit

PROTECTION INPUTS

ENA (Enable)

The ENA input must reach 2.5 volts before the REF and GTDRV outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at pin 15, where the on/off thresholds are 16V and 10V.

SS (Soft start)

The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically 7.5V. An internal current source delivers approximately -14μA from pin 13. Thus a capacitor connected between that pin and ground will charge linearly from zero to 7.5V in 0.54C seconds, with C expressed in microfarads.

APPLICATIONS INFORMATION

PKLIM (Peak current limit)

Use pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 1, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.25 ohm current sense resistor is 7.5V*2K/10K=1.5V, corresponding to 6A. A bypass capacitor from pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

VSENS (Output DC voltage sense)

The threshold voltage for the VSENS input is 7.5V and the input bias current is typically 50nA. The values shown in Figure 1 are for an output voltage of 400V DC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 47nF feedback capacitor places a 15Hz pole in the voltage loop that prevents 120Hz ripple from propagating to the output current.

IAC (Line waveform)

In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.

This input is not a voltage, but a current (hence IAC). It is set up by the 150K and 620K resistive divider (see Figure 1). The voltage at pin 6 is internally held at 6V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400uA at the peak of the waveshape. The following formulas were used to calculate these resistors:

$$R_{AC} = (Vpk + 6) / 400\mu A = 620K$$

$$R_{REF} = R_{IAC}/4 = 150K$$

(where Vpk is the peak line voltage)

ISENS/MULTOUT (Line current)

The voltage drop across the 0.25 ohm current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

VRMS (rms line voltage)

An important feature of the UC3854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in the US (85VAC) to high line in Europe (255VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assumming constant load power). To do this, the multiplier divides the line current by the square of the rms value of the line voltage. The voltage applied to pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at pin 5, is a current that increases with the current at pin 6 and the voltage at pins 7, and decreases with the square of the voltage at pin 8.

PWM FREQUENCY

The PWM oscillator frequency in Figure 1 is 100kHz. This value is determined by CT at pin 14 and RSET at pin 12. RSET should be chosen first because it affects the maximum value of IMULT according to the equation:

$$IMULT_{MAX} = \frac{-3.75}{RSET}$$

This effectively sets a maximum PWM-controlled current. With RSET=15K,

$$IMULT_{MAX} = \frac{-3.75V}{15K} = -250uA$$

It is also important to note that the multiplier output current will never exceed twice IAC.

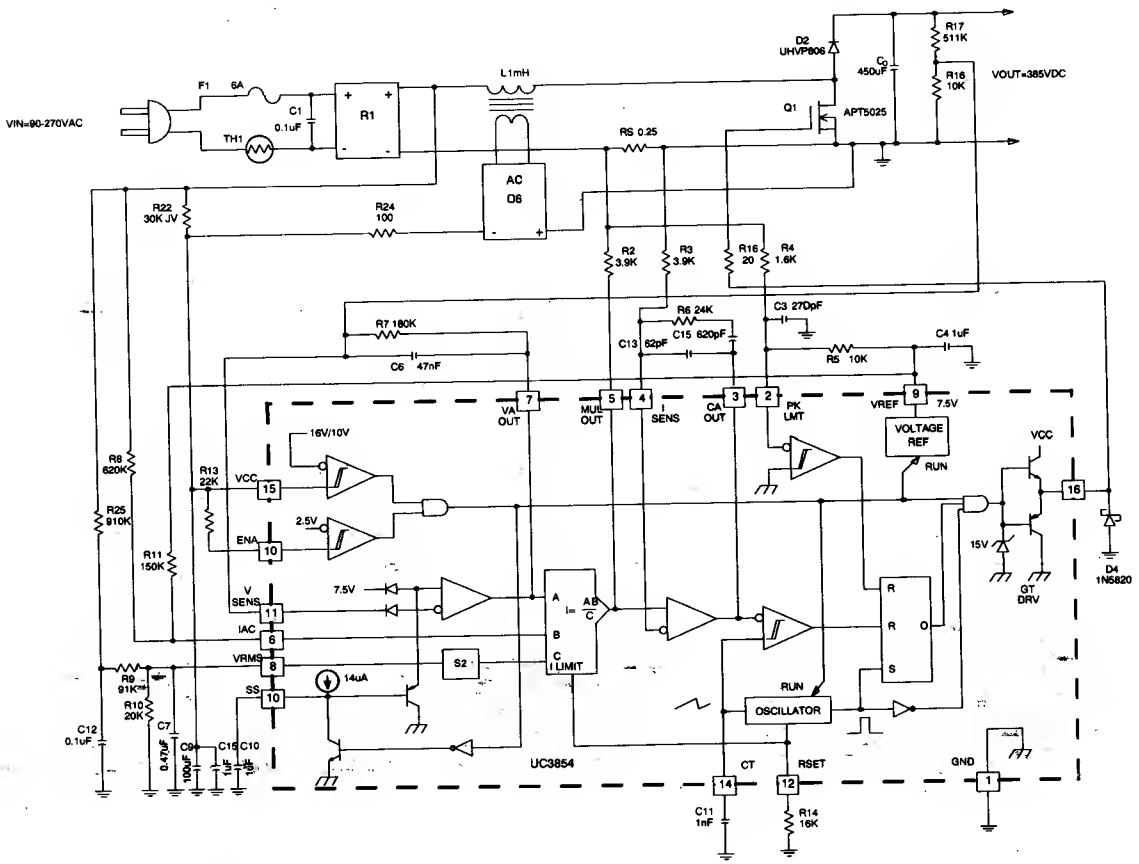
With the 4K resistor from MULTOUT to the 0.25 ohm current sense resistor, the maximum current in the current sense resistor will be

$$I_{MAX} = \frac{-IMULT_{MAX} \times 4K}{0.25\ ohm} = 4Amp$$

Having thus selected RSET, the current sense resistor, and the resistor from MULTOUT to the current sense resistor, calculate CT for the desired PWM oscillator frequency from the equation

$$C_T = \frac{1.25}{F \times RSET}$$

FIGURE 1
250 WATT PREREGULATOR



NOTE: Boost inductor can be fabricated with ARNOLD MPP toroidal core part number A-438381-2 using a 55 turn primary and a 13 turn secondary.

These products contain patented circuitry and are sold under license from Pioneer Magnetics, Inc.

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INTEGRATED CIRCUITS

UNITRODE

RESONANT MODE POWER SUPPLY CONTROLLER

UC1860
UC2860
UC3860

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer — Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

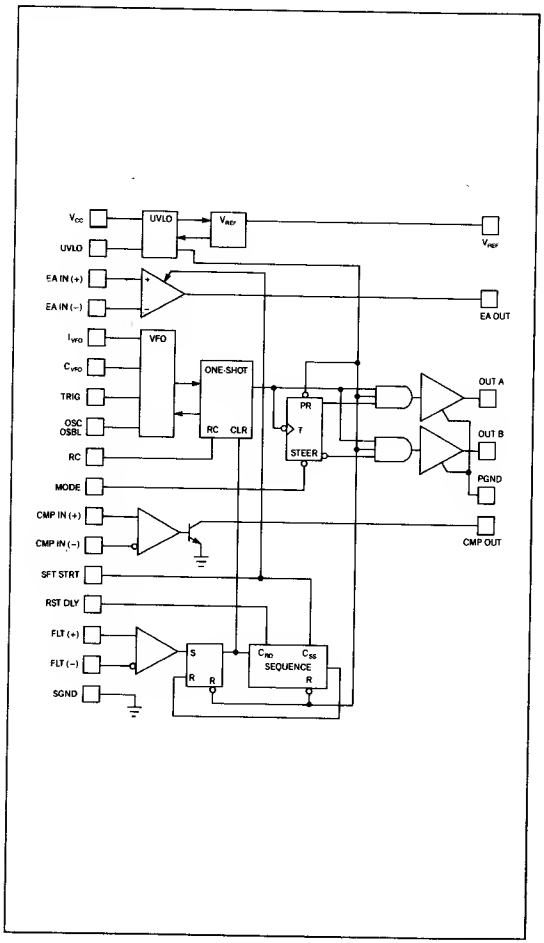
DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant-mode power supply control. This device easily implements frequency-modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

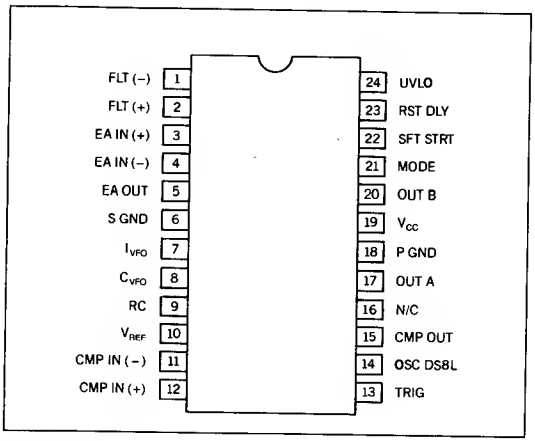
The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

BLOCK DIAGRAM

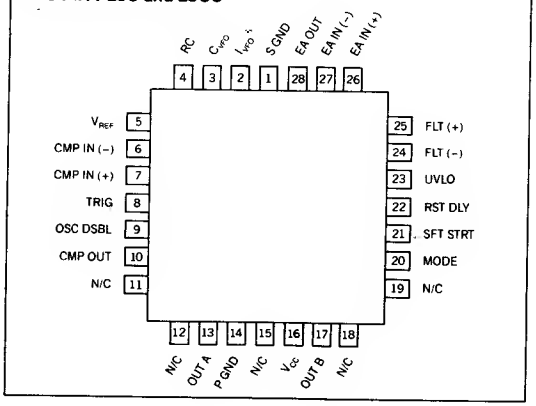


PIN SCHEDULE



PIN SCHEDULE

28 PIN PLCC and LCCC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 19) 20V
Output Current, Source or Sink (pins 17 & 20) 0.8A
DC 3.0A
Pulse (0.5 μs) ..... ± 0.2V
Power Ground Voltage ..... −0.4 to 6V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12, 13, 14, 21, 22, 23 & 24) 2mA
Error Amp Output Current, Source or Sink (pin 5) 2mA
I_{VFO} Current (pin 7) 5mA
Comparator Output Current (pin 15) 15V
Comparator Output Voltage (pin 15) 5mA
Soft Start or Restart Delay Sink Current (pins 22 & 23) 1.25W
Power Dissipation at T_A = 50C (DIP) 1W
Derate 12.5 mW/C for T_A above 50C
Power Dissipation at T_A = 50C (PLCC) ..... 300°C
Derate 10 mW/C for T_A above 50C
Lead Temperature (Soldering, 10 seconds) .....

Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the DIP.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, all specifications apply for $-55 \leq T_A \leq 125°C$ for the UC1860, $-25 \leq T_A \leq 85°C$ for the UC2860, $0 \leq T_A \leq 70°C$ for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k.) $T_A = T_J$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reference Section					
Output Voltage	T_A = 25°C, I_O = 0 I_O = 0	4.95 4.93	5.00	5.05 5.07	V V
Line Regulation	$10 \leq V_{CC} \leq 20V$		2	15	mV
Load Regulation	$0 \leq I_O \leq 10mA$		2	25	mV
Output Noise Voltage*	$10Hz \leq f \leq 10kHz$		50		μV_{RMS}
Short Circuit Current	V_{REF} = 0V	−150		−15	mA
Error Amplifier Section					
Input Offset Voltage	$2.8 \leq V_{CM} \leq 4.5V$		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	dV_O = 1.5V	60	80		dB
PSRR	$10 \leq V_{CC} \leq 20V$	70	100		dB
Output Low (V_O-V_{IVFO})	$-0.1 \leq I_O \leq 0.1mA$	−8	0	8	mV
Output High (V_O-V_{IVFO})	$-0.5 \leq I_O \leq 0.5mA$	1.9	2	2.1	V
Unity Gain Bandwidth*	R_{IN} = 2k	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dIosc*	$100 \leq I_{VFO} \leq 500\mu A$	2	3	4	GHz/A
Trig In Threshold		1.0	1.4	1.8	V
Trig In Open Circuit Voltage		0.7	0.9	1.1	V
Trig In Delta (V_{TH}-V_{OC})		0.3	0.5	0.7	V
Trig In Input Resistance	dV_{TRIG} = V_{OC} to V_{TH}	5	12	25	kohm
Minimum Trig In Pulse Width*			3	10	ns
Osc Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	I_{VFO} = 1.5mA	2.8	3.7	4.6	MHz
Dead Time*	I_{VFO} = 1.5mA	35	70	100	ns

*Guaranteed by design but not 100% tested.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, all specifications apply for $-55 \leq T_A \leq 125°C$ for the UC1860, $-25 \leq T_A \leq 85°C$ for the UC2860, $0 \leq T_A \leq 70°C$ for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k). $T_A = T_J$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	−20mA		1.5	2.0	V
	−200mA		1.7	2.5	V
Rise/Fall Time*	C_{LOAD} = 1nF		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
V_{CC} Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysterisis	0.2	0.4	0.6	V
UVLO Input Resistance	UVLO = 4/V_{CC} = 8	10	23	50	kohm
V_{REF} Comparator Threshold	V_{CC} = UVLO = V_{REF}		4.5	4.9	V
Supply Current					
I_{CC}	V_{CC} = 12V, V_{OSC} DSBL = 3V		30	40	mA
I_{START}	UVLO pin open V_{CC} = V_{CC} (on) −0.3V		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	$-0.3 \leq V_{CM} \leq 3V$		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Propagation Delay To Output*	±50mV input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	$-0.3 \leq V_{CM} \leq 3V$		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Output Low Voltage	I_O = 2mA		0.3	0.5	V
Propagation Delay To Sat*	±50mV input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	I_{SINK} = 100µA		0.2	0.5	V
Charge Current (2 pins)		2	5	10	µA
Restart Delay Threshold		2.8	3.0	3.2	V

*Guaranteed by design but not 100% tested.

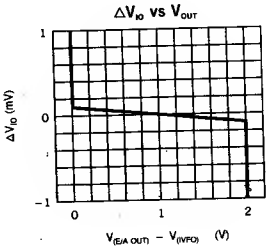
ERROR AMPLIFIER

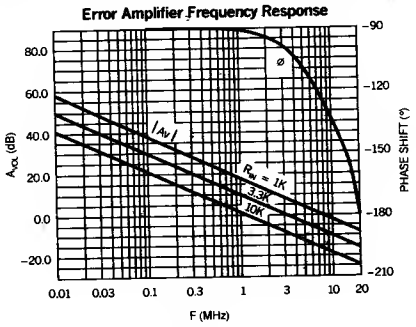
The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

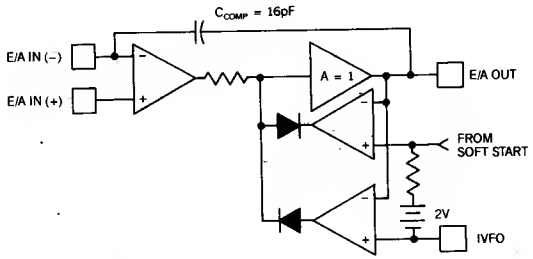
Frequency (0dB) = 1 / (2π * R_{IN} (−) * C_{COMP}).

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the I_{VFO} pin is limited from zero to 2V. Note that pulling Sft Strt (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.





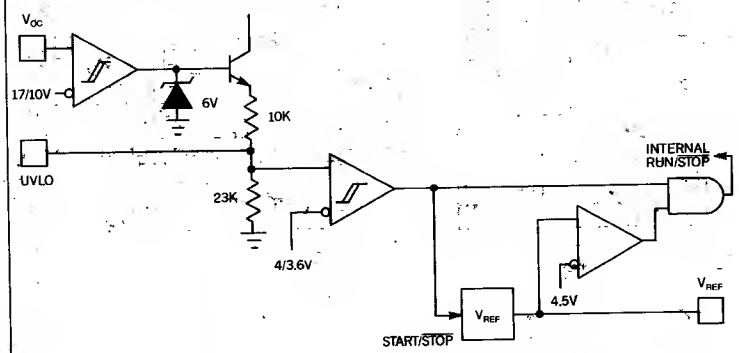


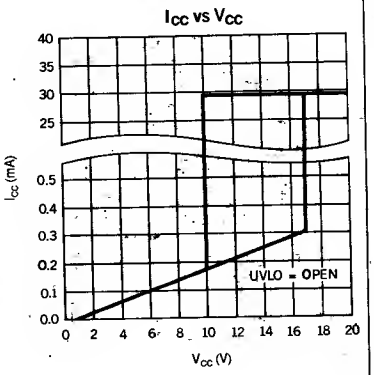
UNDER VOLTAGE LOCKOUT SECTION

The under voltage lockout consists of three comparators that monitor V_{CC}, UVLO, and V_{REF}. The V_{REF} comparator makes sure that the reference voltage is sufficiently high before operation begins. When the UVLO comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The V_{CC} comparator is used for off-line applications by leaving the UVLO pin open. In this application the supply current is typically less than 0.3mA during start-up.

The UVLO comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, UVLO, V_{CC}, and V_{REF} are tied together.





VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: C_{VFO}, I_{VFO}, Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

$$\text{Frequency} = I_{VFO}/(C_{VFO} * 1V).$$

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the I_{VFO} pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

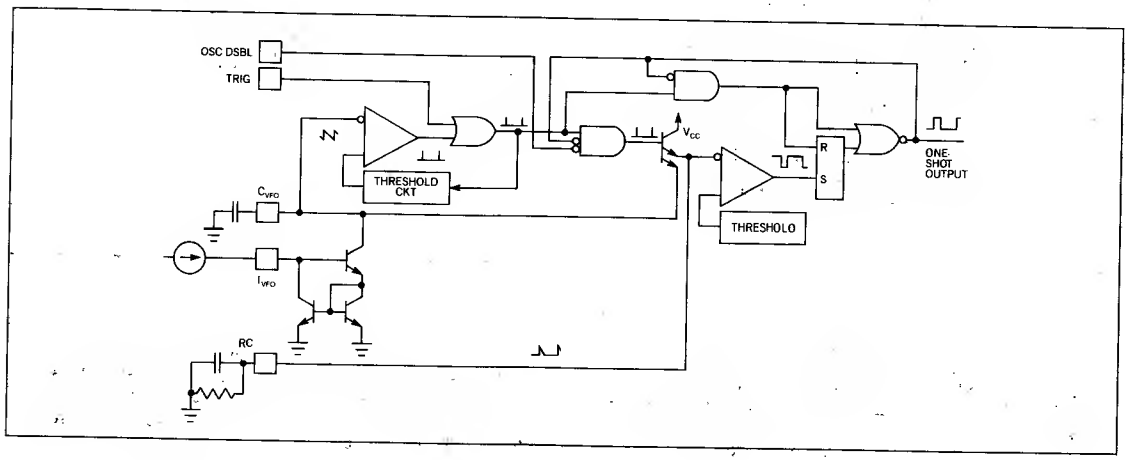
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

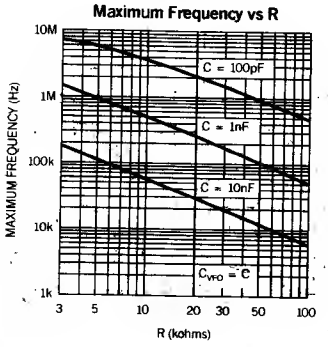
ONE SHOT TIMER

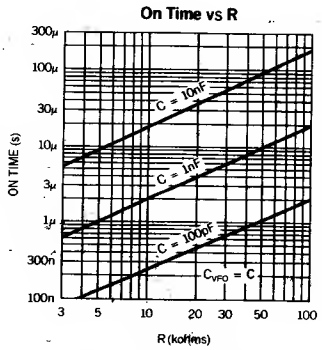
The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

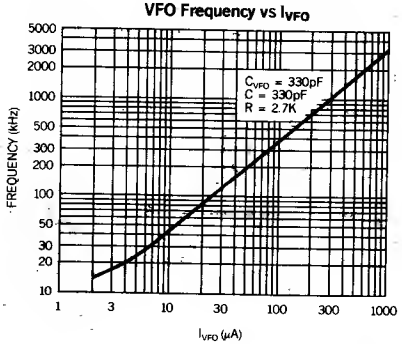
$$t(on) = 0.2 * R * C.$$

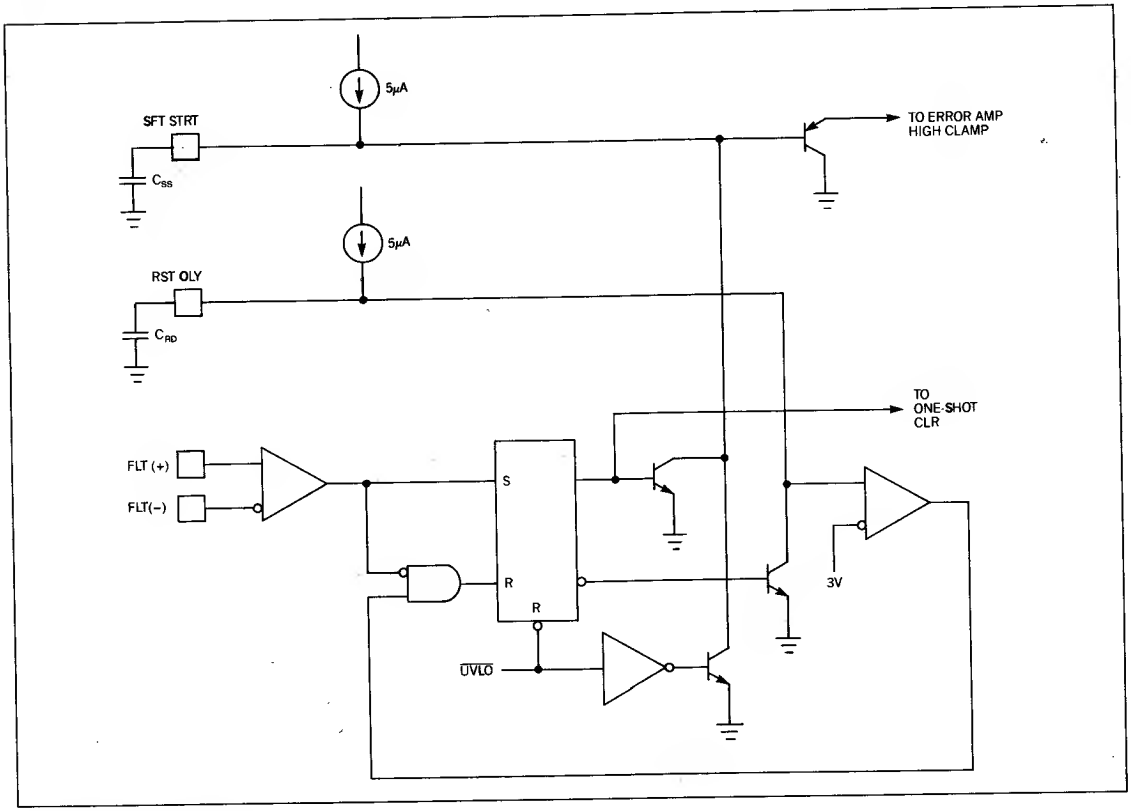
After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.











FAULT MANAGEMENT SECTION

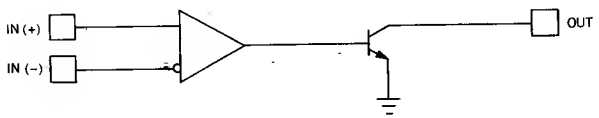
During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

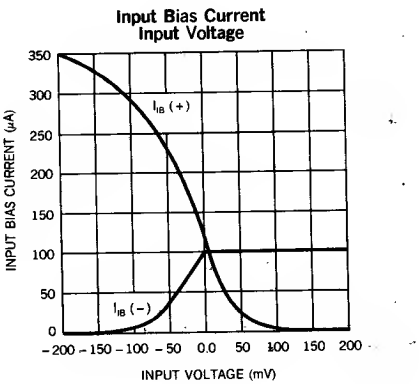
The high speed fault comparator will work over the input common mode range of –0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

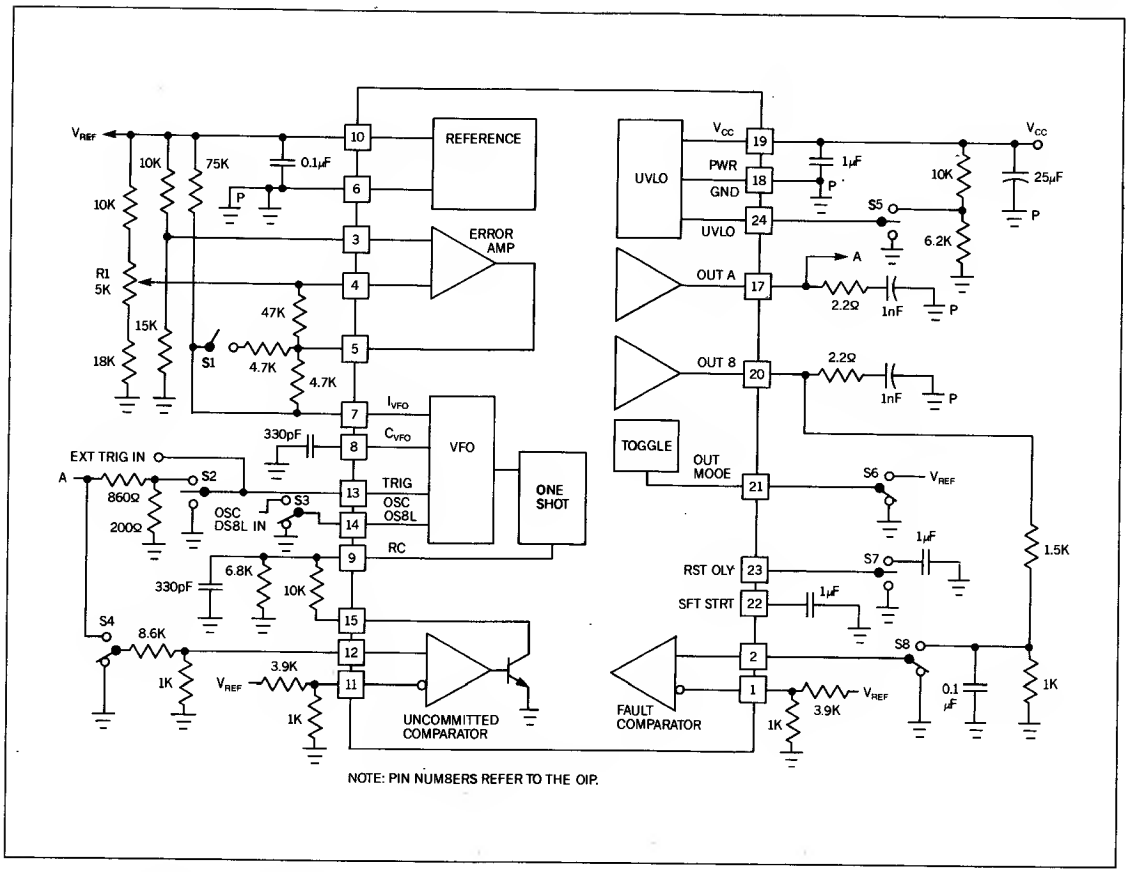
t (off) = 600 kohm * C(Rst Dly).

UNCOMMITTED COMPARATOR

The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of –0.3 to 3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.







OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.
Open the I_{VFO} resistor switch (S1).
Throw the Trig switch (S2) to ground.
Throw the Osc Dsbl switch (S3) to ground.
Throw the uncommitted comparator switch (S4) to ground.
Throw the UVLO switch (S5) to the resistive divider.
Throw the Out Mode switch (S6) to ground.
Open the restart delay switch (S7).
Throw the fault switch (S8) to ground.

In this configuration, the chip will operate for V_{CC} greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0 to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie. A, B, off, . . .).

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the V_{CC} start and stop thresholds are 17 and 10V. Switched to the resistive divider, the thresholds are approximately 12 and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

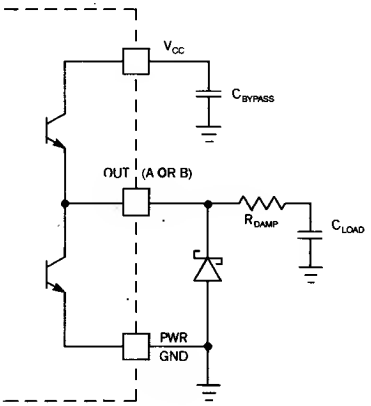
S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, V_{CC}, or opening the switch. Connected to 1 μF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

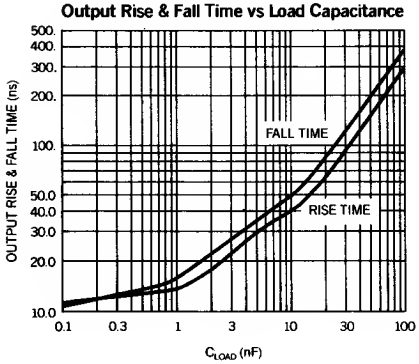
OUTPUT STAGE

The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

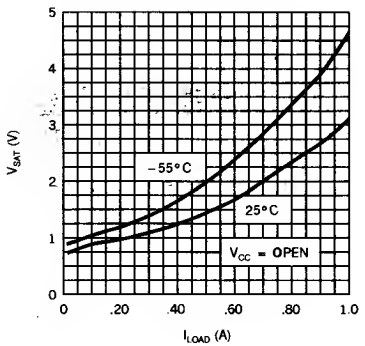
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of dI/dt. This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed ± 0.2V from signal ground.



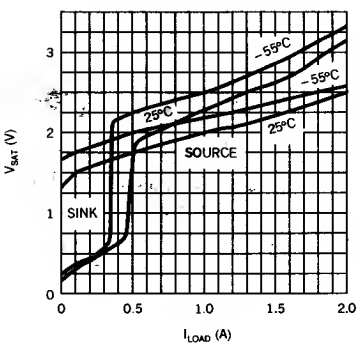
Output Rise & Fall Time vs Load Capacitance



Output Saturation Voltage vs Load Current



Output Saturation Voltage vs Load Current



BYPASS NOTE

The reference should be bypassed with a 0.1 μF ceramic capacitor from the V_{REF} pin directly to the ground plane near the Signal Ground pin. The timing capacitors on C_{VFO} and RC should be treated likewise. V_{CC}, however, should be bypassed with a ceramic capacitor from the V_{CC} pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.

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UC1861/64/65
UC2861/64/65
UC3861/64/65

Resonant-Mode Power Supply Controllers

PRELIMINARY

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) quasi-resonant converters
- Zero-crossing terminated one-shot timer
- Precision 1%, soft-started 5V reference
- Programmable restart delay following fault
- Voltage-Controlled Oscillator (VCO) with programmable minimum and maximum frequencies from 10 kHz to 1 MHz
- Low start-up current (150 µA typ.)
- Dual 1 Amp peak FET drivers
- UVLO option for off-line or DC/DC applications

Device	UVLO	Outputs	'Fixed'
1861	16/10	Alternating	Off Time
1864	9/7	Parallel	On Time
1865	16/10	Alternating	Off Time

Other variations of this series can be

DESCRIPTION

The UC1861/64/65 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865), or off-time for ZVS applications (UC1861/64).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

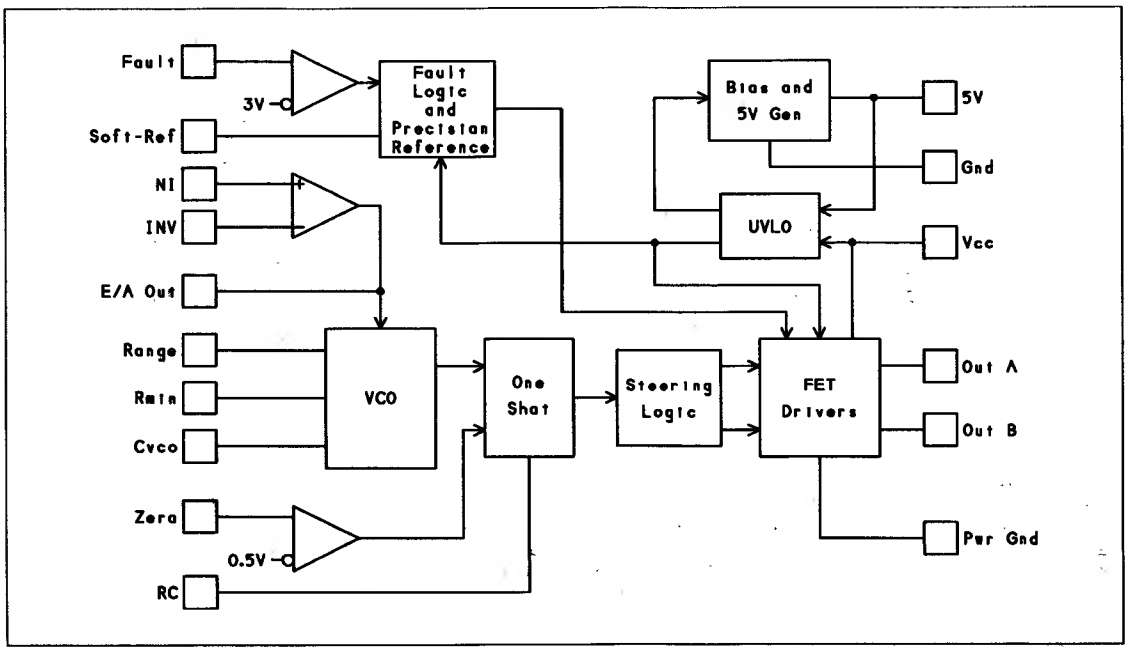
Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150 uA, and the outputs are actively forced to the low state. UVLO thresholds for the UC1861 and UC 1865 are 16V (ON) and 10V (OFF), whereas the UC1864 thresholds are 8V (ON) and 7V (OFF). After Vcc exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/65 devices. The UC1864 outputs operate in unison alllowing 2 Amp peak current.

Options other than the three outlined in this data sheet can be obtained from this family of control IC's. Consult the factory for further information.

BLOCK DIAGRAM



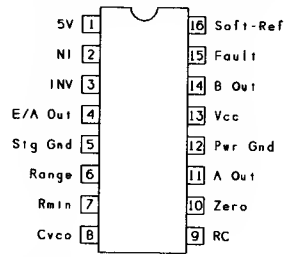
ABSOLUTE MAXIMUM RATINGS

Vcc 22V
Output Current, Source or Sink (Pins 11 & 14) DC 0.5A
Pulse (0.5μs) 1.5A
Power Ground Volage . . . . . ±0.2V
Inputs (Pins 2, 3, 10, & 13) . . . . . –0.4 to 7V
Error Amp Output Current . . . . . ±2mA
Power Dissipation at $T_A \leq 50^oC$ (N & Q package) 1W
Derate 10mW/^{o}C for $T_A > 50^oC$
Power Dissipation at $T_A \leq 70^oC$ (J package) 1W
Derate 12.5mW/^{o}C for $T_A > 70^oC$
Power Dissipation at $T_A \leq 80^oC$ (L package) 1W
Derate 14.3mW/^{o}C for $T_A > 80^oC$.
Junction Temperature (Operating) . . . . . 150^{o}C
Lead Temperature (Soldering, 10 seconds) . . . . . 300^{o}C

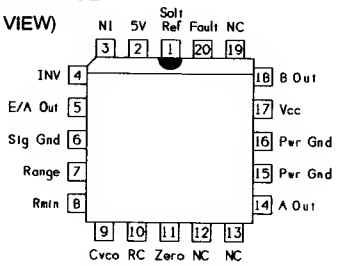
Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages.

CONNNECTION DIAGRAM

J or N PACKAGE (TOP VIEW)



Q or L PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications apply for $-55^oC \leq T_A \leq 125^oC$ for the UC18xx, $-25^oC \leq T_A \leq 85^oC$ for the UC28xx, and $0^oC \leq T_A \leq 70^oC$ for the UC38xx, VCC=12V, Cvco=1nF, Range=7.5K, Rmin=91K, C=200pF, R=4.3K, and Csr=0.1μF. $T_A = T_j$

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
5 VOLT GENERATOR					
Output Voltage	12V≤Vcc≤20V, –10mA≤Io≤0mA	4.8	5.0	5.2	V
Short Circuit Current	Vo=0V	–150		–15	mA
SOFT-REFERENCE					
Restart Delay Current	V=2V	10	20	35	μA
Soft Start Current	V=2V	–650	–500	–350	μA
Reference Voltage	T_J=25°C, Io=0	4.95	5.00	5.05	V
Reference Voltage	12V≤Vcc≤20V, –200μA≤Io≤200μA	4.85		5.15	V
Line Regulation	12V≤Vcc≤20V		2	20	mV
Load Regulation	–200μA≤Io≤200μA		8	25	mV
ERROR AMPLIFIER (Note 3)					
Input Offset Voltage	Vcm=5V, Vo=2V, Io=0	–10		10	mV
Input Bias Current	Vcm=0V	–2.0	–0.3		μA
Voltage Gain	Vcm=5V, 0.5V≤Vo≤3.7V, Io=0	70	100		dB
Power Supply Rejection Ratio	Vcm=5V, Vo=2V, 12V≤Vcc≤20V	70	100		dB
Common Mode Rejection Ratio	0V≤Vcm≤6V, Vo=2V	70	100		dB
Vout Low	Vid=–100mV, Io=200μA		0.05	0.20	V
Vout High	Vid=100mV, Io=–200μA	4.0	4.3		V
Unity Gain Bandwidth		0.7	1.0		MHz

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
VOLTAGE CONTROLLED OSCILLATOR					
Maximum Frequency	Vid (Error Amp)=100mV, T_J=25oC	450	500	550	kHz
Maximum Frequency	Vid (Error Amp)=100mV	425		575	kHz
Minimum Frequency	Vid (Error Amp)=–100mV, T_J=25oC	45	50	55	kHz
Minimum Frequency	Vid (Error Amp)=–100mV	42		58	kHz
ONE SHOT					
Zero Comparator Vth		0.45	0.50	0.55	V
Propogation Delay	(Note 4)		100	200	ns
Maximum Pulse Width	Vzero=1V	900	1000	1100	ns
Maximum to Minimum Pulse Width Ratio	Vzero=0V	5	6	7	
OUTPUT STAGE					
Rise and Fall Time	Cload=1nF (Note 4)		30	60	ns
Output Low Saturation	Io=20mA		0.2	0.4	V
Output Low Saturation	Io=200mA		0.5	2.2	V
Output High Saturation	Io=–20mA, down from Vcc		1.5	2.0	V
Output High Saturation	Io=–200mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	Io=20mA		0.8	1.5	V
FAULT COMPARATOR					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns
UVLO					
Vcc Turn-on Threshold	UCxx61, UCxx65	15	16	17	V
Vcc Turn-on Threshold	UCxx64	7.2	8.0	8.8	V
Vcc Turn-off Threshold	UCxx61, UCxx65	9	10	11	V
Vcc Turn-off Threshold	UCxx64	6.2	7.0	7.8	V
Icc Start	Vcc=Vcc(on)–0.3V		150	300	µA
Icc Run	Vid=100mV		20	30	mA

Note 1: Currents are defined as positive into the pin
Note 2: Pulse measurement techniques are used to insure that $T_J=T_A$
Note 3: Vid=V(NI)-V(INV)
Note 4: This parameter is not 100% tested in production but guaranteed by design.
Note 5: Vi= 0 to 4V, tr(Vi)≤ 10ns tpd=t(Vo=6V)-t(Vi=3V)

UVLO & 5V GENERATOR (See Figure 1)

When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300µA, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1uF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1)

The Soft-Ref pin serves three functions: System reference, restart delay, and soft-start. Designed to source or sink 200uA, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1µF. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source.

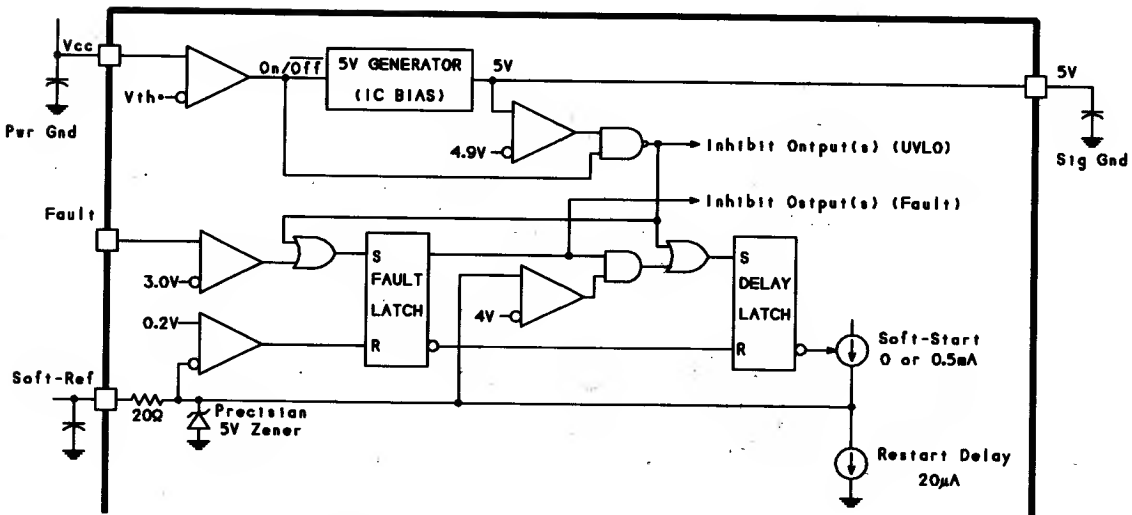
The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20µA. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20K or larger resistor from Soft-Ref to ground.

A 100K resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20µA current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

UVLO, 5V, Fault, and Soft-Ref



• UCX861 and UCX865 thresholds are 16V and 10V.
UCX864 thresholds are 8V and 7V.

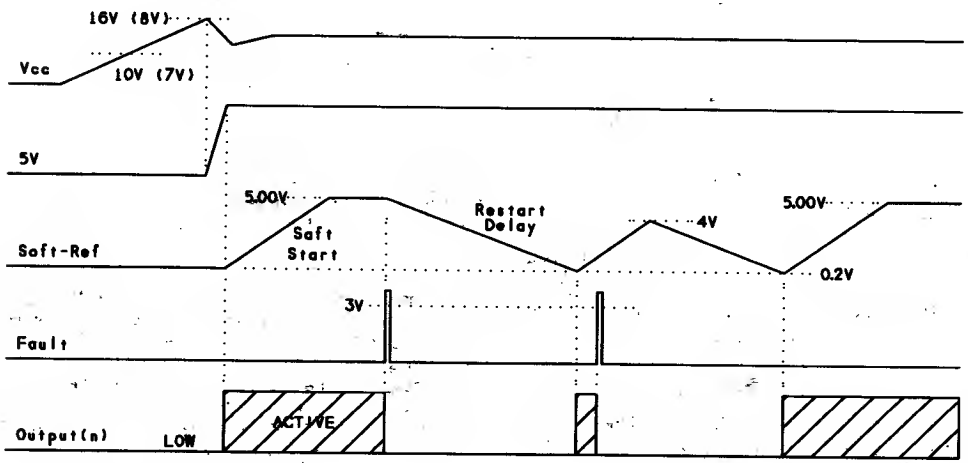


Figure 1

Error Amp, Voltage Controlled Oscillator, and One Shot

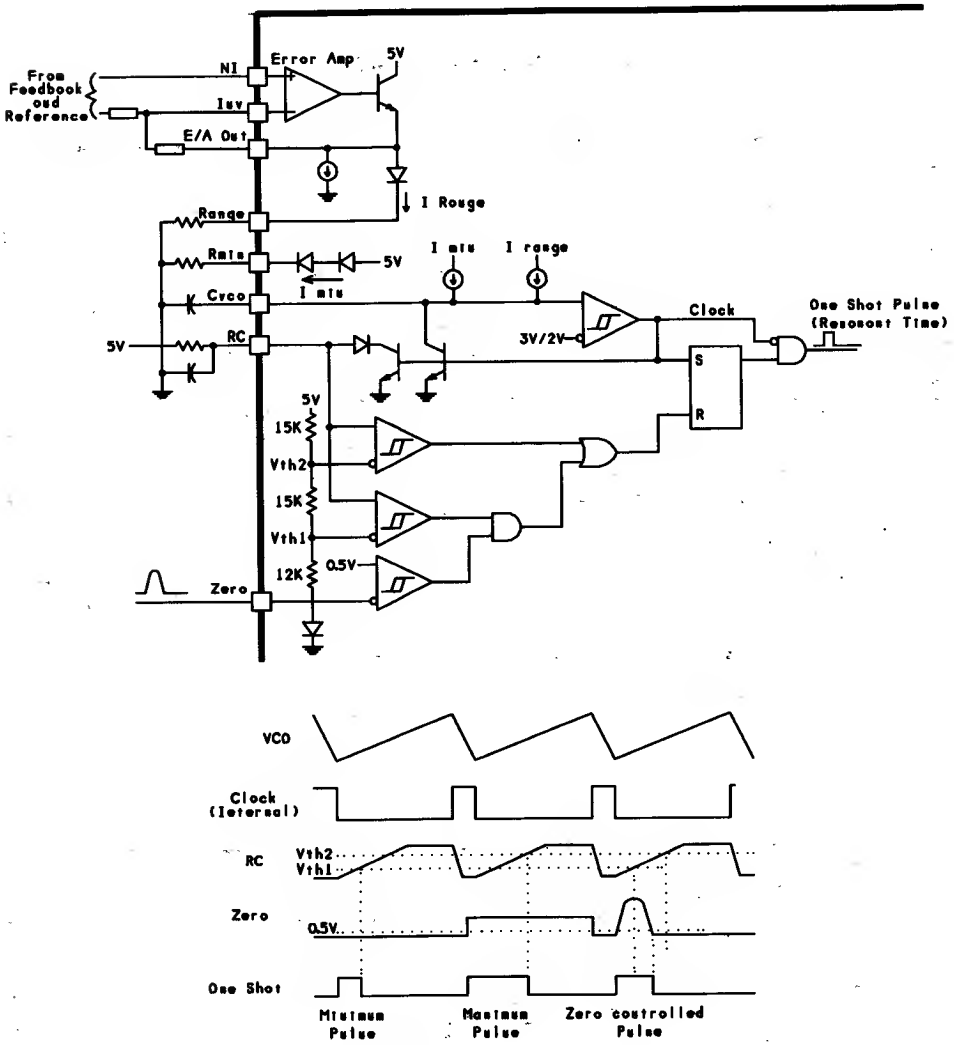


Figure 2

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$Fmin = \frac{4.5}{Rmin * Cvco}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$Fmax = \frac{3.6}{(Rmin||Range) * Cvco}$$

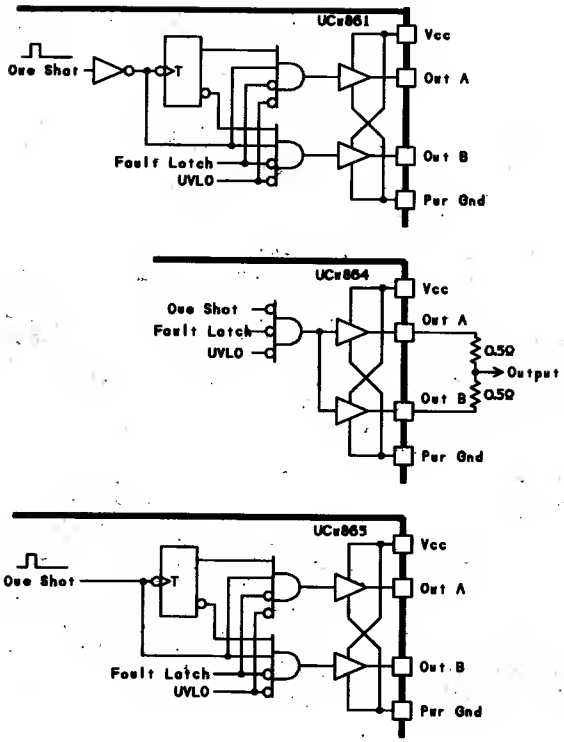
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tpw(min) = 0.2 * R * C.$$

The maximum pulse width is approximately given by:

$$Tpw(max) = 1.2 * R * C.$$

Steering Logic



The steering logic is configured on the UC1861 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.

The steering logic is configured on the UC1864 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

The steering logic is configured on the UC1865 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.

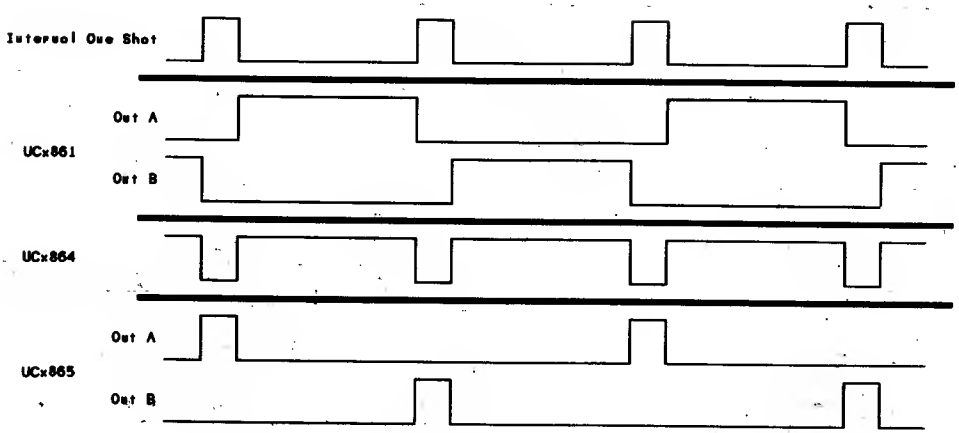


Figure 3

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INTEGRATED CIRCUITS

UNITRODE

UC1883
UC2883
UC3883

ISDN Primary Current Mode Controller

ADVANCED PRODUCT INFORMATION

GENERAL FEATURES

- Can Function as a General-purpose Low-power Controller
- Fully Synchronizing Oscillator
- Synchronization to Secondary-side Logic
- Leading Edge Blanking of Current Sense
- 50% Maximum Duty Cycle
- Undervoltage Lockout
- Programmable Low Line Sensing
- Programmable Softstart
- Programmable Fault/Restart Delay

ISDN FEATURES

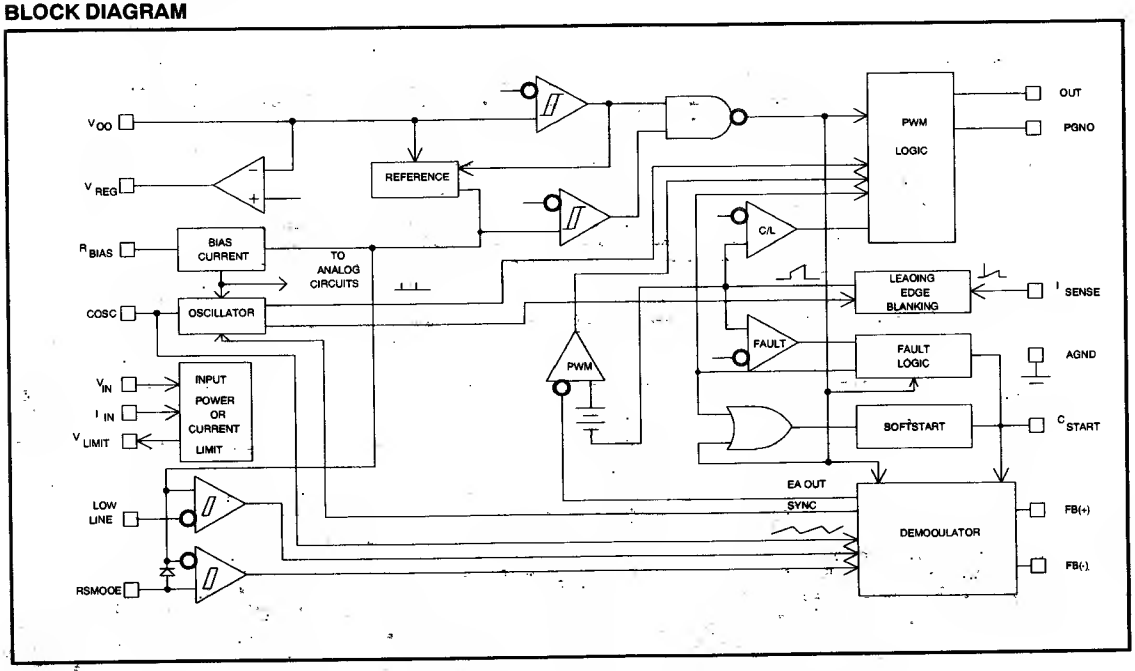
- Zero-power Startup Capability
- Restricted Mode Detection
- Frequency Agile PWM in Restricted Mode
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode
- Accurate, Programmable Input Power Limit or Input Current Limit

DESCRIPTION

The UC1883 primary-side current mode controller, in conjunction with the UC1885 secondary-side regulation IC, provides the necessary features to implement an ISDN-compatible SMPS with improved output regulation. The chip set is intended for use in DC/DC discontinuous flyback power converters, and an external power switch is required. Discontinuous flyback is the most economical scheme for developing multiple output voltages. Current mode control offers the advantage of pulse-by-pulse current limiting. The UC1885 regulation IC provides the feedback control voltage and oscillator synchronization via an isolating pulse transformer. The UC1883 uses this control voltage and frequency information in a conventional current mode PWM circuit. The leading edge blanking of the current sense waveform eliminates the need for an external filtering network on the I_{SENSE} input. An internal comparator provides pulse-by-pulse current limiting, and a catastrophic fault threshold is also maintained. If a fault is detected, the output is immediately disabled, and a programmable restart period occurs before a softstart sequence is initiated. The softstart ramp and restart delay may be independently programmed with an external resistor and capacitor, and a fixed softstart/restart delay ratio may be obtained with only a capacitor. Low input line sensing may also be programmed, in which case no output will occur until an appropriate input voltage is initially established.

ISDN-specific features allow the UC1883/UC1885 combination to be CCITT compatible. The linear regulator is intended to control a depletion-mode NMOS pass transistor. Startup power drawn from the line can be reduced to zero if a bootstrap winding provides power to the UC1883 V_{DD} pin. A dedicated comparator senses restricted mode from an external diode bridge. Maximum input power or input current may be accurately programmed and limited with an external PMOS pass transistor. The UC1883 operates at very low power levels to meet the 25mW restricted mode limit, but the user-programmable precision bias current allows flexible trading of operating frequency against quiescent power consumption. Finally, in restricted mode, the PWM becomes frequency agile, operating with a minimum pulse width determined by the leading edge blanking circuit. This improvement eliminates the spurious EMI generated if short output spikes are produced by the PWM.

BLOCK DIAGRAM



ISDN Secondary Regulation IC

ADVANCED PRODUCT INFORMATION

GENERAL FEATURES

- Wide Operating Range
- Fully Synchronizing Oscillator
- Temperature-stable Oscillator
- Logic Level Synchronization Input
- Precision Reference
- Error Amplifier for Loop Regulation and Compensation
- Undervoltage Lockout

ISDN FEATURES

- Low Line Logic Output
- Restricted Mode Logic Output
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode

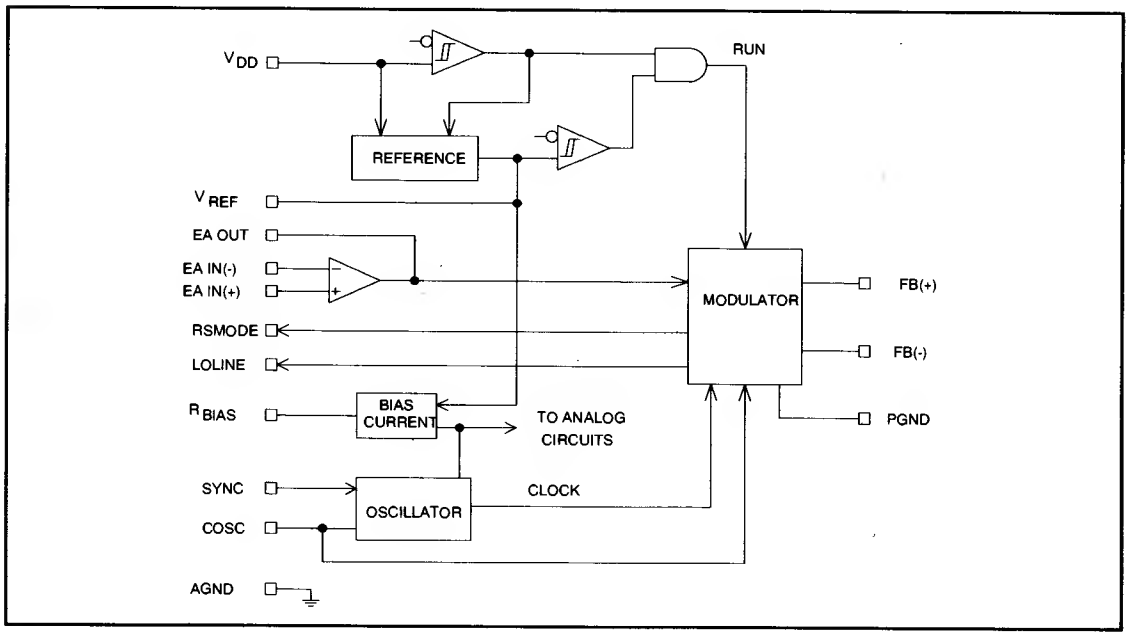
DESCRIPTION

The UC1885 secondary-side regulation IC provides improved output regulation by allowing DC sensing of the regulated output. When used in conjunction with the UC1883 primary-side PWM controller, the UC1885 supplies the necessary functions to implement an ISDN-compatible SMPS with full secondary isolation. The UC1885 contains a precision system reference and a complete error amplifier. The output of the amplifier serves as the PWM control voltage and is provided to the primary side via an isolating pulse transformer. The UC1885 also sends synchronization to the primary side with this transformer. Undervoltage lockout circuitry prevents transmission of data across the isolatioin barrier until adequate secondary-side operating conditions are established.

ISDN-specific features allow the UC 1833/UC1885 combination to be CCITT compatible. The UC1885 receives two digital bits of information from the UC1883 over the isolating pulse transformer. These bits, which indicate restricted power mode and low input line voltage, are output on the secondary-side at CMOS logic levels. Precision programming of the quiescent current used by the UC1885 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

4

BLOCK DIAGRAM



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INTEGRATED CIRCUITS

UNITRODE

Isolated Feedback Generator

UC1901
UC2901
UC3901

FEATURES

- An amplitude-modulation system for transformer coupling an isolated feedback error signal
- Low-cost alternative to optical couplers
- Internal 1% reference and error amplifier
- Internal carrier oscillator usable to 5MHz
- Modulator synchronizable to an external clock
- Loop status monitor

DESCRIPTION

The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

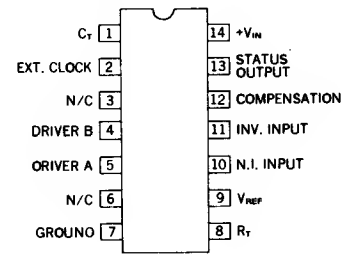
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN}	40V
Reference Output Current	-10mA
Driver Output Currents	-35mA
Status Indicator Voltage	40V
Status Indicator Current	20mA
Ext. Clock Input	40V
Error Amplifier Inputs	-0.5V to +35V
Power Dissipation at T_A = 25°C	
Derate at 10mW/°C above T_A = 50°C	1000mW
Power Dissipation at T_C = 25°C	
Derate at 16mW/°C above T_A = 25°C	2000mW
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

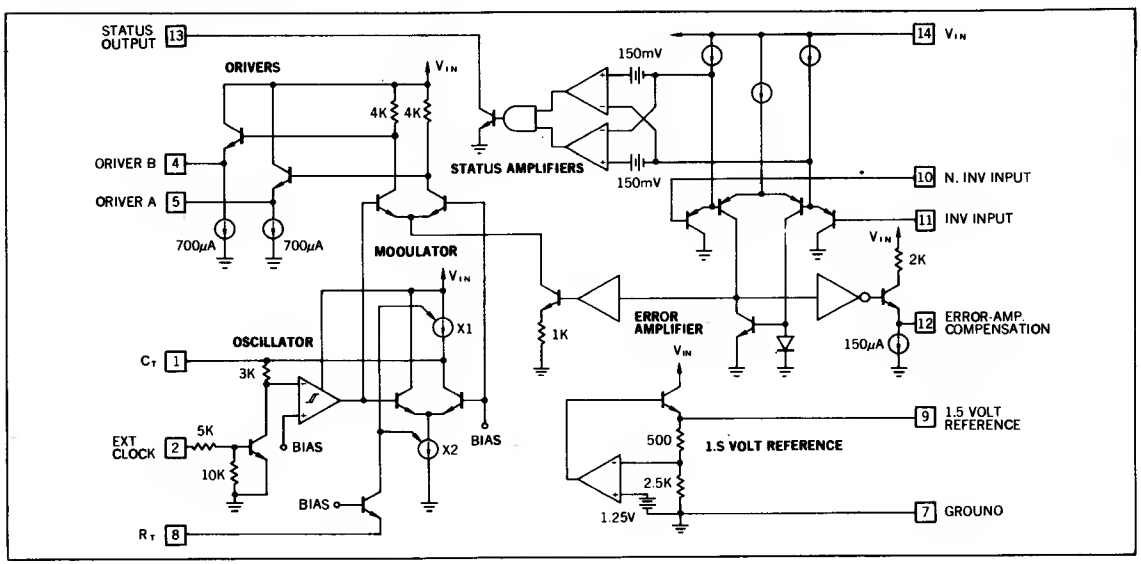
Note 1: Voltages are referenced to ground, Pin 7.
Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-14 (TOP VIEW)
J or N PACKAGE



UC1901 SIMPLIFIED SCHEMATIC

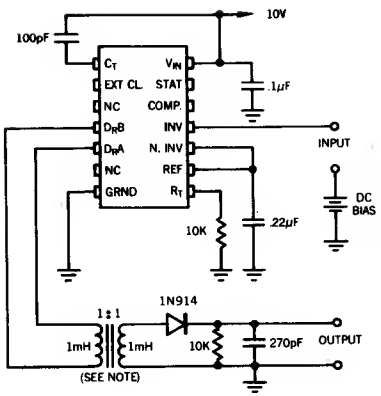


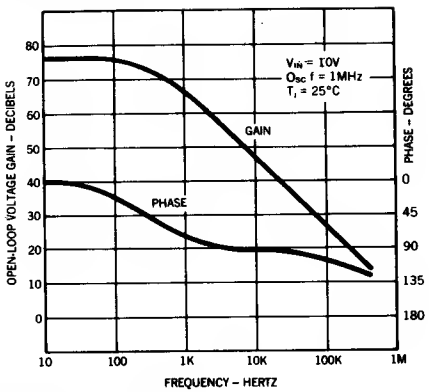
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1901; −25°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_j = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \le T_j \le T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_j = 25°C		−35	−55		−35	−55	mA
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		−1	−3		−1	−6	μA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	μA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 5 to 25V	80	100		80	100		dB
Output Swing, Δ V_O		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		μA
Maximum Source Current		−2	−3		−2	−3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/μs
Modulator/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V
Driver Sink Current		500	700		500	700		μA
Driver Source Current		−15	−35		−15	−35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_j = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \le T_j \le T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10K, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A Δ Input = 0.2V		.05	1		.05	5	μA
Supply Current	V_{IN} = 35V		5	8		5	10	mA

4

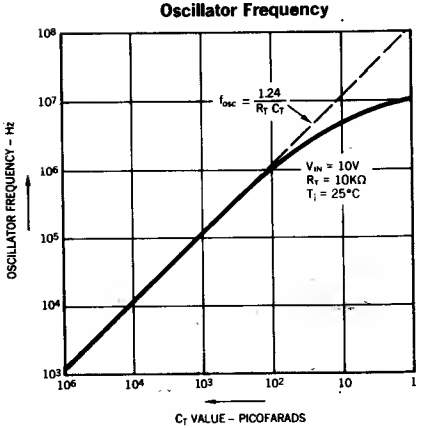
Transformer Coupled Open Loop Transfer Function



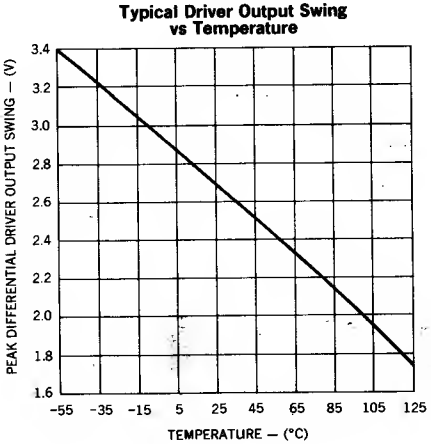


Transformer Data: N1 = N2 = 20T AWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O.D. toroid
Carrier Frequency = 1MHz

Oscillator Frequency



Typical Driver Output Swing vs Temperature



APPLICATION INFORMATION

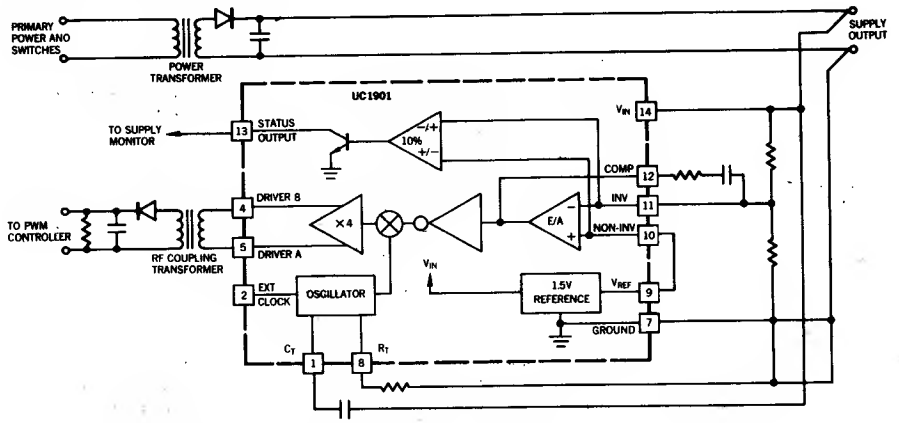
The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_T, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is no clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

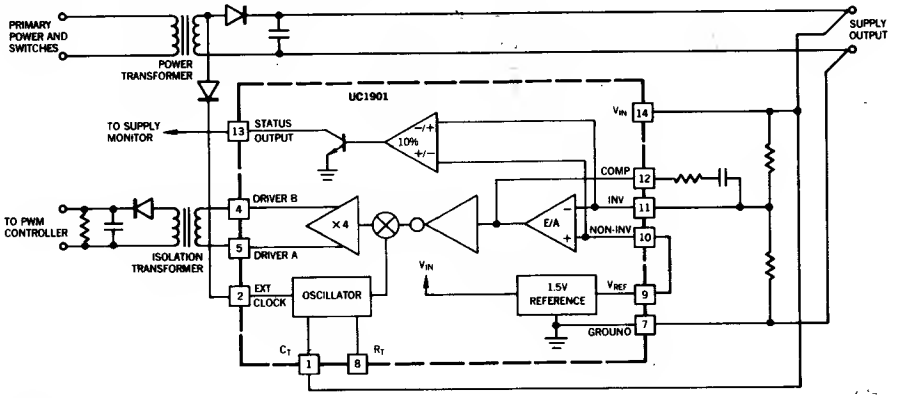
The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700μA, can be increased by adding resistors to ground at the driver outputs.

TYPICAL APPLICATIONS

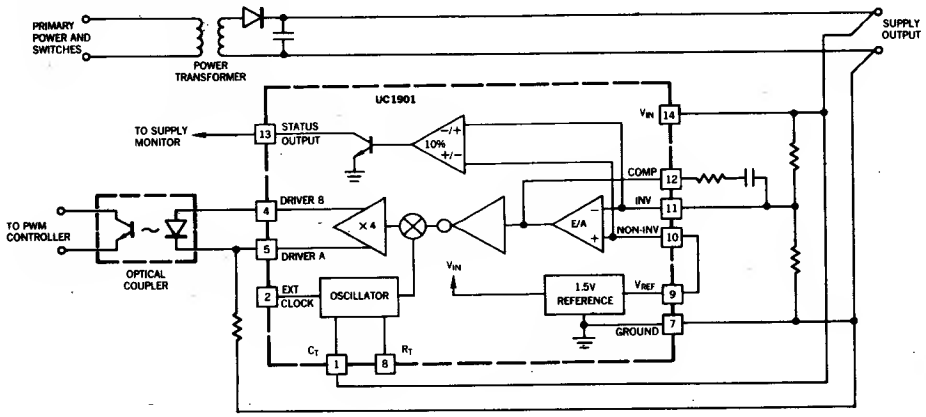
R.F. Transformer Coupled Feedback



Feedback Coupled at Switching Frequency



Optically Coupled DC Feedback



INTEGRATED CIRCUITS

UNITRODE

Quad Supply and Line Monitor

U1903
U2903
U3903

FEATURES

- Inputs for monitoring up to four separate supply voltage levels
- Internal inverter for sensing a negative supply voltage
- Line/switcher sense input for early power source failure warning
- Programmable under- and over-voltage fault thresholds with proportional hysteresis
- A precision 2.5V reference
- General purpose op-amp for auxillary use
- Three high current, >30mA, open-collector outputs indicate over-voltage, under-voltage and power OK conditions
- Input supply under-voltage sensing and start-latch eliminate erroneous fault alerts during start-up
- 8-40V supply operation with 7mA stand-by current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

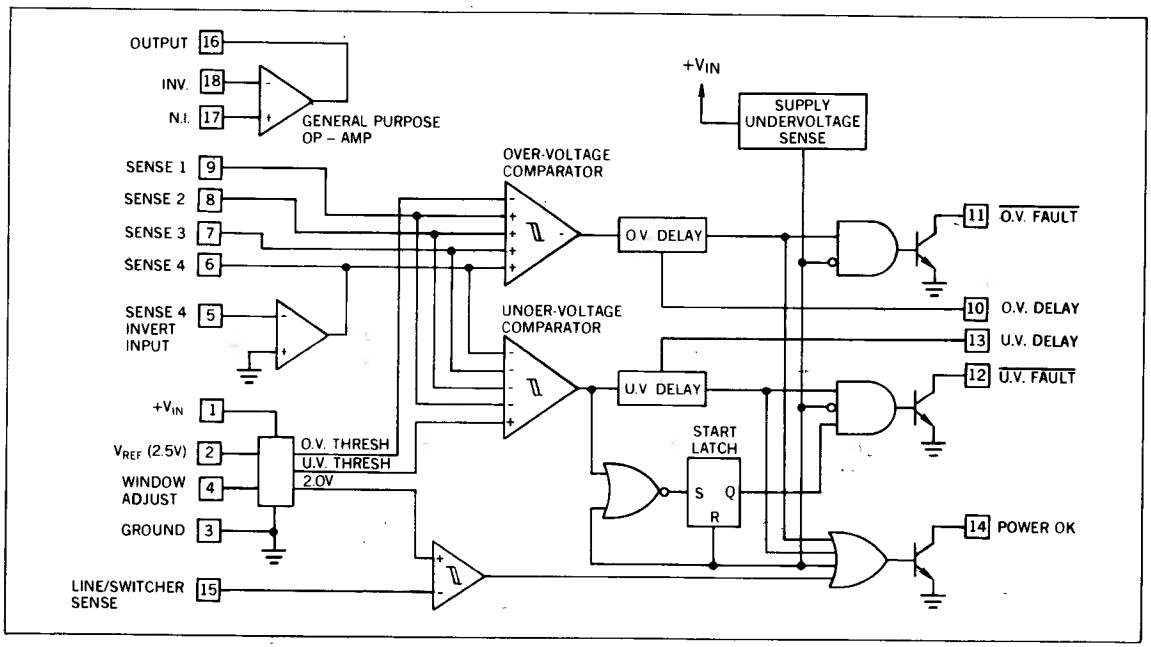
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8.40V input supple range and require a typical stand-by current of only 7mA.

BLOCK DIAGRAM



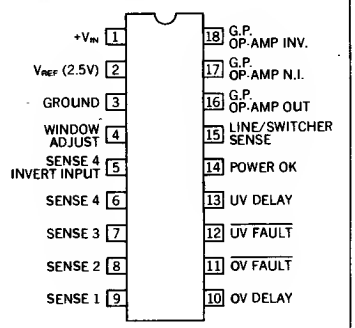
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) ..... +40V
Open Collector Output Voltages ..... +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages ..... -0.3V to +20V
Line/Switcher Sense Input Voltage ..... -0.3V to +40V
Op-Amp and Inverter Input Voltages ..... -0.3V to +40V
Op-Amp and Inverter Output Currents ..... -40mA
Window Adjust Voltage ..... 0.0V to +10V
Delay Pin Voltages ..... 0.0V to +5V
Reference Output Current ..... -40mA
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above T_A = 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above T_C = 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-18 (Top View)
J or N Package



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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1903; -25°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V.) T_A=T_J

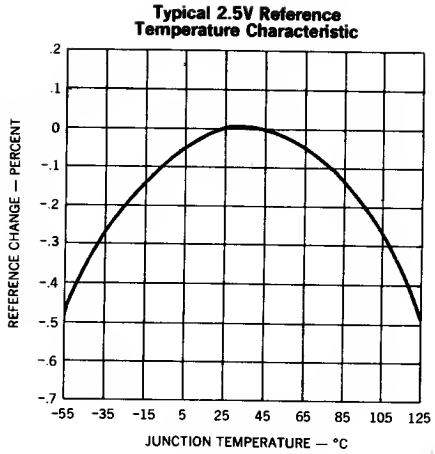
PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply								
Input Supply Current	No Faults	—	7	9	—	7	11	mA
	UV, OV and Line Fault	—	10	15	—	10	18	mA
Supply Under Voltage Threshold (V_{SUV})	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output		—	3.0	4.0	—	3.0	4.0	V
Reference								
Output Voltage (V_{REF})	T_j = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465	—	2.535	2.465	—	2.535	V
Load Regulation	I_L = 0 to 10mA	—	1	10	—	1	15	mV
Line Regulation	$+V_{IN}$ = 8 to 40V	—	1	4	—	1	8	mV
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA
Fault Thresholds								
OV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN4} Input = Low to High, .5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from V_{REF} as a function of V_{PIN4} Input = High to Low, .5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V
OV & UV Threshold Hyst.	.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = V_{SUV} +0.1V to 40V	—	.002	.01	—	.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	—	±1	±10	—	±1	±12	μA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV

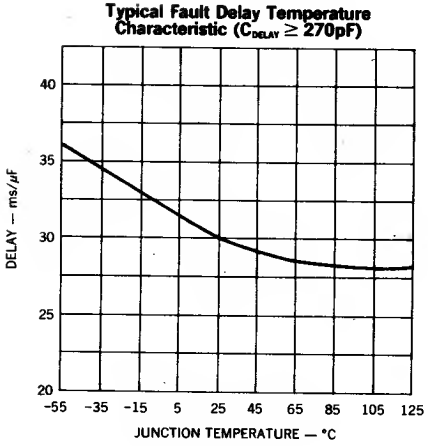
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1903; −25°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6-9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)	—	1	3	—	1	6	μA
	Input = 2.2V (Note 2)	—	-1	-3	—	-1	-6	μA
Line Sense Input Bias Current	Input = 2.3V (Note 2)	—	1	3	—	1	6	μA
OV and UV Fault Delay								
Charging Current		—	60	—	—	60	—	μA
Threshold Voltage	Delay Pin = Low to High	—	1.8	—	—	1.8	—	V
Threshold Hysteresis	T_j = 25°C	—	250	—	—	250	—	mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/μF
Fault Outputs ($\overline{OV}$, $\overline{UV}$, & Power OK)								
Maximum Current	V_{OUT} = 2V	30	70	—	30	70	—	mA
Saturation Voltage	I_{OUT} = 12mA	—	.25	.40	—	.25	.40	V
Leakage Current	V_{OUT} = 40V	—	3	25	—	3	25	μA
Sense 4 Inverter (Note 3)								
Input Offset Voltage		—	2	8	—	2	10	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Open Loop Gain		65	80	—	65	80	—	dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/μs
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA
G.P. Op-Amp (Note 3)								
Input Offset Voltage		—	1	5	—	1	8	mV
Input Bias Current		—	.1	2	—	.1	4	μA
Input Offset Current		—	.01	.5	—	.01	1.0	μA
Open Loop Gain		65	120	—	65	120	—	dB
CMRR	V_{CM} = 0 to $+V_{IN}$ −2.0V	65	100	—	65	100	—	dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100	—	65	100	—	dB
Unity Gain Frequency		—	1	—	—	1	—	MHz
Slew Rate		—	.4	—	—	.4	—	V/μs
Short Circuit Current	T_j = 25°C	—	40	—	—	40	—	mA

Note: 2. These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

Note: 3. When either the G.P. Op—Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.





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OPERATION AND APPLICATION INFORMATION

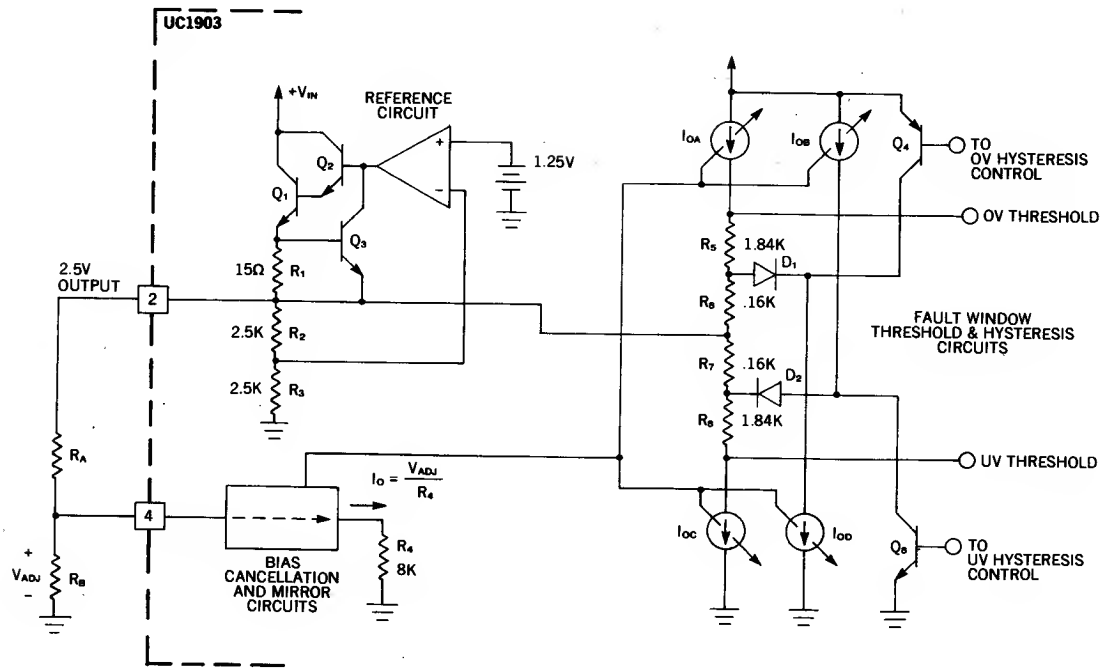

Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION (continued)

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, an 8K resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_6 are turned on. In combination with D_1 and D_2 this prevents I_{OB} and I_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_6)$ respectively. The fault window can be expressed as:

(1) $$2.5V \pm \frac{V_{ADJ}}{4}$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

(2) $$V_S \pm (10 \cdot V_{ADJ})\%$$

When a sense input moves outside the fault window given in equation (1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

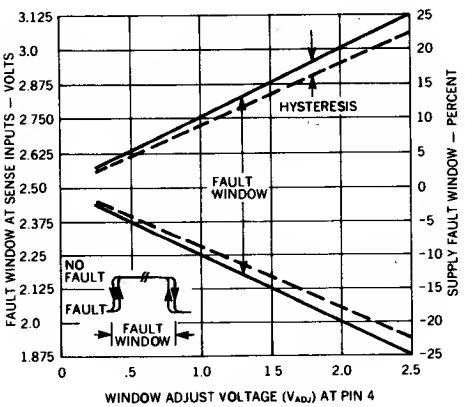

Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

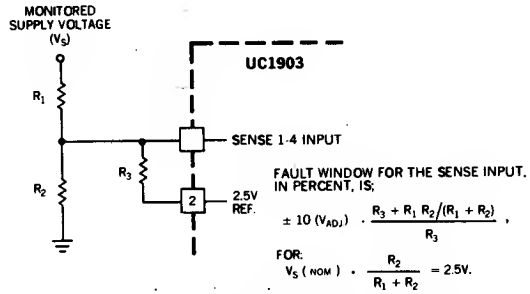

Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

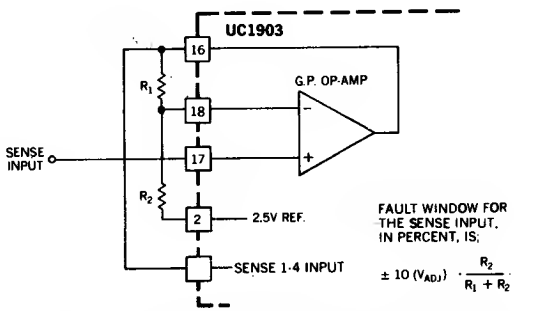

Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxillary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedence points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability, ≥20mA, while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

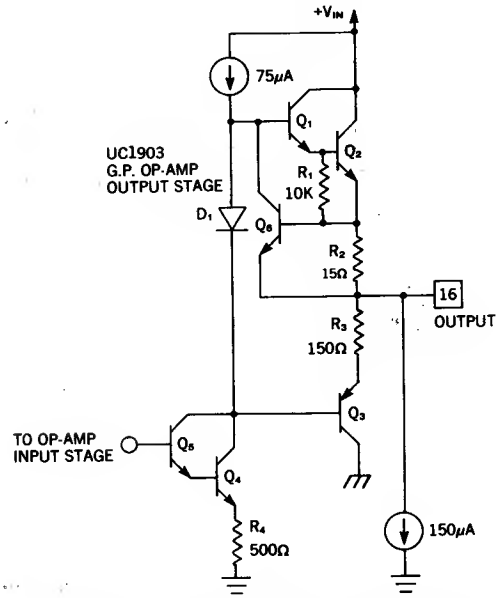

Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q_3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of this inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedence state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.

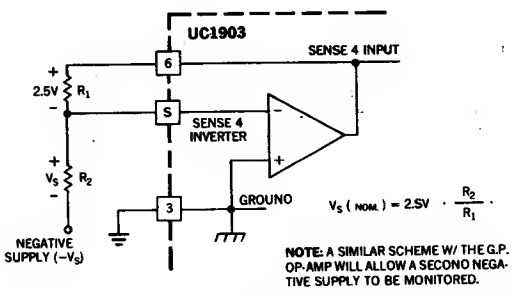

Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned-off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from

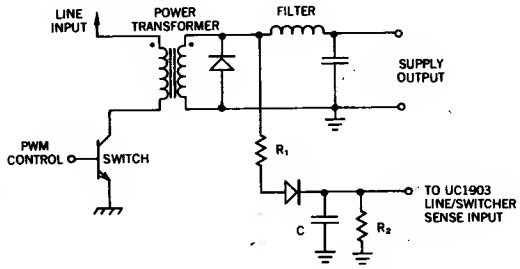

Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2K resistor, R_1, and zener diode, Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above −0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5K series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60μA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

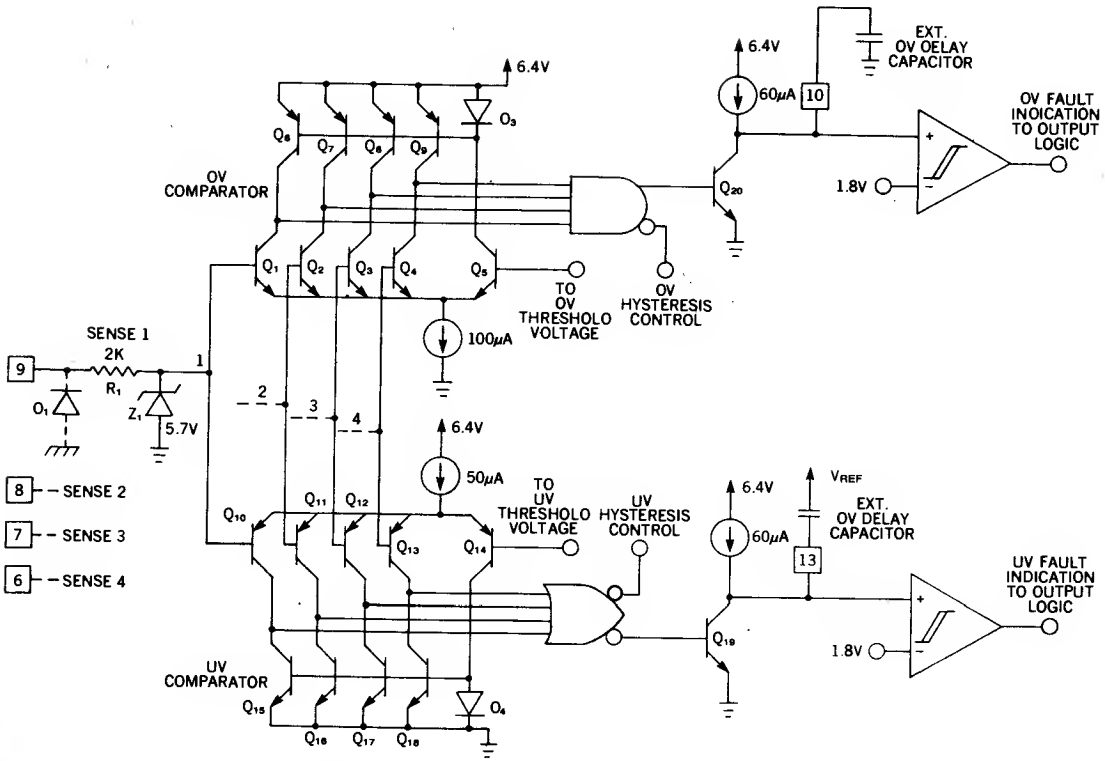

Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply ($+V_{IN}$) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With $+V_{IN}$ below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

Sealed Lead-Acid Battery Charger

FEATURES

- Optimum control for maximum battery capacity and life
- Internal state logic provides three charge states
- Precision reference tracks battery requirements over temperature
- Controls both voltage and current at charger output
- System interface functions
- Typical standby supply current of only 1.6mA

DESCRIPTION

The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply up to 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

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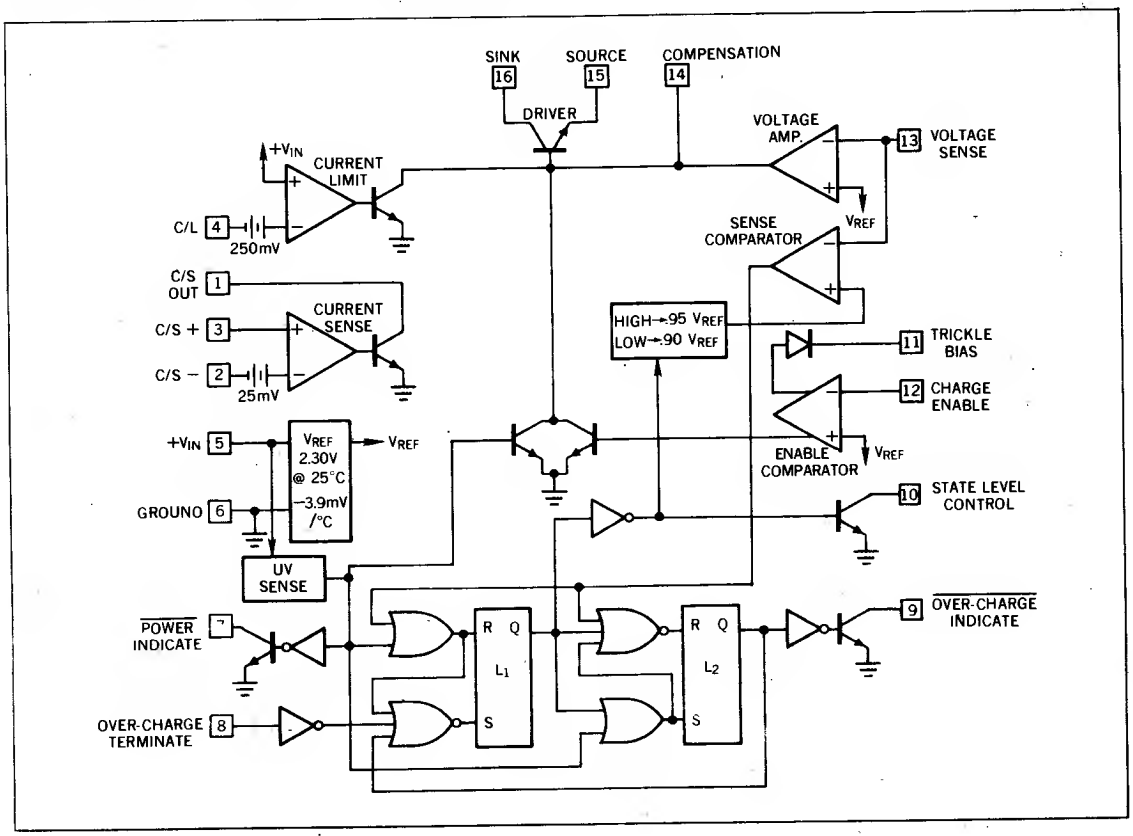
UC2906 BLOCK DIAGRAM



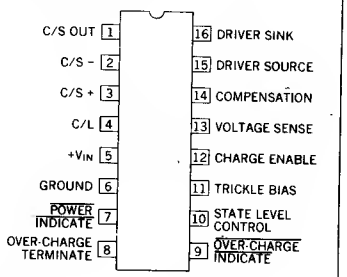
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{IN}$) 40V
Open Collector Output Voltages 40V
Amplifier and Comparator Input Voltages ..... -0.3V to +40V
Over-Charge Terminate Input Voltage ..... -0.3V to +40V
Current Sense Amplifier Output Current 40mA
Other Open Collector Output Currents 5mA
Trickle Bias Output Current ..... -40mA
Driver Current 40mA
Power Dissipation at T_A = 25°C
Derate at 10mW/°C Above T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C
Derate at 16mW/°C Above T_C = 25°C 2000mW
Thermal Resistance, Junction-to-Ambient ..... 100°C/W
Thermal Resistance, Junction-to-Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65° to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground (Pin 6).
Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V.) T_A=T_J

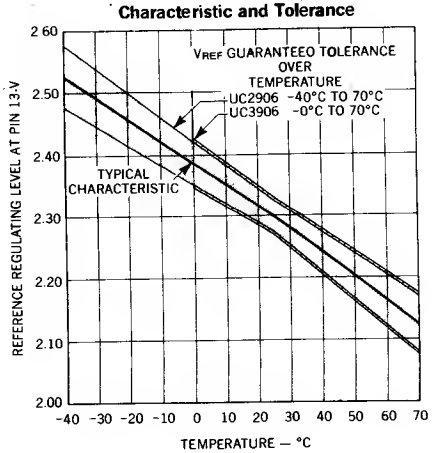
PARAMETER	TEST CONDITIONS	2906			3906			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Supply								
Supply Current	$+V_{IN}$ = 10V		1.6	2.5		1.6	2.5	mA
	$+V_{IN}$ = 40V		1.8	2.7		1.8	2.7	mA
Supply Under-Voltage Threshold	$+V_{IN}$ = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			.20	.30		.20	.30	V
Internal Reference (V_{REF})								
Voltage Level (Note 2)	Measured as Regulating Level At Pin 13 w/ Driver Current = 1mA, T_j = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	$+V_{IN}$ = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			-3.9			-3.9		mV/°C
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	-.5	-.2		-.5	-.2		μA
Maximum Output Current	Source	-45	-30	-15	-45	-30	-15	μA
	Sink	30	60	90	30	60	90	μA
Open Loop Gain	Driver Current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts Above GND or Below $+V_{IN}$		.2			.2		V
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, Io = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage	Driver Current = 10mA		.2	.45		.2	.45	V
Current Limit Amplifier								
Input Bias Current			.2	1.0		.2	1.0	μA
Threshold Voltage	Offset Below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		.03	.25		.03	.25	%/V

Note: 2. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V.) T_A=T_J

PARAMETER	TEST CONDITIONS		2906			3906			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Voltage Sense Comparator									
Threshold Voltage	As a Function of V_{REF}	L_1 = RESET	.945	.95	.955	.945	.95	.955	V/V
		L_1 = SET	.895	.90	.905	.895	.90	.905	V/V
Input Bias Current	Total Input Bias at Thresholds		−.5	−.2		−.5	−.2		μA
Current Sense Comparator									
Input Bias Current				.1	.5		.1	.5	μA
Input Offset Current				.01	.2		,01	.2	μA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA		20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V			.05	.35		.05	.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$			.05	.35		.05	.35	%/V
Maximum Output Current	V_{OUT} = 2V		25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA			.2	.45		.2	.45	V
Enable Comparator									
Threshold Voltage	As a Function of V_{REF}		.99	1.0	1.01	.99	1.0	1.01	V/V
Input Bias Current				−.5	−.2		−.5	−.2		μA
Trickle Bias Maximum Output Current	V_{OUT} = $+V_{IN}$ − 3V		25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts Below $+V_{IN}$, I_{OUT} = 10mA			2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = −10μA		6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input									
Threshold Voltage			.7	1.0	1.3	.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold			10			10		μA
Open Collector Outputs (Pins 7, 9 and 10)									
Maximum Output Current	V_{OUT} = 2V		2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA			.25	.45		.25	.45	V
	I_{OUT} = 50μA			.03	.05		.03	.05	V
Leakage Current	V_{OUT} = 40V			1	3		1	3	μA

Internal Reference Temperature Characteristic and Tolerance



OPERATION AND APPLICATION INFORMATION

Dual Level Float Charger Operation

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn-on mode. The output current of the charger is limited to a low level until the battery reaches a specified voltage, preventing high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn-on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor R_S.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, V_{OC}, during state 1 and state 2. When the battery voltage reaches 95% of V_{OC}, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, I_{OCT}. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the $\overline{\text{OVER-CHARGE INDICATE}}$ signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual level float charger is shown in Figure 3.

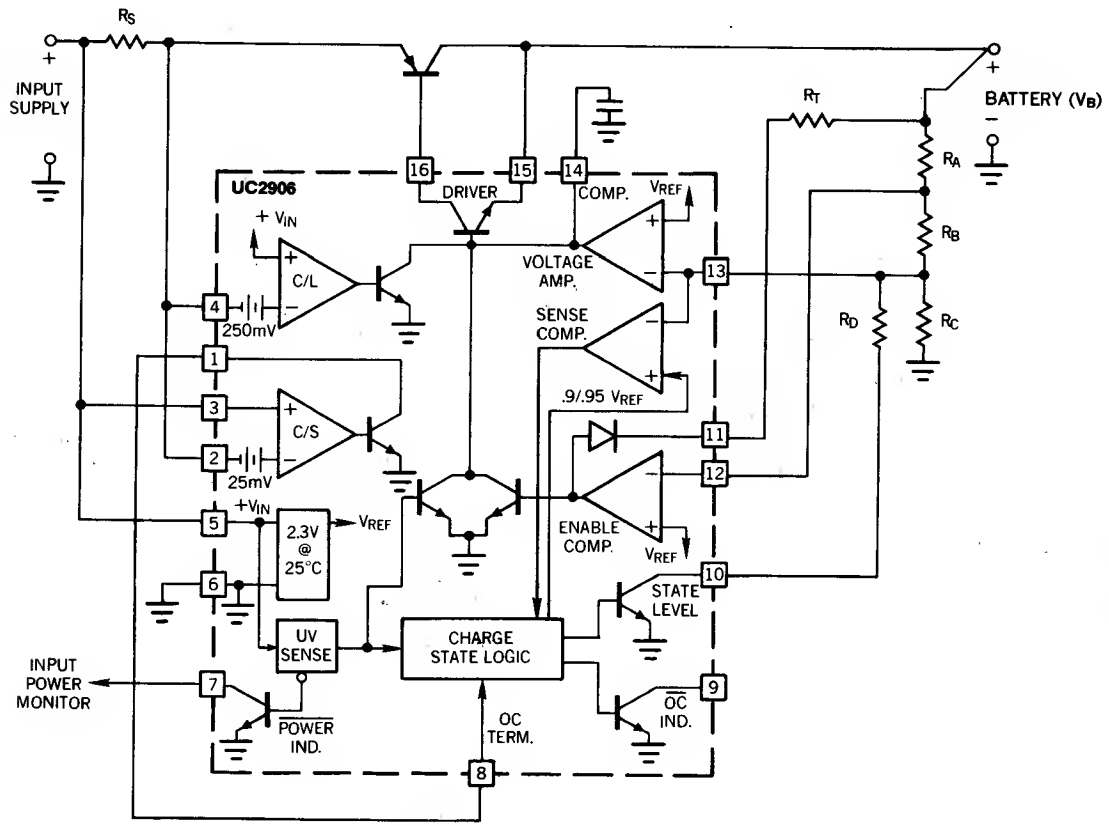
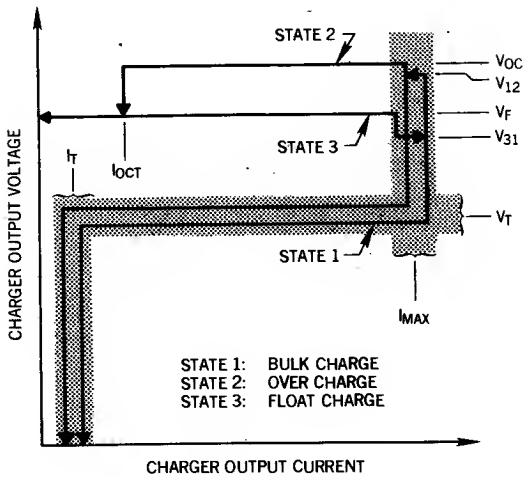


Figure 1. The UC2906 in a Dual Level Float Charger



Design procedure:

1.) Pick divider current, I_D. Recommended value is 50uA to 100uA.

2.) $R_C = 2.3V/I_D$.

3.) $R_A + R_B = R_{SUM} = (V_F - 2.3V)/I_D$

4.) $R_D = 2.3VR_{SUM}/(V_{OC} - V_F)$

5.) $R_A = (R_{SUM} + R_X)(1 - 2.3V/V_T)$
where: $R_X = R_C R_D/(R_C + R_D)$

6.) $R_B = R_{SUM} - R_A$

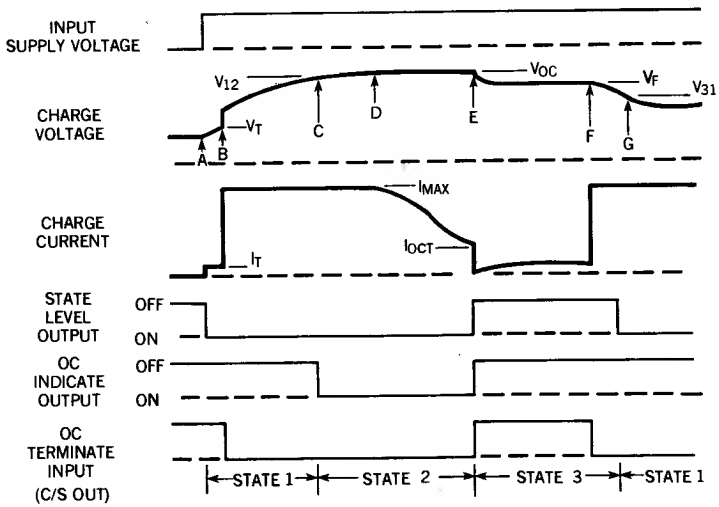
7.) $R_S = 0.25V/I_{MAX}$

8.) $R_T = (V_{IN} - V_T - 2.5V)/I_T$

NOTE: $V_{12} = 0.95V_{OC}$
$V_{31} = 0.90\ V_F$
$I_{OCT} = I_{MAX}/10$

For further design and application information see UICC Application Note U—104.

Figure 2. State Diagram and Design Equations For the Dual Level Float Charger



Explanation: Dual Level Float Charger

A. Input power turns on, battery charges at trickle current rate.

B. Battery voltage reaches V_T enabling the driver and turning off the trickle bias output, battery charges at I_{MAX} rate.

C. Transition voltage V_{12} is reached and the charger indicates that it is now in the over-charge state, state 2.

D. Battery voltage approaches the over-charge level V_{OC} and the charge current begins to taper.

E. Charge current tapers to I_{OCT}. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at V_F.

F. Here a load ($>I_{MAX}$) begins to discharge the battery.

G. The load discharges the battery such that the battery voltage falls below V_{31}. The charger is now in state 1, again.

Figure 3. Typical Charge Cycle: UC2906 Dual Level Float Charger

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, V_F. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, I_H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V_{12} is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the POWER INDICATE pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

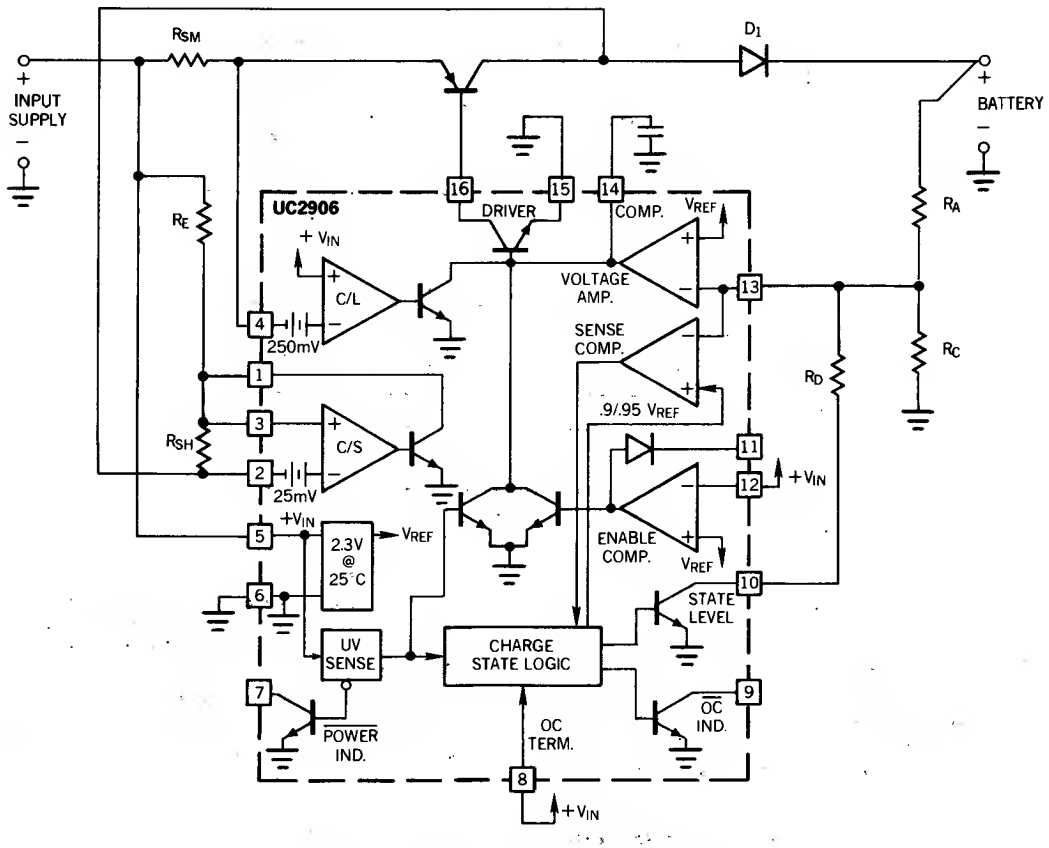
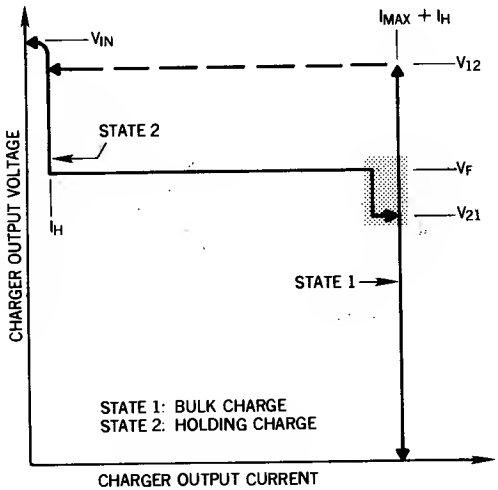


Figure 4. The UC2906 in a Dual Step Current Charger



1.) $V_{12} = .95\ V_{REF}\ (1 + \frac{R_A}{R_C} + \frac{R_A}{R_D})$

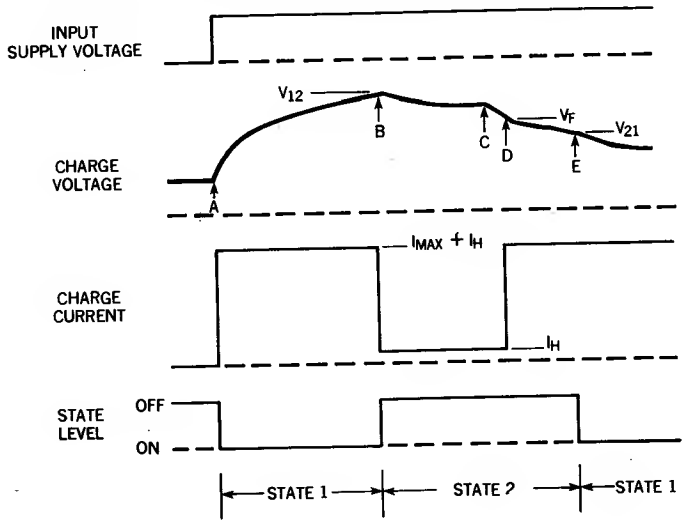
2.) $V_F = V_{REF}\ (1 + \frac{R_A}{R_C})$

3.) $V_{21} = .9\ V_F$

4.) $I_{MAX} = \frac{.25V}{R_{SM}}$

5.) $I_H = \frac{.025V}{R_{SH}}$

Figure 5. State Diagram and Design Equations for the Dual Step Current Charger



Explanation: Dual Step Current Charger

A. Input power turns on, battery charges at a rate of $I_H + I_{MAX}$.

B. Battery voltage reaches V_{12} and the voltage loop switches to the lower level V_F. The battery is now fed with the holding current I_H.

C. An external load starts to discharge the battery.

D. When V_F is reached the charger will supply the full current $I_{MAX} + I_H$.

E. The discharge continues and the battery voltage reaches V_{21} causing the charger to switch back to state 1.

Figure 6. Typical Charge Cycle: UC2906 Dual Step Current Charger

INTEGRATED CIRCUITS

UNITROODE

Three Terminal Fixed Voltage Positive Regulators

UC7800
UC7800C
SERIES

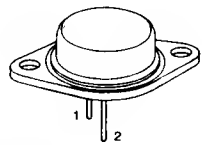
FEATURES

- Complete Specifications at 1A Load
- No External Components
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3, TO-220, TO-257, and isolated TO-257
- Output Voltages of 5V, 12V and 15V (For Other Voltages, Please Contact the Factory)

DESCRIPTION

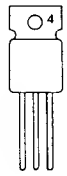
These three terminal monolithic positive voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7800 and 7800C series have output tolerances of ±4%. The 7800A and 7800AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

K(TO-3)



Pin 1, Adjust
2. Input
Case: Output

G, IG (TO-257)

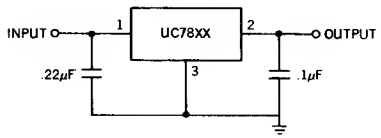


Non-isolated
Pin 1. Adjust
2. Input
3. Output
4. Output

Isolated
Pin 1. Adjust
2. Input
3. Output
4. No Connection

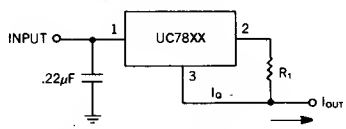
TYPICAL APPLICATIONS

Fixed Output Regulator



Notes: 1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stabilify, it does improve transient responses.
3. Input capacitor required if regulator is located an appreciable distance from power supply filter.

Current Regulator



$$I_{OUT} = \frac{V_{OUT}}{R_1} + I_Q$$

Note: When ordering, add "K" (for TO-3 package), "T" (for TO-220 package), "G" (for non-isolated TO-257) and "IG" (for isolated TO-257) to the part number

ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Power Dissipation ..... Internally limited
Operating Junction Temperature Range
UC7800 SERIES ..... −55°C to +150°C
UC7800C SERIES ..... 0°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds)
K (TO-3), G, IG (TO-257 Packages) ..... 300°C
T (TO-220) package ..... 230°C

Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package	G (TO-257) Package	IG (ISOLATED TO-257)
Rated Power @ 25°C				
T_C	20W	15W	15W	15W
T_A	4.3W	2W	3W	3W
Thermal Resistance				
θ_{JC}	3°C/W	5°C/W	3.5°C/W	4.2°C/W
θ_{JA}	35°C/W	60°C/W	42°C/W	42°C/W

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7805			UC7805C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 10V, I_O = 1A	4.8		5.2	4.8		5.2	V
	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	4.8		5.2	4.77		5.23	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	4.75		5.25	4.75		5.25	V
Line Regulation	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			25			35	mV
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$		10	50		10	50	mV
Load Regulation	T_j = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1.5A (Note 1)		20	26		20	40	mV
	V_{IN} = 10V, 5mA ≤ I_O ≤ 1A (Note 1) Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			50			50	mV
Quiescent Current	T_j = 25°C, V_{IN} = 10V, I_O = 1A		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.5			.5	mA
	T_j = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			.8			.8	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 8V ≤ V_{IN} ≤ 18V, I_O = 500mA	63			63			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 10V, I_O = 1A		40			40		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 10V		2.1			2.1		A
Peak Output Current	T_j = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 10V, I_O = 5mA		-.4			-.4		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 10V, I_O = 5mA		20			20		mV
Thermal Shutdown	V_{IN} = 10V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7812			UC7812C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 1A	11.52		12.48	11.52		12.48	V
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V 5mA ≤ I_{OUT} ≤ 1A, P_O ≤ 15W	11.52		12.48	11.46		12.54	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	11.40		12.60	11.40		12.60	V
Line Regulation	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			60			84	mV
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$		20	120		20	120	mV
Load Regulation	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1.5A (Note 1)		50	64		50	100	mV
	V_{IN} = 19V, 5mA ≤ I_O ≤ 1A Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$ (Note 1)			120			120	mV
Quiescent Current	T_j = 25°C, V_{IN} = 19V, I_O = 1A		4.5	7		4.5	7	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.5			.5	mA
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			.8			.8	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 15V ≤ V_{IN} ≤ 25V, I_O = 500mA	56			56			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 5mA		75			75		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 19V		1.5			1.5		A
Peak Output Current	T_j = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 19V, I_O = 5mA		-.8			-.8		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 19V, I_O = 5mA		50			50		mV
Thermal Shutdown	V_{IN} = 19V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10ms$, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7815			UC7815C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 1A	14.4		15.6	14.4		15.6	V
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	14.4		15.6	14.3		15.7	V
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$	14.25		15.75	14.25		15.75	V
Line Regulation	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			75			100	mV
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$		22	150		22	150	mV
Load Regulation	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1.5A (Note 1)		50	80		50	120	mV
	V_{IN} = 23V, 5mA ≤ I_O ≤ 1A Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$ (Note 1)			150			150	mV
Quiescent Current	T_j = 25°C, V_{IN} = 23V, I_O = 1A		4.5	7		4.5	7	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			.5			.5	mA
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			.8			.8	mA
	Over Temperature, $T_{MIN} \leq T_j \leq T_{MAX}$			1.0			1.0	mA
Ripple Rejection	T_j = 25°C, 18.5V ≤ V_{IN} ≤ 28.5V, I_O = 500mA	54			54			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 5mA		90			90		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 23V		1.2			1.2		A
Peak Output Current	T_j = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 23V, I_O = 5mA		-1.0			-1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 23V, I_O = 5mA		60			60		mV
Thermal Shutdown	V_{IN} = 23V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \leq 10ms$, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX		
	K (TO-3)	G (TO-257)	IG (ISOLATED TO-257)
5V	UC7805K UC7805CK	UC7805G UC7805CG	UC7805IG UC7805CIG
12V	UC7812K UC7812CK	UC7812G UC7812CG	UC7812IG UC7812CIG
15V	UC7815K UC7815CK	UC7815G UC7815CG	UC7815IG UC7815CIG

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INTEGRATED CIRCUITS

UNITRODE

Three Terminal Fixed Voltage Positive Regulators

UC7800A
UC7800AC
SERIES

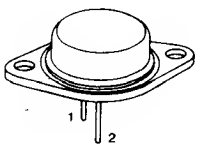
FEATURES

- ±1% Output Voltage on 7800A, AC Series
- Complete Specifications at 1A Load
- No External Components
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3, TO-220, TO-257, and isolated TO-257
- Output Voltages of 5V, 12V and 15V. (For Other Voltages, Please Contact the Factory)

DESCRIPTION

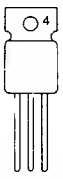
These three terminal monolithic positive voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7800 and 7800C series have output tolerances of ±4%. The 7800A and 7800AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

K(TO-3)



Pin 1. Adjust
2. Input
Case: Output

G, IG (TO-257)

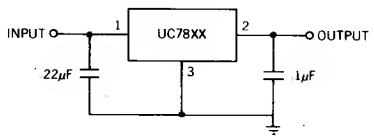


Non-isolated
Pin 1. Adjust
2. Input
3. Output
4. Output

Isolated
Pin 1. Adjust
2. Input
3. Output
4. No Connection

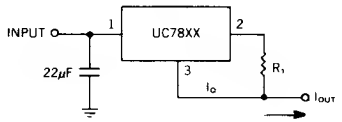
TYPICAL APPLICATIONS

Fixed Output Regulator



Notes: 1 To specify an output voltage, substitute voltage value for "XX".
2 Although no output capacitor is needed for stability, it does improve transient responses.
3 Input capacitor required if regulator is located an appreciable distance from power supply filter.

Current Regulator



$$I_{OUT} = \frac{V_{OUT}}{R_1} + I_O$$

Note: When ordering, add "K" (for TO-3 package), "T" (for TO-220 package), "G" (for non-isolated TO-257) and "IG" (for isolated TO-257) to the part number

ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Power Dissipation ..... Internally limited
Operating Junction Temperature Range
UC7800 SERIES ..... -55°C to +150°C
UC7800C SERIES ..... 0°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds)
K (TO-3), G, IG (TO-257 Packages) ..... 300°C
T (TO-220) package ..... 230°C
Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package	G (TO-257) Package	IG (ISOLATED TO-257)
Rated Power @ 25°C				
T_C	20W	15W	15W	15W
T_A	4.3W	2W	3W	3W
Thermal Resistance				
θ_{JC}	3°C/W	5°C/W	3.5°C/W	4.2°C/W
θ_{JA}	35°C/W	60°C/W	42°C/W	42°C/W

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7805A			UC7805AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_J = 25°C, V_{IN} = 10V, I_O = 1A	4.95		5.05	4.95		5.05	V
	T_J = 25°C, 7.5V ≤ V_{IN} ≤ 20V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	4.9		5.1	4.87		5.13	V
	Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$	4.85		5.15	4.85		5.15	V
Line Regulation	T_J = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			5			6	mV
	Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$		3	10		3	10	mV
Load Regulation	T_J = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1.5A (Note 1)		10	12		10	17	mV
	V_{IN} = 10V, 5mA ≤ I_O ≤ 1A (Note 1) Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$			25			25	mV
Quiescent Current	T_J = 25°C, V_{IN} = 10V, I_O = 1A		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_J = 25°C, V_{IN} = 10V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$			.5			.5	mA
	T_J = 25°C, 7.5V ≤ V_{IN} ≤ 20V, I_O = 500mA			.6			.6	mA
	Over Temperature, $T_{MIN} \le T_J \le T_{MAX}$			.8			.8	mA
Ripple Rejection	T_J = 25°C, 8V ≤ V_{IN} ≤ 18V, I_O = 500mA	69			69			dB
Output Noise Voltage	T_J = 25°C, V_{IN} = 10V, I_O = 1A		40			40		μV
Dropout Voltage	T_J = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_J = 25°C, V_{IN} = 10V		2.1			2.1		A
Peak Output Current	T_J = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ $T_J \le T_{MAX}$, V_{IN} = 10V, I_O = 5mA		-.4			-.4		mV/°C
Long Term Stability	1000 Hrs. @ T_J = 125°C, V_{IN} = 10V, I_O = 5mA		20			20		mV
Thermal Shutdown	V_{IN} = 10V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7812A			UC7812AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 1A	11.88		12.12	11.88		12.12	V
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	11.76		12.24	11.70		12.30	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	11.64		12.36	11.64		12.36	V
Line Regulation	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			12			15	mV
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$		4	18		4	18	mV
Load Regulation	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1.5A (Note 1)		12	32		12	50	mV
	V_{IN} = 19V, 5mA ≤ I_O ≤ 1A Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$ (Note 1)			60			60	mV
Quiescent Current	T_j = 25°C, V_{IN} = 19V, I_O = 1A		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 19V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.5			.5	mA
	T_j = 25°C, 14.5V ≤ V_{IN} ≤ 27V, I_O = 500mA			.6			.6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.8			.8	mA
Ripple Rejection	T_j = 25°C, 15V ≤ V_{IN} ≤ 25V, I_O = 500mA	62			62			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 19V, I_O = 5mA		75			75		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 19V		1.5			1.5		A
Peak Output Current	T_j = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 19V, I_O = 5mA		-.8			-.8		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 19V, I_O = 5mA		50			50		mV
Thermal Shutdown	V_{IN} = 19V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10ms$, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7815A			UC7815AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 1A	14.85		15.15	14.85		15.15	V
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V 5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W	14.7		15.3	14.60		15.40	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	14.55		15.45	14.55		15.45	V
Line Regulation	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			15			19	mV
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$		4	22		4	22	mV
Load Regulation	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1.5A (Note 1)		12	35		12	50	mV
	V_{IN} = 23V, 5mA ≤ I_O ≤ 1A Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$ (Note 1)			75			75	mV
Quiescent Current	T_j = 25°C, V_{IN} = 23V, I_O = 1A		4.5	6		4.5	6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			6.5			6.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = 23V, 5mA ≤ I_O ≤ 1A			.4			.4	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.5			.5	mA
	T_j = 25°C, 17.5V ≤ V_{IN} ≤ 30V, I_O = 500mA			.6			.6	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			.8			.8	mA
Ripple Rejection	T_j = 25°C, 18.5V ≤ V_{IN} ≤ 28.5V, I_O = 500mA	60			60			dB
Output Noise Voltage	T_j = 25°C, V_{IN} = 23V, I_O = 5mA		90			90		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2			2		V
Short Circuit Current	T_j = 25°C, V_{IN} = 23V		1.2			1.2		A
Peak Output Current	T_j = 25°C		2.4			2.4		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = 23V, I_O = 5mA		-1.0			-1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = 23V, I_O = 5mA		60			60		mV
Thermal Shutdown	V_{IN} = 23V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX		
	K (TO-3)	G (TO-257)	IG (ISOLATED TO-257)
5V	UC7805AK UC7805ACK	UC7805AG UC7805ACG	UC7805AIG UC7805ACIG
12V	UC7812AK UC7812ACK	UC7812AG UC7812ACG	UC7812AIG UC7812ACIG
15V	UC7815AK UC7815ACK	UC7815AG UC7815ACG	UC7815AIG UC7815ACIG

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INTEGRATED CIRCUITS

UNITRODE

UC7900
UC7900C

Three Terminal Fixed Voltage Negative Regulators

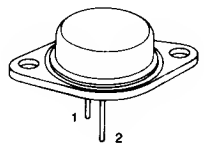
FEATURES

- Output Current to 1.5A
- One External Component
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3, TO-220, TO-257, and isolated TO-257
- Output Voltages of −5V, −12V and −15V (For Other Voltages, Please Contact the Factory)

DESCRIPTION

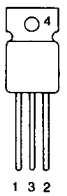
These three terminal monolithic negative voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7900 and 7900C series have output tolerances of ±4%. The 7900A and 7900AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

K(TO-3)



Pin 1. Adjust
2. Input
Case: Output

G, IG (TO-257)



Non-isolated
Pin 1. Adjust
2. Input
3. Output
4. Output

Isolated
Pin 1. Adjust
2. Input
3. Output
4. No Connection

ABSOLUTE MAXIMUM RATINGS

Input Voltage	−35V
Input-Output Voltage Differential	30V
Power Dissipation	Internally limited
Operating Junction Temperature Range	
UC7900A SERIES	−55°C to +150°C
UC7900AC SERIES	0°C to +125°C
UC7900 SERIES	−55°C to +150°C
UC7900C SERIES	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
K (TO-3), G, IG, (TO-257) package	300°C
T (TO-220) package	230°C

Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package	G (TO-257) Package	IG (Isolated TO-257)
Rated Power @ 25°C				
T_C	20W	15W	15W	15W
T_A	4.3W	2W	3W	3W
Thermal Resistance				
θ_{JC}	3°C/W	5°C/W	3.5°C/W	4.2°C/W
θ_{JC}	35°C/W	60°C/W	42°C/W	42°C/W

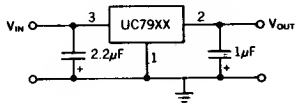
Note: When ordering, add suffix "K" (for TO-3 package), "T" (for TO-220 package), "G" (for non-isolated TO-257) and "IG" (for isolated TO-257) to the part number.

TYPICAL APPLICATIONS

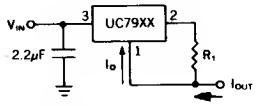
Input bypass capacitors are recommended for stable operation of the UC7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



Basic Current Regulator



$$I_{OUT} = \frac{V_{OUT}}{R_1} + I_o$$

ELECTRICAL CHARACTERISTICS $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC7905			UC7905C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = −10V, I_O = 5mA	−5.20		−4.80	−5.20		−4.80	V
	T_j = 25°C, −25V ≤ V_{IN} ≤ −8V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_O	−5.20		−4.80	−5.23		−4.77	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	−5.25		−4.75	−5.25		−4.75	V
Line Regulation	T_j = 25°C, −25V ≤ V_{IN} ≤ −7V, I_O = 5mA		25	50		25	50	mV
Load Regulation	T_j = 25°C, V_{IN} = −10V, 5mA ≤ I_O ≤ 1.5A (Note 1)			50			100	mV
Quiescent Current	T_j = 25°C, V_{IN} = −10V, I_O = 500mA		1	2.5		1	2.5	mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			3			3	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = −10V, 5mA ≤ I_O ≤ 1.5A			1.0			1.0	mA
	T_j = 25°C, −25V ≤ V_{IN} ≤ −8V, I_O = 500mA			.5			.5	mA
Ripple Rejection	T_j = 25°C, −18V ≤ V_{IN} ≤ −8V, I_O = 500mA	54			54			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = −10V, I_O = 500mA		100			100		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2.0			2.0		V
Short Circuit Current	T_j = 25°C, V_{IN} = −10V		1.8			1.8		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = −10V, I_O = 5mA		−.4			−.4		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = −10V, I_O = 5mA		20			20		mV
Thermal Shutdown	V_{IN} = −10V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le$ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately. P_D = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min $|V_O - V_{IN}|$ @ −55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7912			UC7912C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = -17V, I_O = 5mA	-12.48		-11.52	-12.48		-11.52	V
	T_j = 25°C, -32V ≤ V_{IN} ≤ -14V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_O	-12.48		-11.52	-12.54		-11.46	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	-12.60		-11.40	-12.60		-11.40	V
Line Regulation	T_j = 25°C, -32V ≤ V_{IN} ≤ -14V, I_O = 5mA		30	80		30	80	mV
Load Regulation	T_j = 25°C, V_{IN} = -17V, 5mA ≤ I_O ≤ 1.5A (Note 1)			120			240	mV
Quiescent Current	T_j = 25°C, V_{IN} = -17V, I_O = 500mA		3			3		mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = -17V, 5mA ≤ I_O ≤ 1.5A			.8			.8	mA
	T_j = 25°C, -32V ≤ V_{IN} ≤ -14V, I_O = 500mA			.5			.5	mA
Ripple Rejection	T_j = 25°C, -25V ≤ V_{IN} ≤ -15V, I_O = 500mA	56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = -17V, I_O = 500mA		200			200		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = -17V		1.3			1.3		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = -17V, I_O = 5mA		-.9			-.9		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = -17V, I_O = 5mA		48			48		mV
Thermal Shutdown	V_{IN} = -17V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
P_D = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min $|V_O - V_{IN}|$ @ -55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7915			UC7915C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = -20V, I_O = 5mA	-15.60		-14.40	-15.60		-14.40	V
	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	-15.60		-14.40	-15.68		-14.32	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	-15.75		-14.25	-15.75		-14.25	V
Line Regulation	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V, I_O = 5mA		35	100		35	100	mV
Load Regulation	T_j = 25°C, V_{IN} = -20V, 5mA ≤ I_O ≤ 1.5A (Note 1)			150			300	mV
Quiescent Current	T_j = 25°C, V_{IN} = -20V, I_O = 500mA		3			3		mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = -20V, 5mA ≤ I_O ≤ 1.5A			.8			.8	mA
	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V, I_O = 500mA			.5			.5	mA
Ripple Rejection	T_j = 25°C, -28V ≤ V_{IN} ≤ -18V, I_O = 500mA	56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = -17V, I_O = 500mA		250			250		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = -20V		1.1			1.1		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ $T_j \le T_{MAX}$, V_{IN} = -20V, I_O = 5mA		-1.0			-1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = -20V, I_O = 5mA		60			60		mV
Thermal Shutdown	V_{IN} = -20V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
P_D = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min $|V_O - V_{IN}|$ @ -55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX		
	K (TO-3)	G (TO-257)	IG (ISOLATED TO-257)
-5V	UC7905AK UC7905ACK	UC7905G UC7905CG	UC7905IG UC7905CIG
-12V	UC7912AK UC7912ACK	UC7912G UC7912CG	UC7912IG UC7912CIG
-14V	UC7915AK UC7915ACK	UC7915G UC7915CG	UC7915IG UC7915CIG

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INTEGRATED CIRCUITS

UNITRODE

UC7900A
UC7900AC

Three Terminal Fixed Voltage Negative Regulators

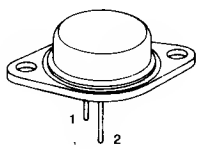
FEATURES

- ±1% Output Voltage on 7900A, AC Series
- Output Current to 1.5A
- One External Component
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Available in TO-3, TO-220, TO-257, and isolated TO-257
- Output Voltages of −5V, −12V and −15V (For Other Voltages, Please Contact the Factory)

DESCRIPTION

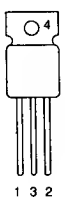
These three terminal monolithic negative voltage regulators employ internal current limiting, thermal shutdown and safe area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A of output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The 7900 and 7900C series have output tolerances of ±4%. The 7900A and 7900AC series offer ±1% tolerances on initial output voltage and, in addition, are specified to provide better regulator performance.

K(TO-3)



Pin 1. Adjust
2. Input
Case: Output

G, IG (TO-257)



Non-isolated
Pin 1. Adjust
2. Input
3. Output
4. Output

Isolated
Pin 1. Adjust
2. Input
3. Output
4. No Connection

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... −35V
Input-Output Voltage Differential 30V
Power Dissipation ..... Internally limited
Operating Junction Temperature Range
- UC7900A SERIES ..... −55°C to +150°C
- UC7900AC SERIES ..... 0°C to +125°C
- UC7900 SERIES ..... −55°C to +150°C
- UC7900C SERIES ..... 0°C to +125°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds)
- K (TO-3), G, IG, (TO-257) package ..... 300°C
- T (TO-220) package ..... 230°C

Power/Thermal Characteristics

	K (TO-3) Package	T (TO-220) Package	G (TO-257) Package	IG (Isolated TO-257)
Rated Power @ 25°C				
T_C	20W	15W	15W	15W
T_A	4.3W	2W	3W	3W
Thermal Resistance				
θ_{JC}	3°C/W	5°C/W	3.5°C/W	4.2°C/W
θ_{JC}	35°C/W	60°C/W	42°C/W	42°C/W

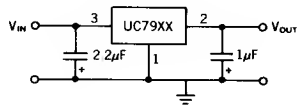
Note: When ordering, add suffix "K" (for TO-3 package), "T" (for TO-220 package), "G" (for non-isolated TO-257) and "IG" (for isolated TO-257) to the part number.

TYPICAL APPLICATIONS

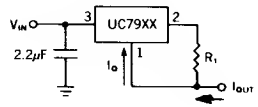
Input bypass capacitors are recommended for stable operation of the UC7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



Basic Current Regulator



$$I_{OUT} = \frac{V_{OUT}}{R_1} + I_o$$

ELECTRICAL CHARACTERISTICS T_A=T_J

PARAMETER	TEST CONDITIONS	UC7905A			UC7905AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = -10V, I_O = 5mA	-5.05		-4.95	-5.05		-4.95	V
	T_j = 25°C, -25V ≤ V_{IN} ≤ -8V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	-5.10		-4.90	-5.13		-4.87	V
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}	-5.15		-4.85	-5.15		-4.85	V
Line Regulation	T_j = 25°C, -25V ≤ V_{IN} ≤ -7V, I_O = 5mA		10	15		10	25	mV
Load Regulation	T_j = 25°C, V_{IN} = -10V, 5mA ≤ I_O ≤ 1.5A (Note 1)		20	50		20	100	mV
Quiescent Current	T_j = 25°C, V_{IN} = -10V, I_O = 500mA		1	2		1	2	mA
	Over Temperature, T_{MIN} ≤ T_j ≤ T_{MAX}			2.5			2.5	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = -10V, 5mA ≤ I_O ≤ 1.5A			.4			.4	mA
	T_j = 25°C, -25V ≤ V_{IN} ≤ -8V, I_O = 500mA			.4			.4	mA
Ripple Rejection	T_j = 25°C, -18V ≤ V_{IN} ≤ -8V, I_O = 500mA	54			54			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = -10V, I_O = 500mA		100			100		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		2.0			2.0		V
Short Circuit Current	T_j = 25°C, V_{IN} = -10V		1.8			1.8		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = -10V, I_O = 5mA		-.4			-.4		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = -10V, I_O = 5mA		20			20		mV
Thermal Shutdown	V_{IN} = -10V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques (t_w ≤ 10ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately. P_D = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min|V_O - V_{IN}| @ -55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7912A			UC7912AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = −17V, I_O = 5mA	−12.12		−11.88	−12.12		−11.88	V
	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_D	−12.24		−11.76	−12.30		−11.70	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	−12.36		−11.64	−12.36		−11.64	V
Line Regulation	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V, I_O = 5mA		10	20		10	30	mV
Load Regulation	T_j = 25°C, V_{IN} = −17V, 5mA ≤ I_O ≤ 1.5A (Note 1)		40	80		40	80	mV
Quiescent Current	T_j = 25°C, V_{IN} = −17V, I_O = 500mA		3			3		mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = −17V, 5mA ≤ I_O ≤ 1.5A			.4			.4	mA
	T_j = 25°C, −32V ≤ V_{IN} ≤ −14V, I_O = 500mA			.4			.4	mA
Ripple Rejection	T_j = 25°C, −25V ≤ V_{IN} ≤ −15V, I_O = 500mA	56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = −17V, I_O = 500mA		200			200		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = −17V		1.3			1.3		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = −17V, I_O = 5mA		−.9			−.9		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = −17V, I_O = 5mA		48			48		mV
Thermal Shutdown	V_{IN} = −17V, I_O = 5mA		175			175		°C
T_{MAX}			125			125		°C
T_{MIN}			−55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
P_D = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min $|V_O - V_{IN}|$ @ −55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ELECTRICAL CHARACTERISTICS $T_A=T_J$

PARAMETER	TEST CONDITIONS	UC7915A			UC7915AC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	T_j = 25°C, V_{IN} = -20V, I_O = 5mA	-15.15		-14.85	-15.15		-14.85	V
	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V 5mA ≤ I_{OUT} ≤ 1.0A, P ≤ P_O	-15.30		-14.70	-15.38		-14.63	V
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$	-15.45		-14.55	-15.45		-14.55	V
Line Regulation	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V, I_O = 5mA		10	20		10	30	mV
Load Regulation	T_j = 25°C, V_{IN} = -20V, 5mA ≤ I_O ≤ 1.5A (Note 1)		50	80		50	80	mV
Quiescent Current	T_j = 25°C, V_{IN} = -20V, I_O = 500mA		3			3		mA
	Over Temperature, $T_{MIN} \le T_j \le T_{MAX}$			4			4	mA
Quiescent Current Change	T_j = 25°C, V_{IN} = -20V, 5mA ≤ I_O ≤ 1.5A			.4			.4	mA
	T_j = 25°C, -35V ≤ V_{IN} ≤ -17V, I_O = 500mA			.4			.4	mA
Ripple Rejection	T_j = 25°C, -28V ≤ V_{IN} ≤ -18V, I_O = 500mA	56			56			dB
Output Noise Voltage	f = 10Hz to 100KHz, C_L = 1μf T_j = 25°C, V_{IN} = -17V, I_O = 500mA		250			250		μV
Dropout Voltage	T_j = 25°C, I_O = 1A		1.1			1.1		V
Short Circuit Current	T_j = 25°C, V_{IN} = -20V		1.1			1.1		A
Peak Output Current	T_j = 25°C		2.0			2.0		A
Avg. Temp. Variation of V_{OUT}	0°C ≤ T_j ≤ T_{MAX}, V_{IN} = -20V, I_O = 5mA		-1.0			-1.0		mV/°C
Long Term Stability	1000 Hrs. @ T_j = 125°C, V_{IN} = -20V, I_O = 5mA		60			60		mV
Thermal Shutdown	V_{IN} = -20V, I_O = 5mA		175			175		°C
	T_{MAX}		125			125		°C
	T_{MIN}		-55			0		°C

Note: All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_w \le 10$ms, duty-cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
P_O = 20W for TO-3 (K) and 15W for TO-220 (T), non-isolated TO-257 (G) and isolated TO-257 (IG) Min $|V_O - V_{IN}|$ @ -55°C = 2.5V.

1) Measurement taken at 0.180 inches from case for G and IG Packages.

ORDERING INFORMATION

OUTPUT VOLTAGE	PACKAGE SUFFIX		
	K (TO-3)	G (TO-257)	IG (ISOLATED TO-257)
-5V	UC7905AK UC7905ACK	UC7905AG UC7905ACG	UC7905AIG UC7905ACIG
-12V	UC7912AK UC7912ACK	UC7912AG UC7912ACG	UC7912AIG UC7912ACIG
-14V	UC7915AK UC7915ACK	UC7915AG UC7915ACG	UC7915AIG UC7915ACIG

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MOTION CONTROL CIRCUITS

5

MOTOR CONTROL CIRCUITS DESIGNER GUIDE

UNITRODE PART NUMBER	L292	L293	L293D	L295	L298	L298D	UC2950	UC3517	UC3620	UC3622	UC3623	UC3625	UC3633	UC3634,35	UC3637	UC3655	UC3657	UC3661	UC3717,17A	UC3720	UC3728	UC3770A/B	UC3174[3]
PERFORMANCE CHARACTERISTICS																							
Linear							■																
PWM	■			■					■	■	■	■			■			■	■	■	■	■	
Fixed off-time									■		■									■	■	■	
Fixed Frequency	■									■		■			■			■					
Transconductance Ampl.	■			■			■		■		■	■			■	■		■					
Low Noise	■						■	■			■					■							
Number of Totem Pole Outputs	2	4	4		4	4	1	2		3	3	3				2	3	3	2	2			2
Over 0.5A Output	■	■	■	■	■	■	■	■		■	■	■				■	■	■	■	■	■	■	
Includes Output Diodes			■			■	■			■		■					■		■				
Reversible Direction	■							■		■	■	■			■	■		■	■				■
Microstepping Capability	■			■				■		■	■	■			■			■	■				■
Hall Logic										■	■	■				■							
Full-Step/Half-Step Logic								■															
Phase-Lock Speed Control													■	■									
Four Quadrant Output	■									■		■						■					
Current Sense Capability	■			■	■	■			■	■	■	■				■	■	■	■	■	■	■	
Brake Function												■											
Tristable Outputs		■	■		■	■	■		■	■	■					■	■						
Thermal Protection	■	■	■	■	■	■	■	■	■	■	■	■			■	■	■	■	■	■	■	■	
Undervoltage Lockout	■							■	■	■	■	■				■		■		■	■		
Driver Only: TTL Inputs		■	■		■	■	■										■						
APPLICATIONS[1]																							
Unipolar Bilevel Stepper								■															
Bipolar Stepper		■	■	■	■	■	■								■		■			■			■
Three-Phase Brushless							■			■	■	■	■	■			■						
Two-Phase Brushless							■							■		■							
PWM Servo	■	■	■	■	■	■	■	■		■	■	■		■	■	■	■	■	■				■
Solenoid	■	■	■	■	■	■	■	■		■	■	■			■		■	■			■	■	
Relay	■	■	■	■	■	■	■	■		■	■	■			■		■	■			■	■	
Voice-Coil	■			■				■		■	■	■			■			■					
STANDARD PACKAGE[2]																							
16-Pin Batwing		■	■										■	■						■			■
16-Pin DIL								■															
18-Pin DIL															■								
20 Pin PLCC								■												■			■
24-Pin DIL																							
28-Pin Power PLCC							■					■				■							■
28-Pin DIL												■										■	
5-Pin TO-220							■																
15-Pin Multiwatt	■			■	■	■		■		■	■					■	■			■			
24-Pin Power Ceramic																		■					

Note 1. See Application Section for more
Note 2. Alternate Packaging Available
Note 3. Also includes 3175, 3176, 3177.

5

CROSS-APPLICATION CHART

It is often possible — and advantageous — to fit into one application an IC that was originally designed for another. Here are a few hints:

UNITRODE PART #	BRUSH SERVOMOTOR	STEPPING MOTOR	MICRO-STEPPING	BRUSHLESS		VOICE COIL	SOLENOID
				1Ø	3Ø		
L292							
L293, 293D							
L295							
L298, 298D							
UC2950							
UC3174,5,6,7							
UC3517							
UC3610,11							
UC3620,22,23							
UC3633,34							
UC3637							
UC3657							
UC3705,07							
UC3717,17A							
UC3770A,B							

INTEGRATED CIRCUITS

UNITRODE

Switchmode Driver for DC Motors

FEATURES

- Driving capability: 2A, 36V, 30KHz
- Two logic chip enable inputs
- External loop gain adjustment
- Single power supply (18 to 36V)
- Input signal symmetric to ground
- Thermal protection

DESCRIPTION

The L292 is a monlithic LSI circuit in a 15-lead Multiwatt® package. It is intended to drive DC motors controlling positioning devices such as used in typewriters, printers, plotters and other computer peripherals.

The device contains a level shifter, triangle waveform oscillator, error amplifier, PWM comparator, current sensing amplifier, H-bridge output stage with a 2A, 36V driving capability and two output enable inputs. Protection circuitry includes under-voltage output inhibit and thermal protection.

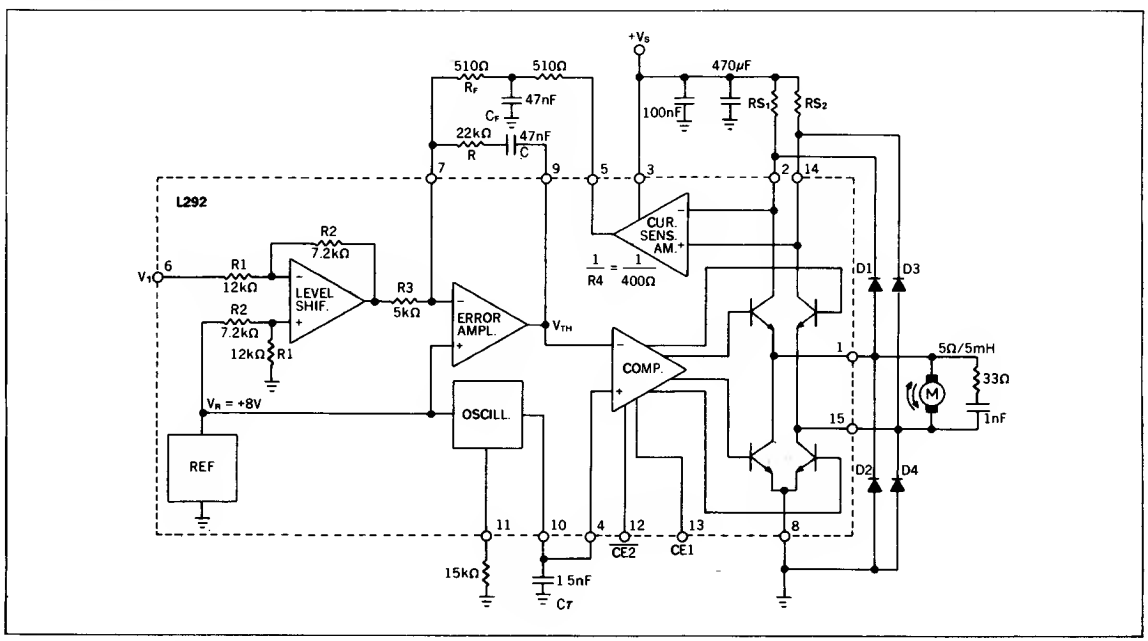
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s 36V
Input Voltage, V_1 ..... -15 to +V_sV
Inhibit Voltage, $V_{inhibit}$ ..... 0 to V_sV
Output Current, I_o 2.5A
Total Power Dissipation (T_{case} = 75°C) 25W
Storage and Junction Temperature, T_{stg} ..... -40 to +150°C
Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W

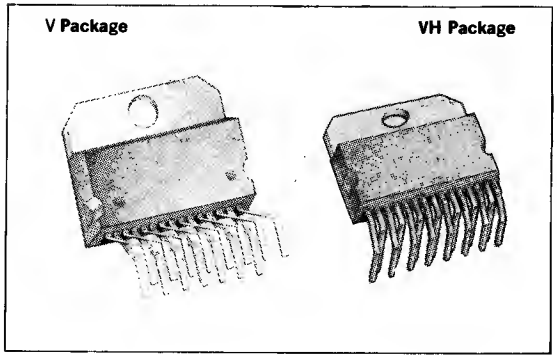
THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max

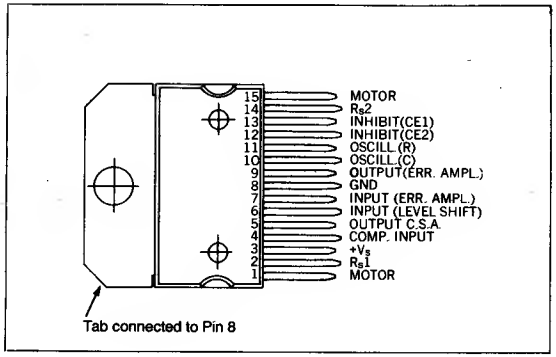
BLOCK DIAGRAM



MECHANICAL DATA



CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C; f_{osc} = 20KHz unless otherwise specified) T_A=T_J

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_s			18		36	V
Quiescent Drain Current	I_d	V_s = 20V (offset null)			30	50	mA
Input Offset Voltage (Pin 6)	V_{os}	V_s = 36V, I_o = 0				±350	mV
Inhibit Input Voltage (Pin 12, 13)	$V_{inh.}$ L					2	V
	$V_{inh.}$ H			3.2			V
Inhibit Input Current	$I_{inh.}$ L	$V_{inh.}$ (L) = 0.4V				−100	μA
	$I_{inh.}$ H	$V_{inh.}$ (H) = 3.2V				10	μA
Input Current (Pin 6)	I_I		V_I = −8.8V			−1.8	mA
			V_I = +8.8V			0.5	mA
Input Voltage (Pin 6)	V_I	R_{S1} = R_{S2} = 0.2Ω	I_o = 2A		9.1		V
			I_o = −2A		−9.1		V
Output Current	I_o	V_I ± 9.8V, R_{S1} = R_{S2} = 0.2Ω		±2			A
Total Drop Out Voltage	V_D	(including sensing resistors)	I_o = 2A			5	V
			I_o = 1A			3.5	V
Sensing Resistor Voltage Drop	V_{RS}	T_j = 150°C, I_o = 2A				0.44	V
Transconductance	$\frac{I_o}{V_i}$	R_{S1} = R_{S2} = 0.2Ω		220	240	260	mA/V
		R_{S1} = R_{S2} = 0.4Ω			120		mA/V
Frequency Range (Pin 10)	f_{osc}			1		30	KHz

TRUTH TABLE

$V_{Inhibit}$		Output Stage Condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal Operation
H	L	Disabled
H	H	Disabled

FUNCTIONAL DESCRIPTION

The error signal input has been designed to accept a bidirectional error signal symmetrical to ground. The level shifter converts the ± error signal into a single positive signal with the aid of an internally generated 8V reference. This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_T, C_T - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \text{ (with } R \geq 8.2K\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{S1}, R_{S2} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in this RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5Ω, 5mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ, is programmed by C_T in conjunction with an internal resistor R_T.

This can be found from:

$\tau = R_T \cdot C_{PIN\ 10}$ (C_T in the diagram)

Since R_T is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5μS, $C_{PIN\ 10}$ should be around 1.5nF.

The current sense resistors R_{S1} and R_{S1} should be high precision types (maximum tolerance ±2%) and the recommended value is given by:

$R_{max} \cdot I_{o\ max} \leq 0.44V$

It is possible to synchronize two L292s, if desired, using the network shown in Figure 1.

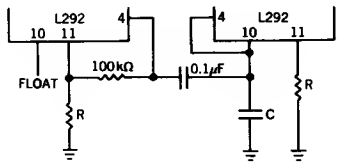


Figure 1.

Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively). Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generate spikes as high as 1.5V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see Figure 2).

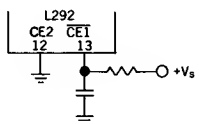


Figure 2.

APPLICATION INFORMATION

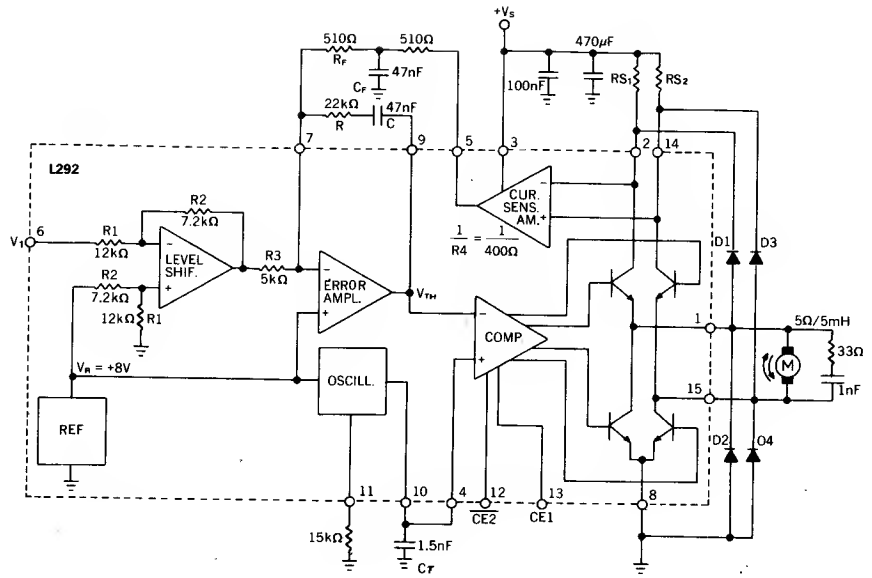
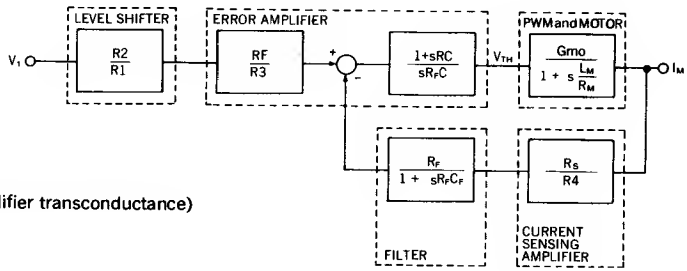


Figure 3.

The schematic diagram used for the Laplace analysis of the system is shown in Figure 4.



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3}\,\Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance
R_M = Motor resistance
I_M = Motor current

$G_{mo} = \left.\frac{I_M}{V_{TH}}\right|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current (I_M)).

Figure 4.

APPLICATION INFORMATION (continued)

Neglecting the $V_{CE\ sat}$ of the bridge transistor and the V_{BE} of the diodes:

$$G_{mo} = \frac{1}{R_M}\frac{2V_S}{V_R} \quad \text{where: } V_S = \text{supply voltage} \quad (1)$$

V_R = 8V (reference voltage)

DC Transfer Function

In order to be sure that the current loop is stable the following condition is imposed:

$$1 + sRC = 1\ s\frac{L_M}{R_M} \quad \text{(pole cancellation)} \quad (2)$$

from which $RC = \frac{L_M}{R_M}$ (Note that in practice R must be greater than 5.6KΩ)

The transfer function is then, (3)

$$\frac{I_M}{V_i}(s) = \frac{R_2R_4}{R_1R_3} G_{mo} \frac{1 + sR_FC_F}{G_{mo}R_s + s\,R_4C + s^2\,R_FC_FR_4C}$$

In DC condition, this is reduced to

$$\frac{I_M}{V_i}(o) = \frac{R_2R_4}{R_1R_3} \cdot \frac{1}{R_s} = \frac{0.048}{R_s}\left[\frac{A}{V}\right]$$

Open-Loop Gain and Stability Criterion

For $RC = L_M/R_M$, the open loop gain is: (5)

$$A\beta = \frac{1}{sR_FC} \cdot G_{mo}\frac{R_s}{R_4}\frac{R_F}{1 + sR_FC_F} = \frac{G_{mo}\,R_s}{R_4C}\frac{1}{s\,(1 + sR_FC_F)}$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_FC_F}$, $|A\beta|$ must be < 1

(see Figure 5), that is:

$$|A\beta|\ f = \frac{1}{2\pi R_FC_F} = \frac{G_{mo}R_s}{R_4C}\frac{R_FC_F}{\sqrt{2}} < 1 \quad (6)$$

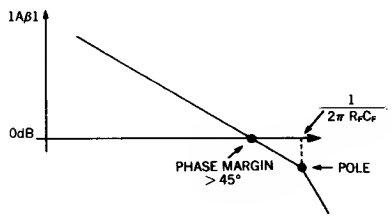


Figure 5. Open-Loop Frequency Response

Closed-Loop System Step Response

a) Small-signals analysis

The transfer function (3) can be written as follows:

$$\frac{I_M}{V_i}(s) = \frac{0.048}{R_s}\frac{1 + \frac{s}{2\,\xi\,\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \quad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo}R_s}{R_4C\ R_FC_F}}$ is the cutoff frequency

where: $\xi = \sqrt{\frac{R_4C}{4\ R_FC_F\ G_{mo}\ R_s}}$ is the damping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

1) $\xi = 1$ from which

$$I_M(t) = \frac{0.048}{R_s}\left[1 - e^{-\frac{t}{2R_FC_F}}\left(1 + \frac{t}{4\ R_FC_F}\right)\right] \cdot V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.048}{R_s}\left(1 - \cos\frac{t}{2R_FC_F}\ e^{-\frac{t}{2R_FC_F}}\right) V_i$$

From Figure 7 it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.

The previous linear analysis is correct for this example.

Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \quad \text{(phase margin = 45°)}$$

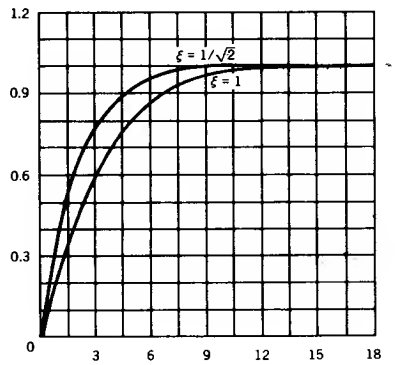


Figure 6. Small Signal Step Response (Normalized Amplitude vs t/R_FC_F)

APPLICATION INFORMATION (continued)

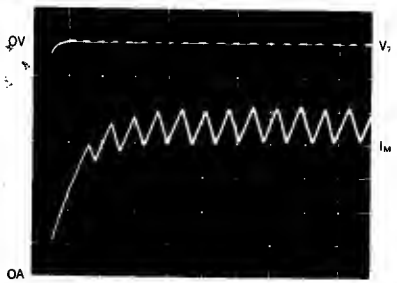


Figure 7. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Small Signal Response

b) Large signal response

The large step signal response is limited by slew-rate and inductive load. In this case, during the rise-time of the motor current, the L292 works in open-loop condition, as can be seen from Figure 8.

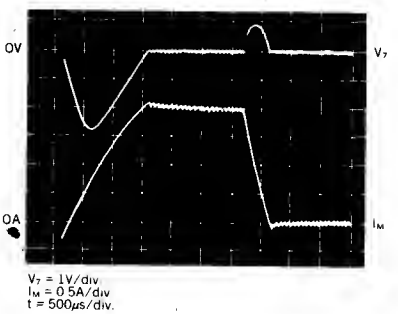


Figure 8. Motor Current and Pin 7 Voltage Waveforms (Application of Figure 3). Large Signal Response

The voltage at pin 7 (inverting input of the error amplifier) departs from the reference voltage V_R present at the non-inverting input and the feedback loop is open.

The feedback loop is on when the motor current reaches its steady-state value (2A).

Closed Loop System Bandwidth

A good choice for ξ is the value $1/\sqrt{2}$. In this case:

$$\frac{I_M}{V_i}(s) = \frac{0.048}{R_s} \cdot \frac{1 + s\,R_F C_F}{1 + 2s\,R_F C_F + 2s^2 R_F^2 C_F^2} \qquad (8)$$

The module of the transfer function is: (9)

$$\left|\frac{I_M}{V_i}\right| = \frac{0.048}{R_s} \cdot \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}}$$

The cutoff frequency is derived from expression (9) by putting

$$\left|\frac{I_M}{V_i}\right| = 0.707 \cdot \frac{0.048}{R_s} \text{ (-3dB);}$$

from which:

$$\omega_T = \frac{0.9}{R_F C_F} \qquad f_T = \frac{0.9}{2\pi R_F C_F} \qquad (10)$$

Note that R_F must be less than 1.5KΩ in order to have the maximum current swing at the output of current sensing amplifier.

Working Frequency and Motor Current Ripple

For a value of rotation speed ω the e.m.f. E is equal to $K_E\omega$, where K_E is the motor speed constant.

Neglecting the motor resistance R_M, the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes, we have:

$$\Delta t_1 = \frac{\Delta I_M}{V_s - E} L_M \quad \text{(transistors conduction period)} \qquad (11)$$

$$\Delta t_2 = \frac{\Delta I_M}{V_s + E} L_M \quad \text{(diodes conduction period)}$$

Where ΔI_M is the current ripple in the motor (see Figure 9).

The working frequency is:

$$f = \frac{1}{2\,R_T C_T} = \Delta t_1 = \Delta t_2 \qquad (12)$$

where R_T is the resistance at pin 11 and C_T the capacitor at pin 10. R_T must be ≥ 8.2KΩ due to the output current capability at pin 11.

If we consider E = 0 (ω = 0; motor stopped) we have:

$$\Delta t_1 = \Delta t_2 = \frac{\Delta I_M}{V_s} L_M \qquad (13)$$

from this formula we can write

$$\Delta I_M = \frac{V_s}{L_M} \frac{T}{2} \qquad \left(\frac{T}{2} = \Delta t_1 = \Delta t_2 = \text{half period}\right) \qquad (13 \text{ bis})$$

The motor current ripple ΔI_M must be limited in order to reduce dissipation in the motor and the peak output current of the L292.

$\Delta I_{M\,max}$ should be less than 10% of $I_{M\,max}$ (see Figure 9).

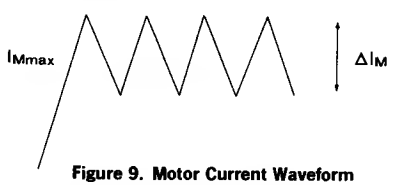


Figure 9. Motor Current Waveform

From the equation (13 bis) and considering $\Delta I_M = 0.1\,I_{M\,max}$ we have:

$$0.1\,I_{Mmax} = \frac{V_s}{2f\,L_{Mmin}} \qquad (14)$$

from which:

$$L_{Mmin} = \frac{5\,V_s}{f\,I_{Mmax}} \qquad (15)$$

The switching characteristics of the L292 demand that the working frequency f is less than 30KHz.

If for f = 30KHz, L_M is less than L_{Mmin}, an external inductor should be put in series with the motor.

From relationship (15) we have:

$$L_{seriss} = \frac{5\ V_s}{f\ I_{Mmax}} - L_M \qquad (16)$$

Deadtime

A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which, if it were allowed to occur would damage them. To overcome this the comparator that drives the final stage in effect consists of two separate comparators (Figure 10): both receive the same Vt signal but on opposite inputs. The other two inputs are driven by V_{TH} shifted by plus or minus $R_T I'$. This voltage shift when compared with Vt results in a delay in switching from one comparator to the other. In this way there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor R_T (1.5K) and an external capacitor C_T connected to pin 10 which also fixes oscillator frequency.

It is: $\tau = R_T C_T$

In a typical application, a capacitor of 1.5nF is used to give a switching delay of 2.25μs, a more than adequate time when you consider that the switch-off delay of the integrated transistors is only 0.5μs.

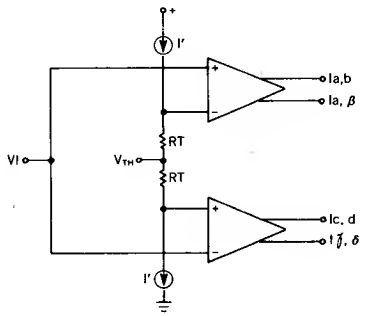


Figure 10. L292 Deadtime Control

Efficiency and Power Dissipation

The expression for the bridge efficiency, independently of the losses due to the switching times and neglecting the dissipation due to the motor current ripple, is:

$$\eta = 1 - \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{sat}}{V_s} - \frac{\Delta t_2}{\Delta t_1 + \Delta t_2} \cdot \frac{V_{ovsr}}{V_s} \qquad (17)$$

where $V_{over} \cong 2V\ (2V_{BE} + R_s I_M)$
$V_{sat} \cong 4V\ (2V_{CE\ sat} + 3V_{BE})$
Δt_1 = transistors conduction period.
Δt_2 = diodes conduction period.

If $\Delta t_1 \gg \Delta t_2$ and $V_s = 20V$, we obtain:

$$\eta = 1 - \frac{4}{20} = 80\% \qquad (18)$$

In practice, the efficiency will be slightly lower due to the signal circuit dissipation (1W @ 20V) and the finite switching times (about 1W). If we transfer to the motor a power of 40W the bridge power dissipation from (18) is 10W and the total dissipation is 12W. This is an actual efficiency of 77%. Considering a maximum dissipation equal to 20W for the L292 (Multiwatt package), it is possible to handle continuous powers greater than 60W.

EXAMPLE

a) Data
- Motor characteristics: $L_M = 5mH$, $R_M = 5\Omega$, $L_M/R_M = 1msec$
- Voltage and current characteristics: $V_s = 20V$ $I_M = 2A$ $V_i = 8.3V$
- Closed loop bandwidth: 3kHz.

b) Calculation
- From relationship (4):

$$R_s = \frac{0.048}{I_M} V_i = 0.2\Omega$$

and from (1):

$$G_{mo} = \frac{2V_s}{R_M V_R} 1\Omega^{-1}$$

- RC = 1msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{400\ C}{4\ R_F C_F \cdot 0.2}$$

The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 3kHz$$

c) Summarizing
- $RC = 1 \cdot 10^{-3}$ sec
- $\frac{1000\ C}{R_F C_F} = 1$
- $R_F C_F \cong 47\mu s$

} C = 47nF, R = 22KΩ

For $R_F = 510\Omega$ → $C_F = 92nF$

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INTEGRATED CIRCUITS

UNITRODE

Push-Pull Four Channel Driver

L293
L293D

FEATURES

- Output current 1A per channel (600mA for L293D)
- Peak output current 2A per channel (1.2A for L293D)
- Inhibit facility
- High noise immunity
- Separate logic supply
- Over-temperature protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are packaged in 16-pin plastic DIPs; both use the four center pins to conduct heat to the printed circuit boards.

ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_c 36V
Logic Supply Voltage, V_{ss} 36V
Input Voltage, V_i 7V
Inhibit Voltage, $V_{inh.}$ 7V
Peak Output Current (Non-Repetitive), I_{out} (L293) 2A
I_{out} (L293D) 1.2A
Total Power Dissipation at $T_{ground-pins.}$ = 80°C, P_{tot} 5W
Storage and Junction Temperature, T_{stg}, T_j .....-40 to +150°C

THERMAL DATA

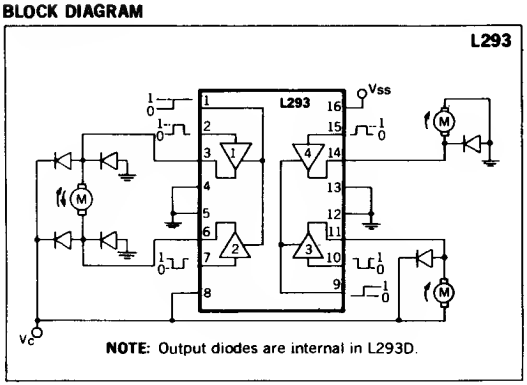
Thermal Resistance Junction-Case, θ_{JC} ..... 14°C/W max
Thermal Resistance Junction-Ambient, θ_{JA} ..... 80°C/W max

TRUTH TABLE

V_i (each channel)	$V_{inh.}$*	V_o
H	H	H
L	H	L
H	L	X**
L	L	X**

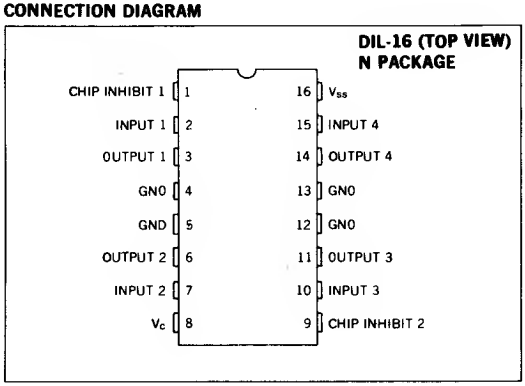
*Relative to the considered channel.
**High output impedance.

BLOCK DIAGRAM



NOTE: Output diodes are internal in L293D.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS (For each channel, V_c = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified) T_A=T_J

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_c				36	V
Logic Supply Voltage	V_{ss}		4.5		36	V
Collector Supply Current	I_c	V_i = L, I_o = 0, $V_{inh.}$ = H		2	6	mA
		V_i = H, I_o = 0, $V_{inh.}$ = H		16	24	
		$V_{inh.}$ = L			4	
Total Quiescent Logic Supply Current	I_{ss}	V_i = L, I_o = 0, $V_{inh.}$ = H		44	60	mA
		V_i = H, I_o = 0, $V_{inh.}$ = H		16	22	
		$V_{inh.}$ = L		16	24	
Input Low Voltage	V_{iL}		-0.3		1.5	V
Input High Voltage	V_{iH}	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Input Current	I_{iL}	V_i = L			-10	μA
High Voltage Input Current	I_{iH}	V_i = H		30	100	μA
Inhibit Low Voltage	$V_{inh.L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{inh.H}$	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
Low Voltage Inhibit Current	$I_{inh.L}$			-30	-100	μA
High Voltage Inhibit Current	$I_{inh.H}$				10	μA
Source Output Saturation Voltage	V_{CEsatH}	I_o = -1A (-0.6A for L293D)		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	I_o = 1A (0.6A for L293D)		1.2	1.8	V
Clamp Diode Forward Voltage (L293D only)	V_F	I_F = 0.6A		1.3		V
Rise Time	t_r	0.1 to 0.9 V_o (See Figure 1)		250		ns
Fall Time	t_f	0.9 to 0.1 V_o (See Figure 1)		250		ns
Turn-On Delay	t_{ON}	0.5 V_i to 0.5 V_o (See Figure 1)		450		ns
Turn-Off Delay	t_{OFF}	0.5 V_i to 0.5 V_o (See Figure 1)		200		ns

SCHEMATIC DIAGRAM

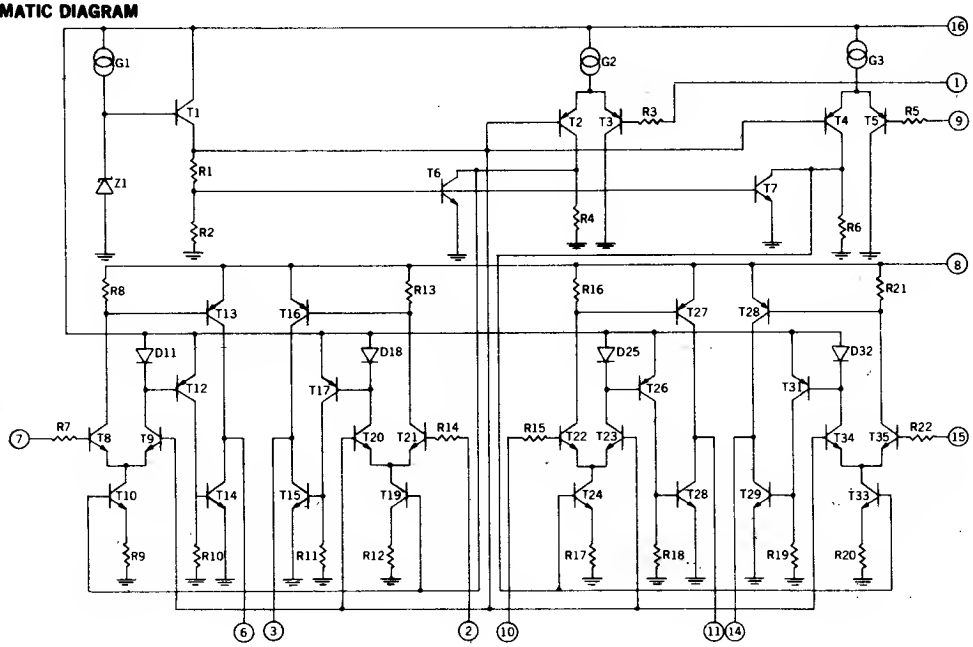


Figure 1. Switching Times

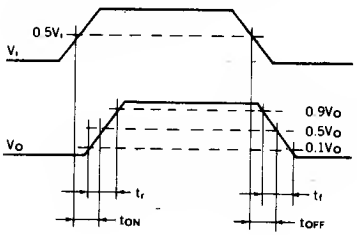


Figure 2. Quiescent Logic Supply Current vs Logic Supply Voltage

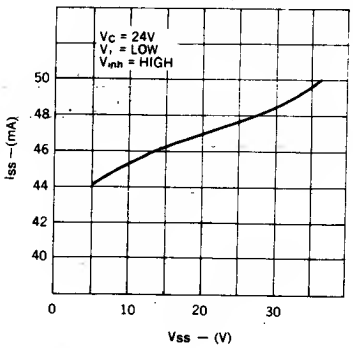


Figure 3. Output Voltage vs Input Voltage

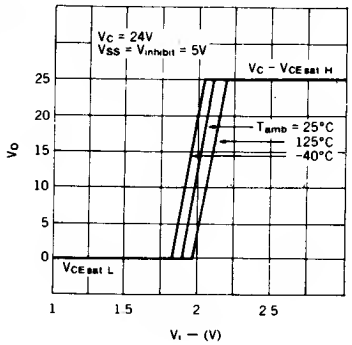


Figure 4. L293 Saturation vs Output Current

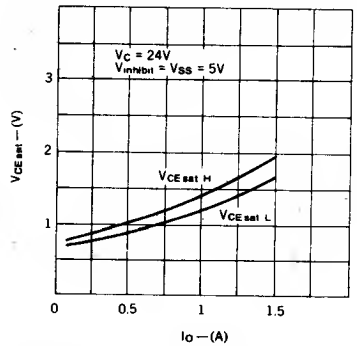


Figure 5. L293 Source Saturation vs Ambient Temperature

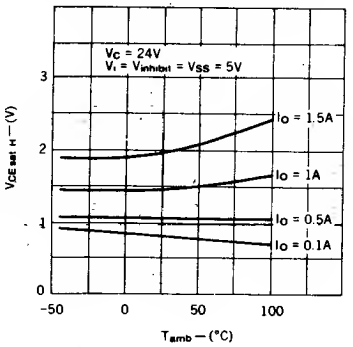
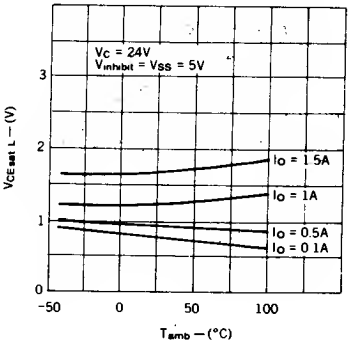


Figure 6. L293 Sink Saturation Voltage vs Ambient Temperature



NOTE: For L293D curves, multiply output current by 0.6

Figure 7. DC Motor Controls (with Connection to Ground and to the Supply Voltage)

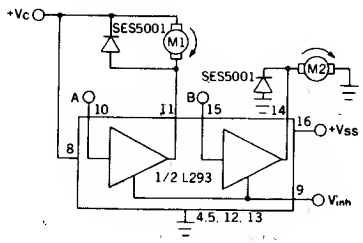
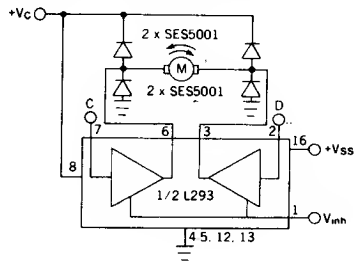


Figure 8. Bidirectional DC Motor Control



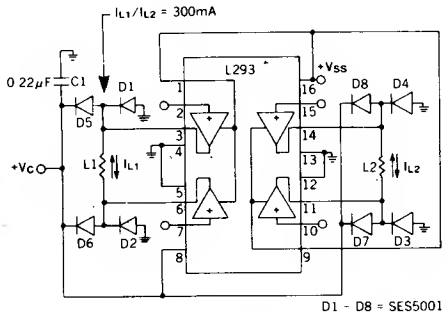
$V_{inh.}$	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't care

INPUTS		FUNCTION
$V_{inh.}$ = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
$V_{inh.}$ = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 9. Bipolar Stepping Motor Control



MOUNTING INSTRUCTIONS

The $R_{th_{j-amp}}$ of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power P_{tot} and the θ_{JA} as a function of the side " ℓ " of two equal square copper areas having a thickness of 35μ (see Figure 12). In addition, it is possible to use an external heatsink (see Figure 14).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 10. Example of P.C. Board Copper Area which is used as Heatsink

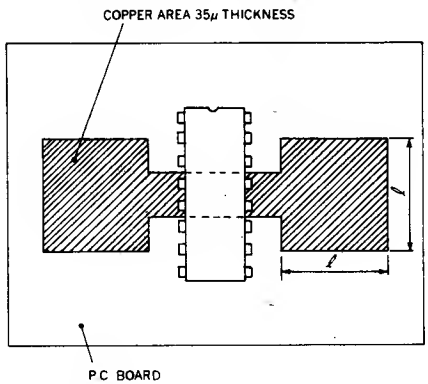


Figure 11. External Heatsink Mounting Example (θ_{JA} = 25°C/W)

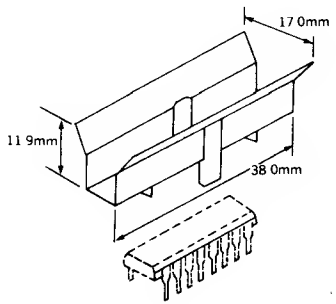


Figure 12. Maximum Package Power and Junction to Ambient Thermal Resistance vs Size " ℓ "

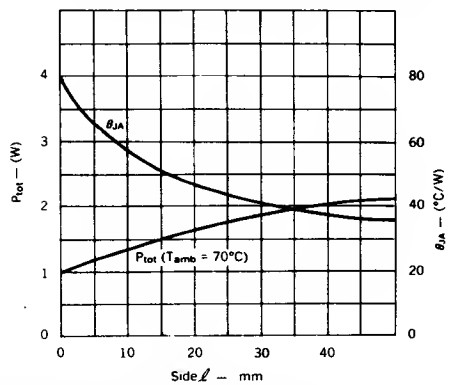
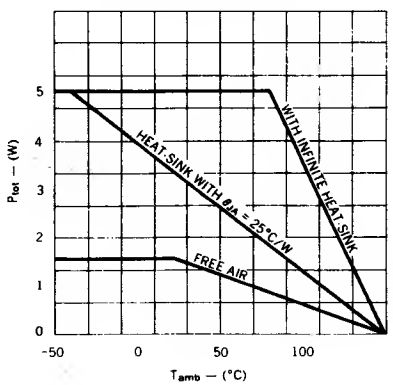


Figure 13. Maximum Allowable Power Dissipation vs Ambient Temperature



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Telephone 603-424-2410 • FAX 603-424-3460

Dual Full-Bridge Power Driver

FEATURES

- Operating Supply Voltage up to 46V
- Total Saturation Voltage 3.4V max at 1A
- Overtemperature Protected
- Operates in Switched and L/R Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs

DESCRIPTION

The L298 is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 2A continuously.

Logic inputs to the L298 have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298 input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are separately available for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298 ideal for systems that require low standby current, such as portable or battery-operated equipment.

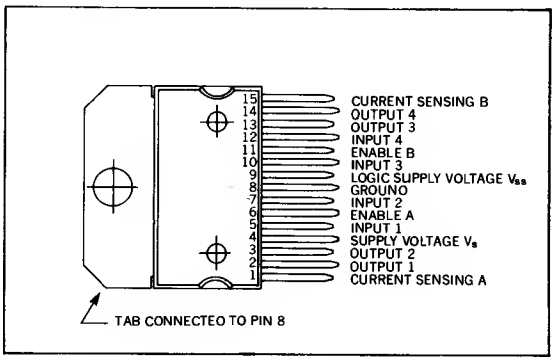
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s 50V
Logic Supply Voltage, V_{ss} 7V
Input and Inhibit Voltage, V_i, $V_{inhibit}$ ..... -0.3V to +7V
Peak Output Current (each channel), I_o
  Non-Repetitive (t = 100μs) 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Sensing Voltage, V_{sens} ..... -1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot} 25W
Storage and Junction Temperature, T_{stg}, T_j ..... -40°C to +150°C

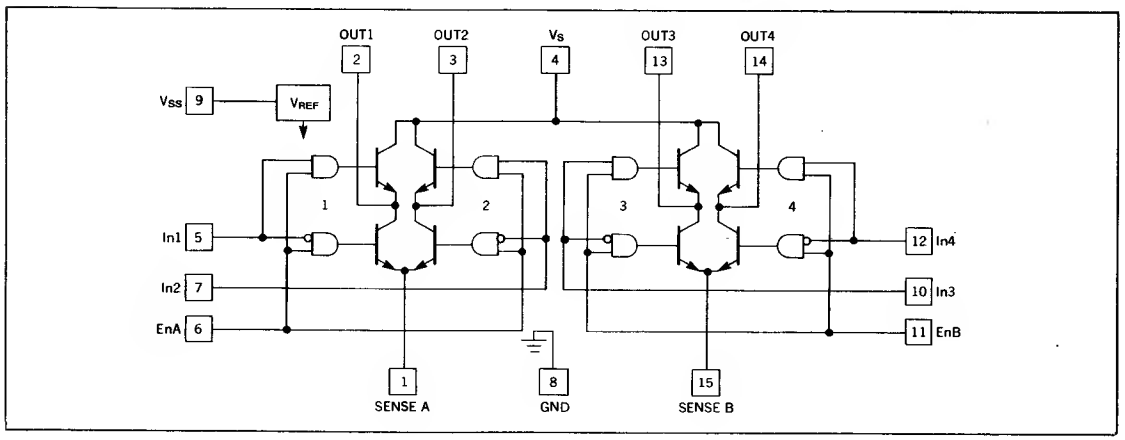
THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j\text{-}case}$ ..... 3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j\text{-}amb}$ .... 35°C/W max.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C) T_A=T_J

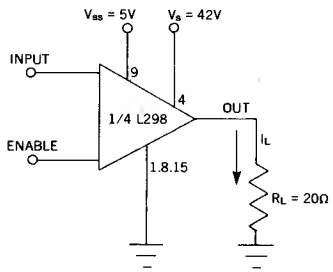
PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operating Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	$V_{inh.}$ = H $\quad \overline{V_i}$ = L		3	7	mA
	I_L = 0 $\quad \overline{V_i}$ = H		15	20	
	$V_{inh.}$ = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	$V_{inh.}$ = H $\quad \overline{V_i}$ = L		5	10	mA
	I_L = 0 $\quad \overline{V_i}$ = H		1.5	3	
	$V_{inh.}$ = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\ L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\ H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ H}$	V_i = H		30	100	
Inhibit Low Voltage (Pins 6, 11), $V_{inh.\ L}$		-0.3		1.5	V
Inhibit High Voltage (Pins 6, 11), $V_{inh.\ H}$		2.3		7	
Low Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ L}$	$V_{inh.}$ = L			-10	μA
High Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ H}$	$V_{inh.}$ = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\ sat(H)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.8	2.8	
Sink Saturation Voltage, $V_{CE\ sat(L)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.7	2.6	
Total Drop, $V_{CE\ sat}$	I_L = 1A			3.4	V
	I_L = 2A			5.2	
Sensing Voltage (Pins 1, 15), V_{sens}		-1 (1)		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency, f_c	I_L = 2A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

5

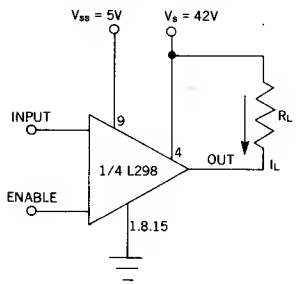
SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 2. Switching Times Test Circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input or Enable Chopper.

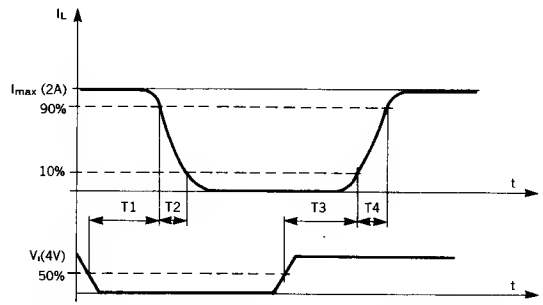
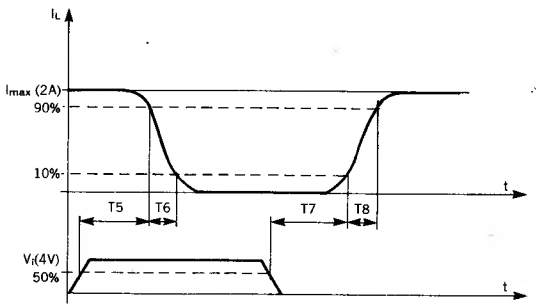
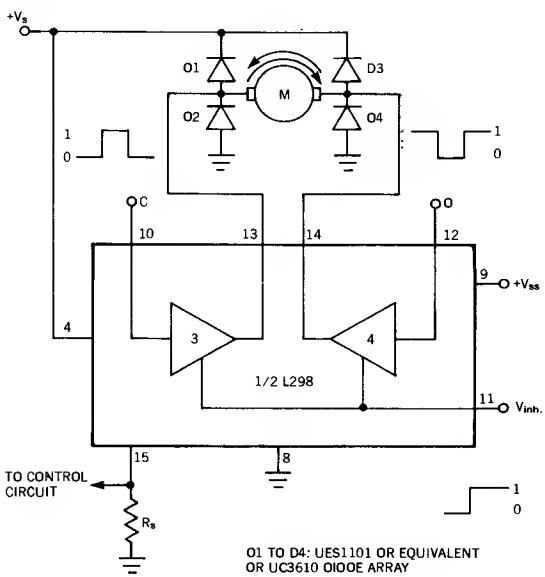


Figure 2a. Sink Current Delay Times vs. Input or Enable Chopper.



APPLICATIONS

Figure 3. Bi-Directional DC Motor Control.

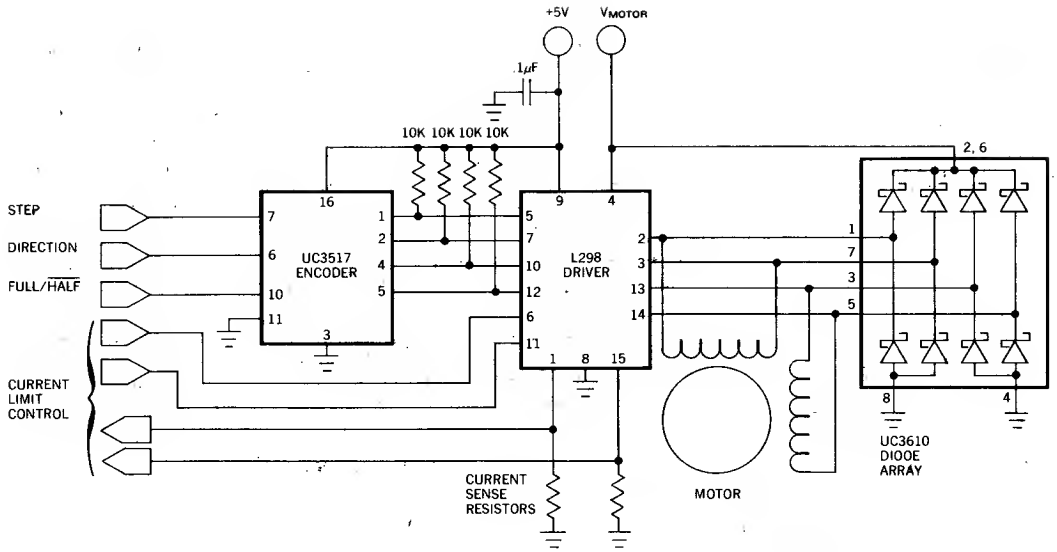


D1 TO D4: UES1101 OR EQUIVALENT OR UC3610 OIODE ARRAY

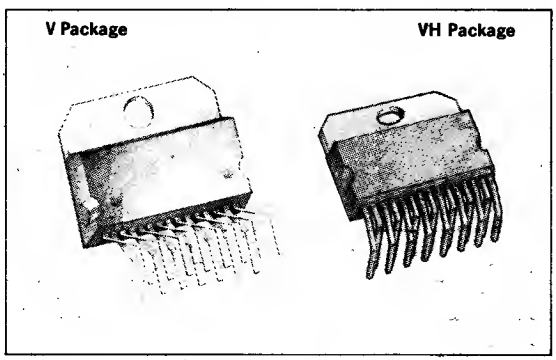
	INPUTS	FUNCTION
$V_{inh.}$ = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
$V_{inh.}$ = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

Figure 4. Bipolar Step Motor Driver.



STANDARD PACKAGES



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INTEGRATED CIRCUITS

UNITRODE

L298D

Dual Full-Bridge Power Driver

FEATURES

- Operating Supply Voltage up to 46V
- Overtemperature Protected
- Operates in Switched and L/R Current Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs
- Internal Diodes Minimize Parts Count

DESCRIPTION

The L298D is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 1A continuously.

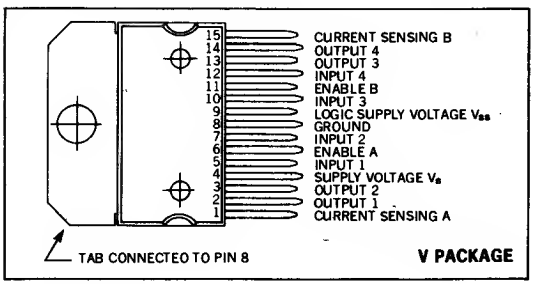
The L298D features internal diodes for clamping output excursions when driving inductive loads, such as motors and transmission lines. For most applications, these diodes can completely replace all external clamp diodes. In certain cases, however, additional output catch diodes may be valuable for reducing recovery time or power dissipation.

Logic inputs to the L298D have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298D input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are available in pairs for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298D ideal for systems that require low standby current, such as portable or battery-operated equipment.

CONNECTION DIAGRAM (TOP VIEW)



V PACKAGE

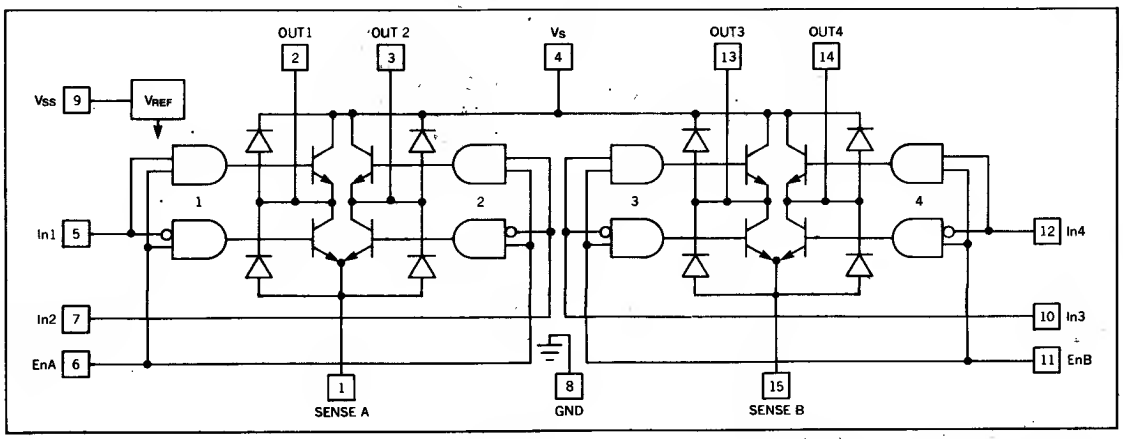
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s	50V
Logic Supply Voltage, V_{ss}	7V
Input and Enable Voltage, V_i, V_{En}	−0.3V to +7V
Peak Output Current (each channel), I_o	
Non-Repetitive (t = 100μs)	1.5A
Repetitive (80% on - 20% off; t_{ON} = 10ms)	1.2A
DC Operation	1A
Sensing Voltage, V_{sens}	−1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot}	25W
Storage and Junction Temperature, T_{stg}, T_j	−40°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j-case}$	3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j-amb}$	35°C/W max.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C) T_A=T_J

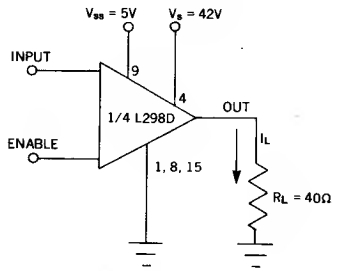
PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operating Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	V_{En} = H V_i = L		3	7	mA
	I_L = 0 V_i = H		15	20	
	V_{En} = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	V_{En} = H V_i = L		5	10	mA
	I_L = 0 V_i = H		1.5	3	
	V_{En} = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\,L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\,H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\,L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\,H}$	V_i = H		30	100	
Enable Low Voltage (Pins 6, 11), $V_{En\,L}$		-0.3		1.5	V
Enable High Voltage (Pins 6, 11), $V_{En\,H}$		2.3		7	
Low Voltage Enable Current (Pins 6, 11), $I_{En\,L}$	V_{En} = L			-10	μA
High Voltage Enable Current (Pins 6, 11), $I_{En\,H}$	V_{En} = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\,sat(H)}$	I_L = 1A		1.2	2.2	V
Sink Saturation Voltage, $V_{CE\,sat(L)}$	I_L = 1A		1.4	2.2	V
Total Drop, $V_{CE\,sat}$	I_L = 1A		2.6	4.2	V
High-Side Diode Voltage, $V_{D(H)}$	I_L = 1A		1.6	2.1	V
Low-Side Diode Voltage, $V_{D(L)}$	I_L = 1A		1.6	2.1	V
Sensing Voltage (Pins 1, 15), V_{sens}		-1 (1)		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency, f_c	I_L = 1A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

5

SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input.

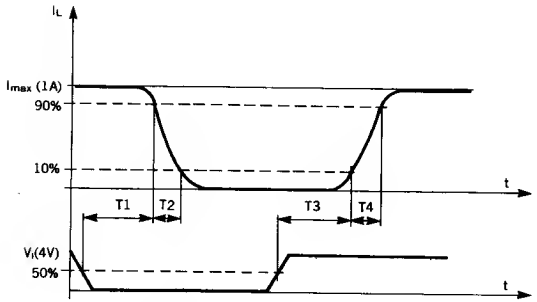
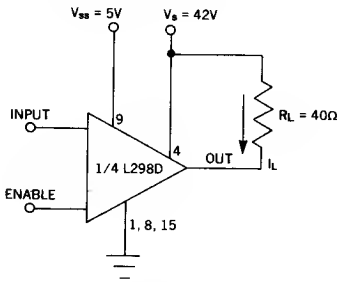
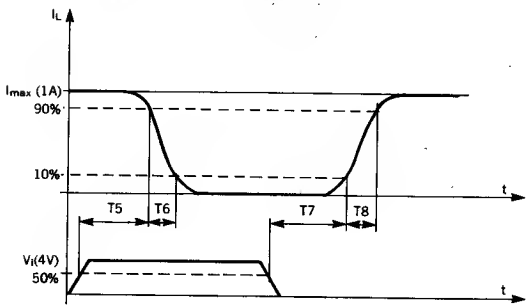


Figure 2. Switching Times Test Circuits.



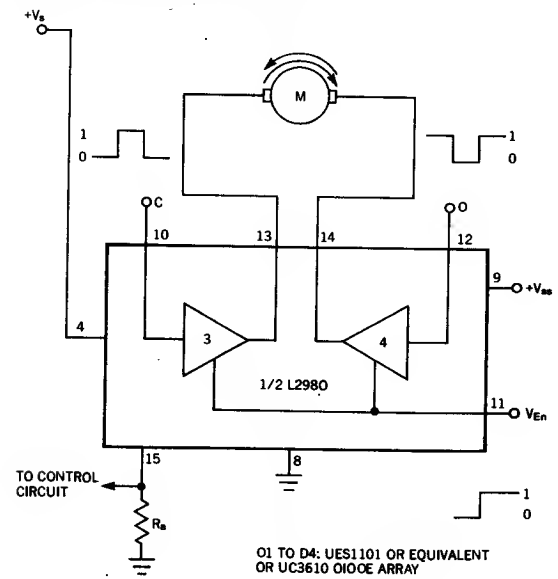
NOTE: For INPUT chopper, set EN = H.

Figure 2a. Sink Current Delay Times vs. Input.



APPLICATIONS

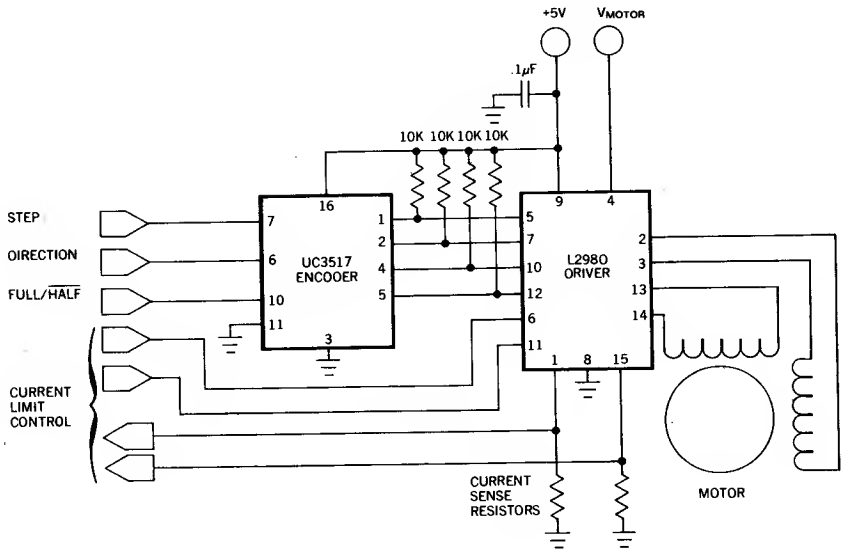
Figure 3. Bi-Directional DC Motor Control.



	INPUTS	FUNCTION
V_{En} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{En} = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

Figure 4. Bipolar Step Motor Driver.



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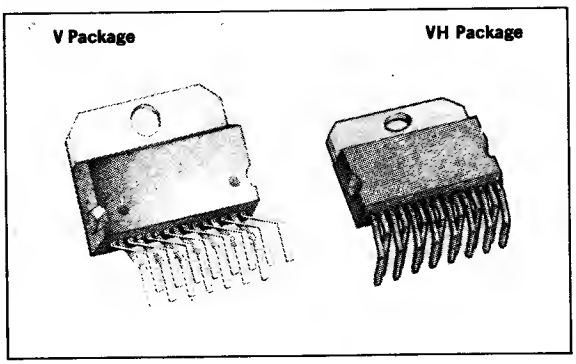
STANDARD PACKAGES



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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

Stepper Motor Drive Circuit

UC1517
UC3517

FEATURES

- Complete Motor Driver and Encoder
- Continuous Drive Capability 350mA per Phase
- Contains all Required Logic for Full and Half Stepping
- Bilevel Operation for Fast Step Rates
- Operates as a Voltage Doubler
- Useable as a Phase Generator and/or as a Driver
- Power-On Reset Guarantees Safe, Predictable Power-Up
- Monolithic Construction
- 16 Lead Plastic or Hermetic DIL Package

DESCRIPTION

The UC3517 contains four NPN drivers that operate in two-phase fashion for full-step and half-step motor control. The UC3517 also contains two emitter followers, two monostables, phase decoder logic, power-on reset, and low-voltage protection, making it a versatile system for driving small stepper motors or for controlling large power devices.

The emitter followers and monostables in the UC3517 are configured to apply higher-voltage pulses to the motor at each step command. This drive technique, called "**Bilevel**," allows faster stepping than common resistive current limiting, yet generates less electrical noise than chopping techniques.

ORDERING INFORMATION

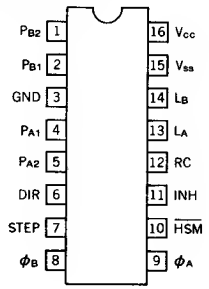
	Operating Temperature Range
UC1517J, CERDIP	-55°C to +125°C
UC3517J, CERDIP	0°C to +70°C
UC3517N, Plastic Package	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

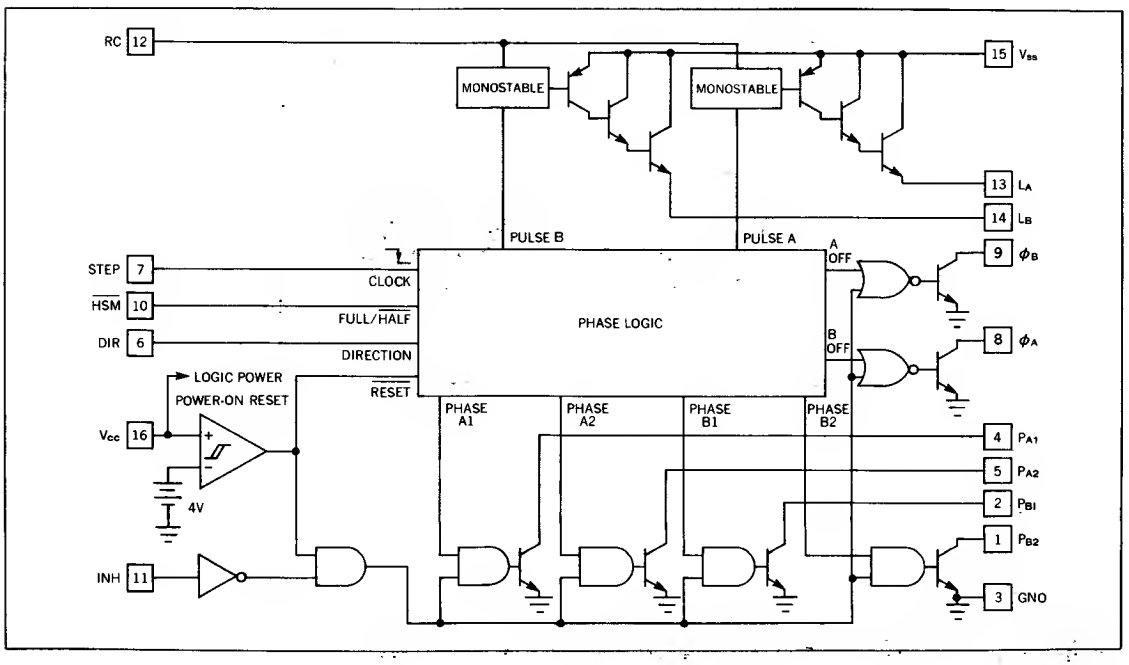
Second Level Supply, V_{ss} 40V
Phase Output Supply, V_{mm} 40V
Logic Supply, V_{cc} 7V
Logic Input Voltage, V_{in} ..... -.3V to +7V
Logic Input Current, I_{in} ..... ±10mA
Output Current, Each Phase, I_{phase} 500mA
Output Current, Emitter Follower, I_{second} ..... -500mA
Power Dissipation, 50°C, CERDIP, P_{diss} 1W
Derate 10mW/°C Above 50°C
Power Dissipation, 25°C, Plastic Package, P_{diss} 2W
Derate 10mW/°C above 25°C
Junction Temperature, T_{junct} ..... 150°C
Ambient Temperature, UC1517, $T_{ambient}$ ..... -55°C to +125°C
Ambient Temperature, UC3517, $T_{embient}$ ..... 0°C to +70°C
Storage Temperature, $T_{storage}$ ..... -55°C to +150°C

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1517 and 0°C to +70°C for the UC3517; V_{cc} = 5V; V_{ss} = 20V.) T_A=T_J

PARAMETER	TEST CONDITIONS	UC1517 UC3517			UNITS
		MIN.	TYP.	MAX.	
Logic Supply, V_{cc}	Pin 16	4.75		5.25	V
Second Supply, V_{ss}	Pin 15	10		40	V
Logic Supply Current	V_{INH} = 0.4V		45	60	mA
Logic Supply Current	V_{INH} = 4.0V		12		mA
Input Low Voltage	Pins 6, 7, 10, 11			0.8	V
Input High Voltage	Pins 6, 7, 10, 11	2.0			V
Input Low Current	Pins 6, 7, 10, 11; V = 0V			−400	μA
Input High Current	Pins 6, 7, 10, 11; V = 5V			20	μA
Phase Output Saturation Voltage	Pins 1, 2, 4, 5; I = 350mA		0.6	0.85	V
Phase Output Leakage Current	Pins 1, 2, 4, 5; V = 39V			500	μA
Follower Saturation Voltage to V_{ss}	Pins 13, 14; I = 350mA			−2	V
Follower Leakage Current	Pins 13, 14; V = 0V			500	μA
Output Low Voltage, ϕ_A, ϕ_B	Pins 8, 9; I = 1.6mA		0.1	0.4	V
Phase Turn-On Time	Pins 1, 2, 4, 5		2		μS
Phase Turn-Off Time	Pins 1, 2, 4, 5		1.8		μS
Second-Level On Time, t_{mono}	Pins 13, 14; Figure 3 Test Circuit	275	325	375	μS
Logic Input Set-Up Time, t_s	Pins 6, 10; Figure 4	400			nS
Logic Input Hold Time, t_h	Pins 6, 10; Figure 4	0			nS
STEP Pulse Width, t_p	Pin 7; Figure 4	800			nS
Timing Resistor Value	Pin 12	1K		100K	Ω
Timing Capacitor Value	Pin 12	0.1		500	nF
Power-On Threshold	Pin 16		4.3		V
Power-Off Threshold	Pin 16		3.8		V
Power Hysteresis	Pin 16		0.5		V

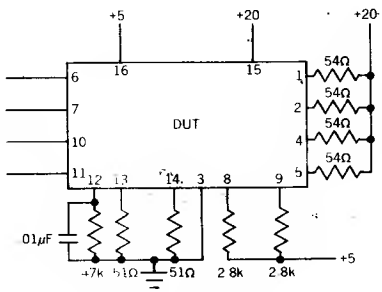


Figure 3. Test Circuit

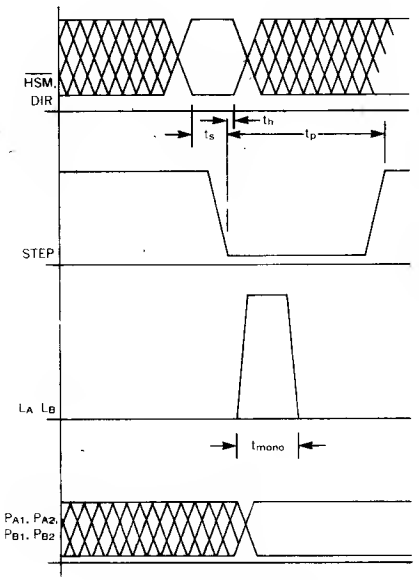


Figure 4. Timing Waveforms

PIN DESCRIPTIONS

V_{cc}: V_{cc} is the UC3517's logic supply. Connect to a regulated 5VDC, and bypass with a 0.1μF ceramic capacitor to absorb switching transients.

V_{mm}: V_{mm} is the primary motor supply. It connects to the UC3517 phase outputs through the motor windings. Limit this supply to less than 40V to prevent breakdown of the phase output transistors. Select the nominal V_{mm} voltage for the desired continuous winding current.

V_{ss}: V_{ss} is the secondary motor supply. It drives the L_A and L_B outputs of the UC3517 when a monostable in the UC3517 is active. In the bilevel application, this supply is applied to the motor to charge winding inductance faster than the primary supply could. Typically, V_{ss} is higher in voltage than V_{mm}, although V_{ss} must be less than 40V. The V_{ss} supply should have good transient capability.

GROUND: The ground pin is the common reference for all supplies, inputs, and outputs.

RC: RC controls the timing functions of the monostables in the UC3517. It is normally connected to a resistor (R_T) and a capacitor (C_T) to ground, as shown in Figure 3. Monostable on time is determined by the formula: $T_{ON} \approx 0.69\ R_T\ C_T$. To keep the monostable on indefinitely, pull RC to V_{cc} through a 50k resistor. The UC3517 contains only one RC pin for two monostables. If step rates comparable to T_{ON} are commanded, incorrect pulsing can result, so consider maximum step rates when selecting R_T and C_T. Keep $T_{ON} \leq T_{STEP\ MAX}$.

ϕ_A and ϕ_B: These logic outputs indicate half-step position. These outputs are open-collector, low-current drivers, and may directly drive TTL logic. They can also drive CMOS logic if a pull-up resistor is provided. Systems which use the UC3517 as an encoder and use a different driver can use these outputs to disable the external driver, as shown in Figure 8. The sequencing of these outputs is shown in Figure 5.

P_{A1}, P_{A2}, P_{B1}, and P_{B2}: The phase outputs pull to ground sequentially to cause motor stepping, according to the state diagram of Figure 5. The sequence of stepping on these lines, as with the L_A and L_B lines is controlled by the STEP input, the DIR input, and the $\overline{HSM}$ input. Caution: If these outputs or any other IC pins are pulled too far below ground either continuously or in a transient, step memory can be lost. It is recommended that these pins be clamped to ground and supply with high-speed diodes when driving inductive loads such as motor windings or solenoids. This clamping is very important because one side of the winding can "kick" in a direction opposite the swing of the other side.

L_A and L_B: These outputs pull to V_{ss} when their corresponding monostable is active, and will remain high until the monostable on time elapses. Before and after, these outputs are high-impedance. For detailed timing information, consult Figure 5.

STEP: This logic input clocks the logic in the UC3517 on every falling edge. Like all other UC3517 inputs, this input is TTL/CMOS compatible, and should not be pulled below ground.

DIR: This logic input controls the motor rotation direction by controlling the phase output sequence as shown in Figure 5. This signal must be stable 400nS before a falling edge on STEP, and must remain stable through the edge to insure correct stepping.

$\overline{HSM}$: This logic input switches the UC3517 between half-stepping ($\overline{HSM}$ = low) and full-stepping ($\overline{HSM}$ = high) by controlling the phase output sequence as shown in Figure 5. This line requires the same set-up time as the DIR input, and has the same hold requirement.

INH: When the inhibit input is high, the phase and ϕ outputs are inhibited (high-impedance). STEP pulses received while inhibited will continue to update logic in the IC, but the states will not be reflected at the outputs until inhibit is pulled low. In stepper motor systems, this can be used to save power or to allow the rotor to move freely for manual repositioning.

OPERATING MODES

The UC3517 is a system component capable of many different operating modes, including:

Unipolar Stepper Driver: In its simplest form, the UC3517 can be connected to a stepper motor as a unipolar driver. L_A, L_B, RC and V_{ss} are not used, and may be left open. All other system design considerations mentioned above apply, including choice of motor supply V_{mm}, undershoot diodes, and timing considerations.

Unipolar Bilevel Stepper Driver: If increased step rates are desired, the application circuit of Figure 6 makes use of the monostables and emitter followers as well as the configuration mentioned above to provide high-voltage pulses to the motor windings when any phase is turned on. For a given dissipation level, this mode offers faster step rates, and very little additional electrical noise.

The choice of monostable components can be estimated based on the timing relationship ot motor current and voltage: $V = Ldl/dt$. Assuming a fixed secondary supply voltage (V_{ss}), a fixed winding inductance (L_m), a desired winding peak current (I_w), and no back EMF from the motor, we can estimate that $R_T\ C_T = 1.449\ I_w L_m / V_{ss}$. In practice, these calculations should be confirmed and adjusted to accommodate for effects not modeled.

Voltage-Doubler Mode: The UC3517 can also be used to generate higher voltages than available with system power supplies using capacitors and diodes. Figure 9 shows how this might be done, and gives some estimates for component values.

Higher-Current Operation: For systems requiring more than 350mA of drive per phase the UC3517 can be used in conjunction with discrete power transistors or power driver ICs, like the L298. These can be connected as current gain devices that turn on when the phase outputs turn on.

Bipolar Motor Driver: Bipolar motors can be controlled by the UC3517 with the addition of bipolar integrated drivers such as the UC3717A (Figure 8) and the L298, or discrete devices. Care should be taken with discrete devices to avoid potential cross-conduction problems.

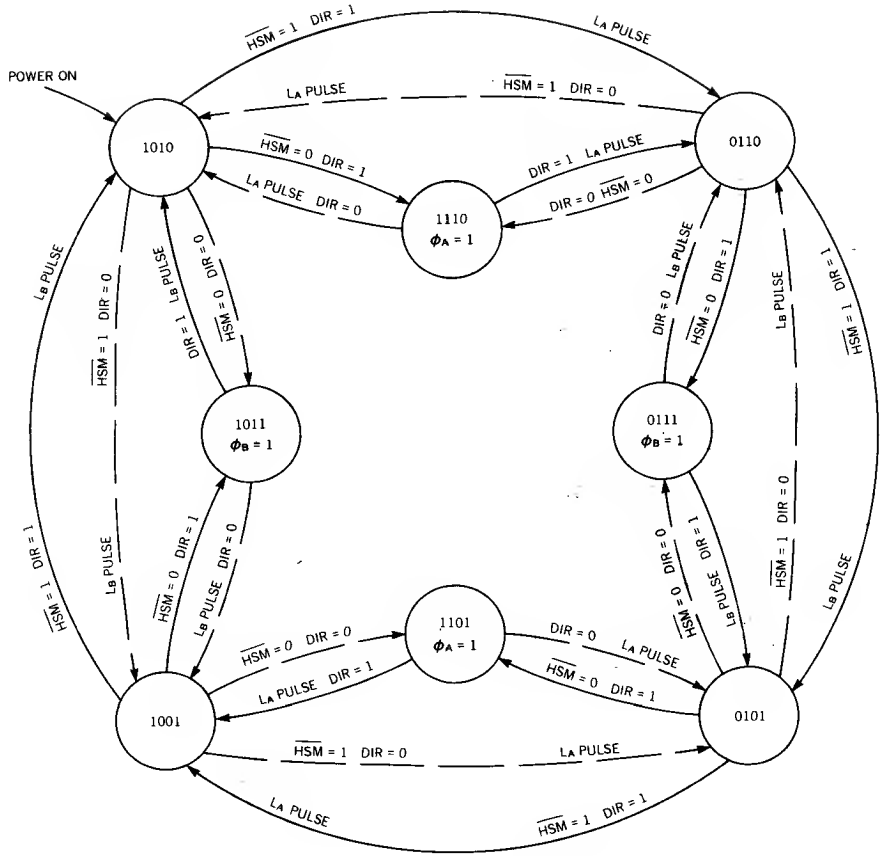


Figure 5. Logic Flow Graph

LOGIC FLOW GRAPH

The UC3517 contains a bidirectional counter which is decoded to generate the correct phase and ϕ outputs. This counter is incremented on every falling edge of the STEP input. Figure 5 shows a graph representing the counter sequence, inputs that determine the next state (DIR and $\overline{HSM}$), and the outputs at each state. Each circle represents a unique logic state, and the four inside circles represent the half-step states.

The four bits inside the circles represent the phase outputs in each state (P_{A1}, P_{A2}, P_{B1}, and P_{B2}). For example, the circle labeled 1010 is immediately entered when the device is powered up, and represents P_{A1} off ("1" or high), P_{A2} on ("0" or low), P_{B1} off ("1" or high), and P_{B2} on ("0" or low). The ϕ_A and ϕ_B outputs are both low (unidentified).

The arrows in the graph show the state changes. For example, if the IC is in state 0110, DIR is high, $\overline{HSM}$ is high, and STEP falls, the next state will be 0101, and a pulse will be generated on the L_B line by the monostable.

Inhibit will not effect the logic state, but it will cause all phase outputs and both ϕ outputs to go high (off). A falling edge on STEP will still cause a state change, but inhibit will have to toggle low for the state to be apparent.

A falling edge on STEP with $\overline{HSM}$ high will cause the counter to advance to the next full step state regardless of whether or not it was in a full step state previously.

No L_A or L_B pulses are generated entering half-states.

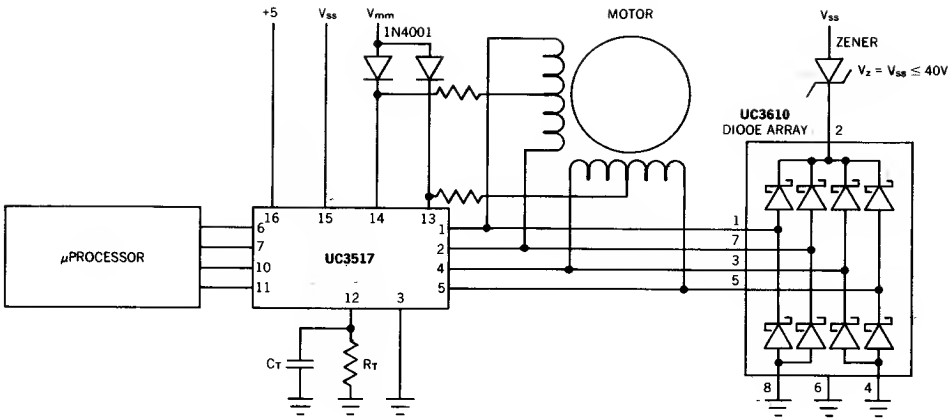


Figure 6. Bilevel Motor Driver

For applications requiring very fast step rates, a zener diode permits windings to discharge at higher voltages, and higher rates. Driver transistor breakdown must be considered when selecting V_{ss} and zener voltage to insure that the outputs will not overshoot past 40V. If the zener diodes are not used and UC3610 pin 2 is connected directly to V_{ss}, then higher V_{ss} can be used.

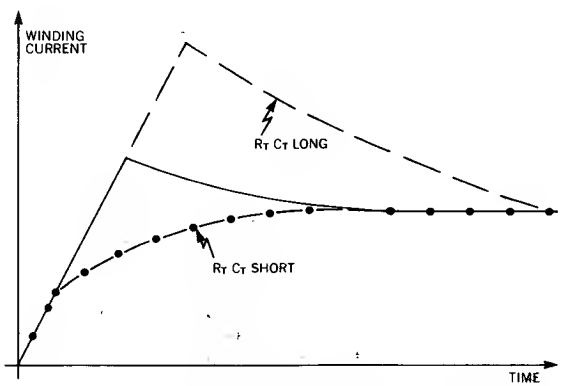


Figure 7. Effects of Different R_T & C_T on Bilevel Systems

Experimental selection of R_T and C_T allow the designer to select a small amount of winding current overshoot, as shown above. Although the overshoot may exceed the continuous rated current of the winding and the drive transistors, the duration can be well controlled. Average power dissipation for the driver and motor must be considered when designing systems with intentional overshoot, and must stay within conservative limits for short duty cycles.

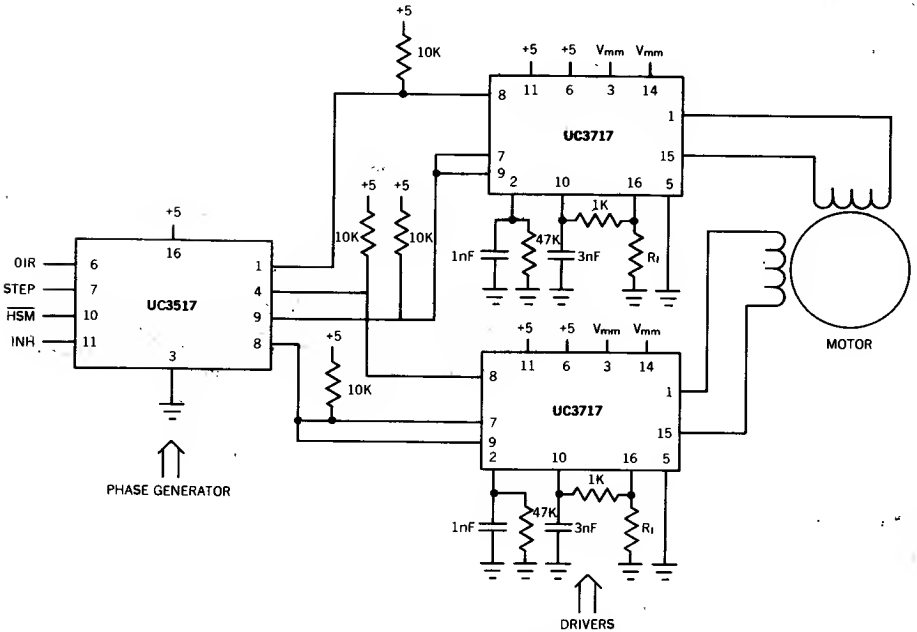


Figure 8. Interface to UC3717 Bipolar Driver

In this application, the ϕ_A and ϕ_B outputs of the UC3517 are connected to the current program inputs of the UC3717. This allows the UC3517 inhibit signal to inhibit the UC3717, and also allows half-step operation of the UC3717. Peak motor winding current will be limited to approximately .42V/R_I by chopping.

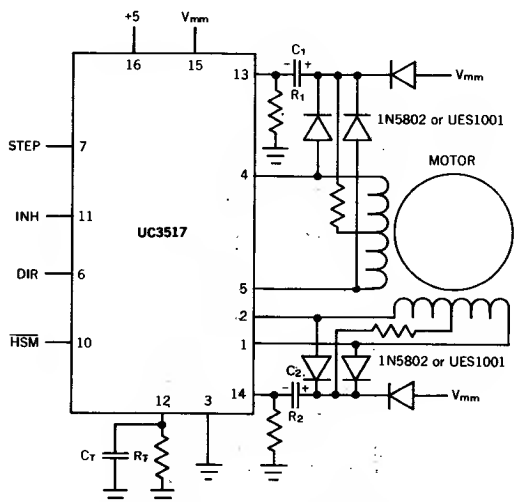


Figure 9. Using the UC3517 as a Voltage Doubler

Although component values can be best optimized experimentally, good starting values speed development. For this design, start with:

$R_T C_T = 3 L_w/R_w$

$C_1 = C_2 = L_w I_r/R_w$

$R_1 = R_2 = 2.9 T_{min}/C_1$

where:

L_w is winding inductance,

R_w is winding resistance,

I_r is rated winding current, and

T_{min} is minimum step period expected.

INTEGRATED CIRCUITS

UNITRODE

DUAL Schottky Diode Bridge

UC1610
UC3610

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

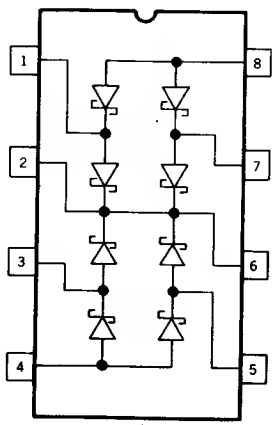
This single monolithic chip is fabricated in both hermetic cerdip and copper-leaded plastic minidip packages. The UC1610 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 ..... 1A
  UC3610 ..... 3A
Power Dissipation at T_A = 70°C 1W
  Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE

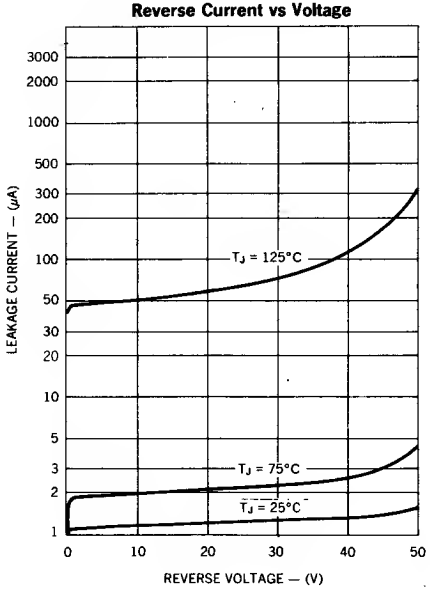


ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = 25°C except as noted.) T_A=T_J

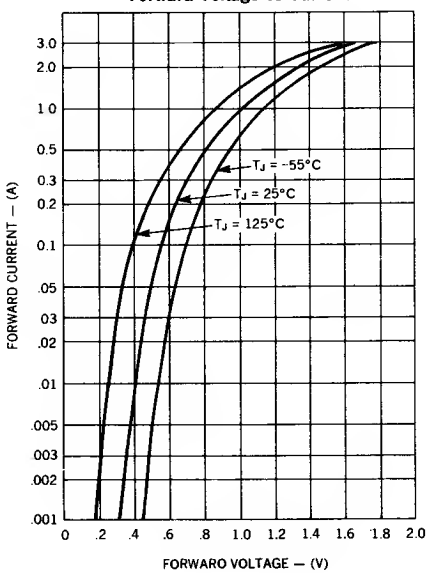
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA I_F = 1A	0.4 0.8	0.5 1.0	0.7 1.3	V
Leakage Current	V_R = 40V V_R = 40V, T_J = 100°C		.01 0.1	0.1 1.0	mA
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

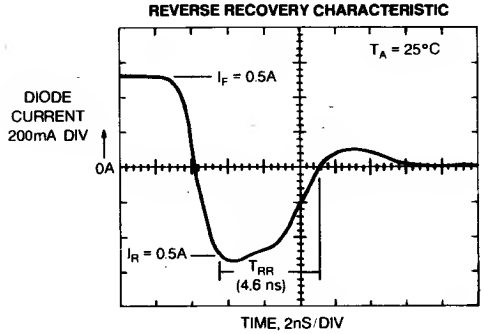
Reverse Current vs Voltage



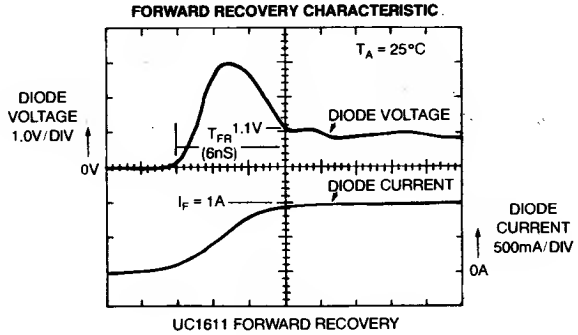
Forward Voltage vs Current



REVERSE RECOVERY CHARACTERISTIC



FORWARD RECOVERY CHARACTERISTIC



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INTEGRATED CIRCUITS

UNITRODE

Quad Schottky Diode Array

UC1611
UC3611

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

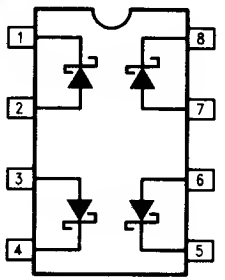
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic MINIDIP packages. The UC1611 in ceramic is designed for −55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
  UC1611 ..... 1A
  UC3611 ..... 3A
Power Dissipation at T_A = +70°C 1W
  Derate 12.5 mW/°C above +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

CONNECTION DIAGRAM

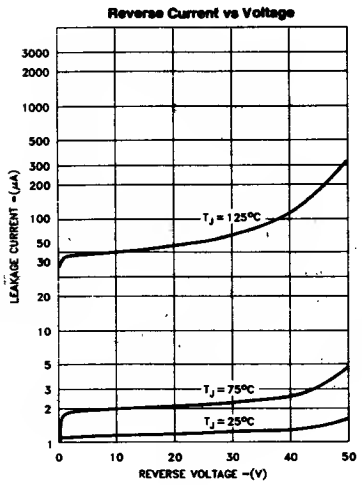
DIL-8 (TOP VIEW)
J or N PACKAGE

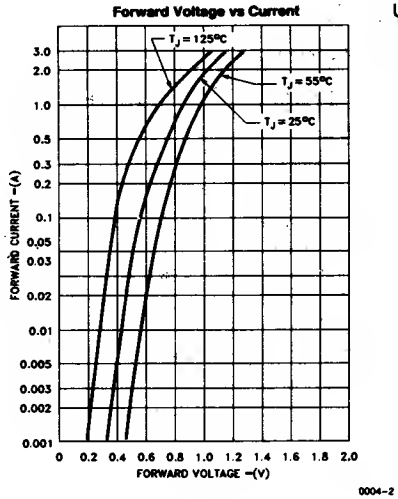


ELECTRICAL CHARACTERISTICS (All specifications apply to each individual diode. T_J = +25°C except as noted.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100 mA I_F = 1A	0.4	0.5 0.9	0.7 1.2	V
Leakage Current	V_R = 40V V_R = 40V, T_J = +100°C		0.01 0.1	0.1 1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

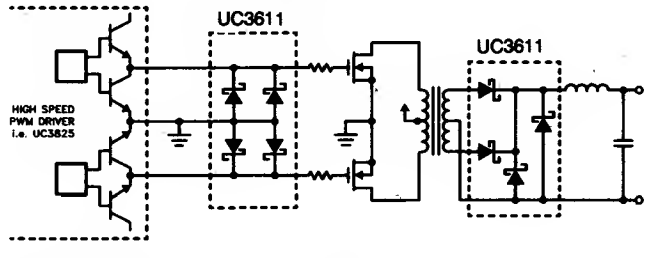
Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.



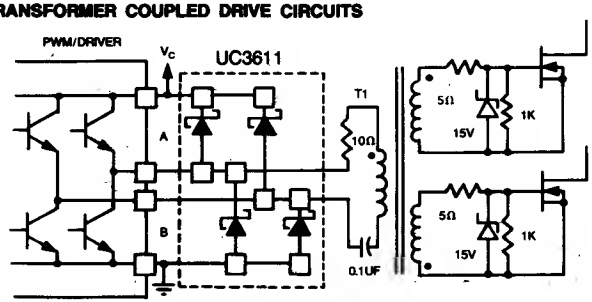


TYPICAL APPLICATIONS

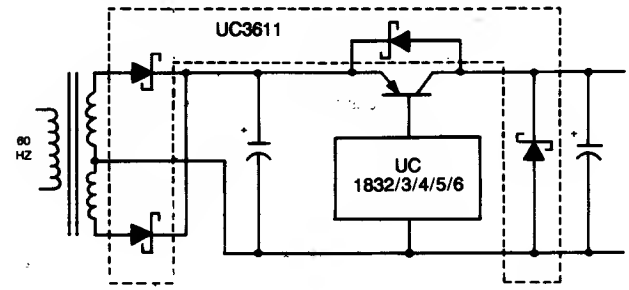
A. CLAMP DIODES - PWMS AND DRIVERS



B. TRANSFORMER COUPLED DRIVE CIRCUITS



C. LINEAR REGULATORS



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INTEGRATED CIRCUITS

UNITRODE

UC1620
UC3620

Switchmode Driver For 3-ϕ Brushless DC Motors

FEATURES

- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Servo Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- Available in V, VH Commercial, and JP Hermetic Military Package

DESCRIPTION

The UC3620 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/μs for any load condition.

The UC1620JP is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC3620V (and VH) is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

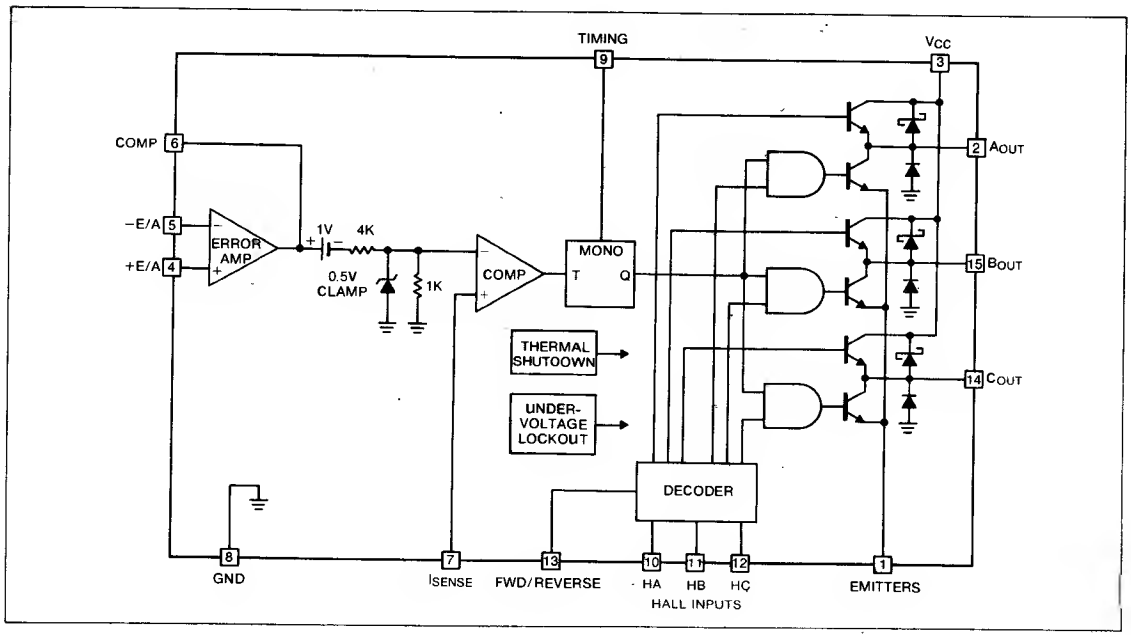
Supply Voltage, V_{cc} 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), Io 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Analog Inputs ..... -0.3 to +V_{cc}
Logic Inputs ..... -0.3 to +V_{cc}
Total Power Dissipation (at T_{CASE} = 75°C) (V pkg.) 25W
Total Power Dissipation (at T_{CASE} = 75°C) for JP Package 15W
Storage and Junction Temperature ..... -40°C to +150°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

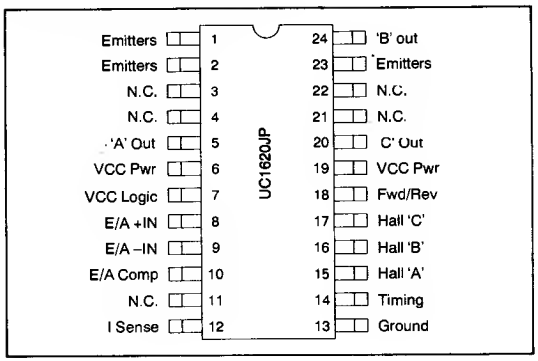
THERMAL DATA

Thermal Resistance Junction Case (V, JP), θ_{jc} ..... 3°C/W Max
Thermal Resistance Junction-Ambient (V, JP), θ_{jc} .... 35°C/W Max

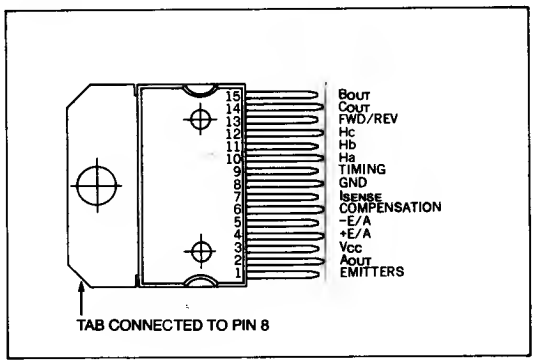
BLOCK DIAGRAM



CONNECTION DIAGRAM
JP HERMATIC POWER DOIL



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for 3620; T_A = 55°C to +125°C for UC1620; $V_{CC\ (PIN\ 3)}$ = 20V, R_T = 20V, R_T = 10k C_T = 2.2nF) T_A=T_J

		UC3620			UC1620			
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Error Amplifier Section								
Input Offset Voltage			1.5	10		1.5	10	mV
Inut Bias Current			–.25	–2 0		–.25	–2.0	uA
Input Offset Current			15	250		15	250	nA
Common Mode Range	V_{CC} = 8V TO 40V	0		V_{IN}–2	0		V_{IN}–2	V
Open Loop Gain	Δ $V_{PIN\ 6}$ = 1V TO 4V	80	100		75	100		dB
Unity Gain Bandwidth	T_J = 25°C, Note 2		0 8			0.8		MHz
Output Sink Current	$V_{PIN\ 6}$ = 1V		2			2		mA
Output Source Current	$V_{PIN\ 6}$ = 4V		8			8		mA
Current Sense Section								
Input Bias Current			–2.0	–5		–2 0	–5	uA
Internal Clamp		.425	0.5	575	405	0 5	595	V
Divider Gain		.180	0.2	220	170	0 2	230	V/V
Internal Offset Voltage		.8	1 0	1 2	75	1.0	1 25	V
Timing Section								
Output Off Time		18	20	22	17	20	23	µs
Upper Mono Threshold			5 0			5.0		V
Lower Mono Threshold			2 0			2 0		V
Decoder Section								
High-Level Input Voltage		2 2			2 5			V
Low-Level Input Voltage				0 8			0 8	V
High-Level Input Current				10			10	uA
Low-Level Input Current		–10			–10			uA
Output Section								
Output Leakage Current	V_{CC} = 40V			500			1 500	uA
V_F, Schottky Diode	I_O = 2A		1 5	2.0		1 5	2 0	V
V_F, Substrate Diode	I_O = 2A		2 2	3.0		2.2	3.0	V
Total Output Voltage Drop	I_O = 2A, Note 3		3.0	3 6		3 0	3.6	V
Output Rise Time	R_L = 44Ω		150			150		ns
Output Fall Time	R_L = 44Ω		150			150		ns

Note 2. These parameters, although guaranteed over the recommended operating conditions, ere not 100% tested in production

Note 3. The total voltage drop is defined as the sum of both top and bottom side driver.

5

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for UC3620, T_A = 55°C to +125°C for UC1620 $V_{CC\ (PIN\ 3)A}$ = 20V, R_T = 10K, C_T = 2.2nF) $T_A = T_J$

		UC3620			UC1620			
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Under-Voltage Lockout								
Stert-Up Threshold				8.0			8.0	V
Threshold Hysteresis			0.5			0.5		V
Thermal Shutdown								
Junction Temperature		150		180	150		180	°C
Total Standby Current								
Supply Current			32	55		32	55	mA

TABLE 1

STEP	FWD/ REV	H_a	H_b	H_c		A_{OUT}	B_{OUT}	C_{OUT}
1	1	1	0	1		H	L	0
2	1	1	0	0		H	0	L
3	1	1	1	0		0	H	L
4	1	0	1	0		L	H	0
5	1	0	1	1		L	0	H
6	1	0	0	1		0	L	H
1	0	1	0	1		L	H	0
2	0	1	0	0		L	0	H
3	0	1	1	0		0	L	H
4	0	0	1	0		H	L	0
5	0	0	1	1		H	0	L
6	0	0	0	1		0	H	L

H = HIGH OUTPUT
L = LOW OUTPUT
0 = OPEN OUTPUT

CIRCUIT DESCRIPTION

The UC3620 is designed for implementation of a complete 3-Φ brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

As shown in Table 1, the decoder employs a 120 electrical degree hall decode scheme (others available via mask programming) to decode and drive each of three high current totem pole output stages. A forward/reverse signal, pin 13, is used to provide direction. At any point in time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by turning the sink driver off during the monostable reset time, producing a fixed off-time chop mode. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses. Hall lines require pull-up resistors.

CURRENT SENSING

Referring to Figure 1, emitter current is sensed across R_S and fed back through a low pass filter to the current sense pin 7. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1KΩ and 1000pF range.

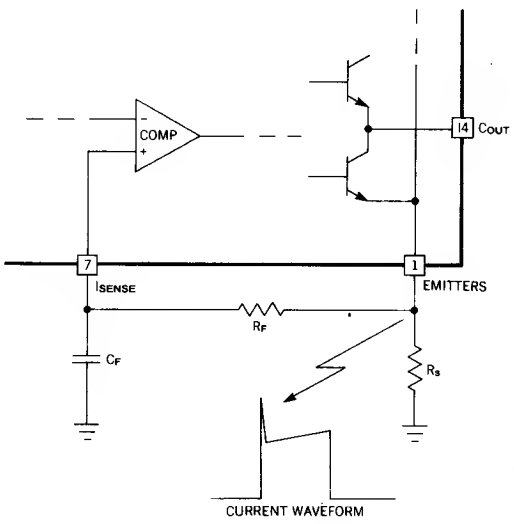


Figure 1. Current Sense Filter

TIMING

An R-C time constant on pin 9 is used by the monostable to generate a fixed off time at the outputs according to the formula:

$T_{OFF} = .916\ R_T C_T$.

As the peak current in the emitters approaches the value at the minus (−) input of the on-board comparator, the monostable is triggered, causing the outputs to be turned off. On time is determined by the amount of time required for motor current to increase to the value required to re-trip the monostable. A timing sequence of these events is shown in Figure 2.

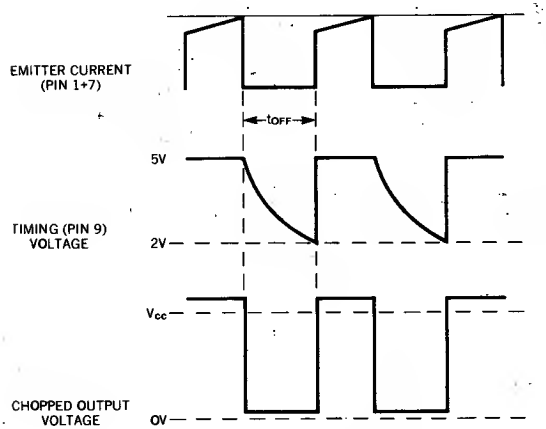


Figure 2. Chopped Mode Timing Diagram

CURRENT LIMIT

Since peak current is being controlled at all times by the internal comparator, a simple voltage clamp at its negative (−) input will limit peak current to a maximum value. A fixed 0.5V internal clamp has been included on the UC3620, and any current spike in the output which generates a sensed voltage greater than 0.5V will immediately shut down the outputs. Actual peak current values may be programmed by selecting the appropriate value of R_S according to the formula:

$$R_S = 0.5/I_{CURRENT\ LIMIT}$$

ERROR AMPLIFIER

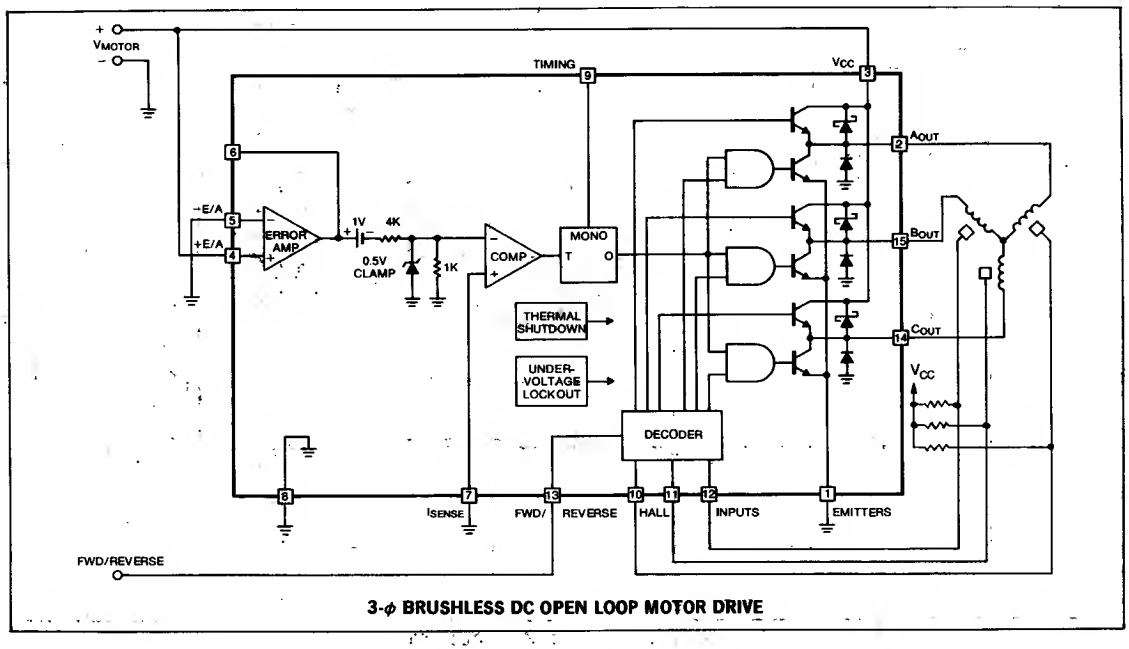
A high performance, on-board error amplifier is included to facilitate implementing closed loop motor control. Error voltage generation and loop compensation are easily accomplished by appropriately configuring the gain and feedback of this amplifier. To provide a larger dynamic signal range at the output of the error amplifier, a divide by 5 resistor network is used to reduce the error signal level before applying to the internal comparator. In addition, a one volt offset has been introduced at the output of the error amplifier to guarantee control down to zero current in the output stages. Since this offset is divided by the open loop gain of the feedback loop, it has virtually no effect on closed loop performance.

PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-stated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

5

TYPICAL APPLICATIONS



3-ϕ BRUSHLESS DC OPEN LOOP MOTOR DRIVE

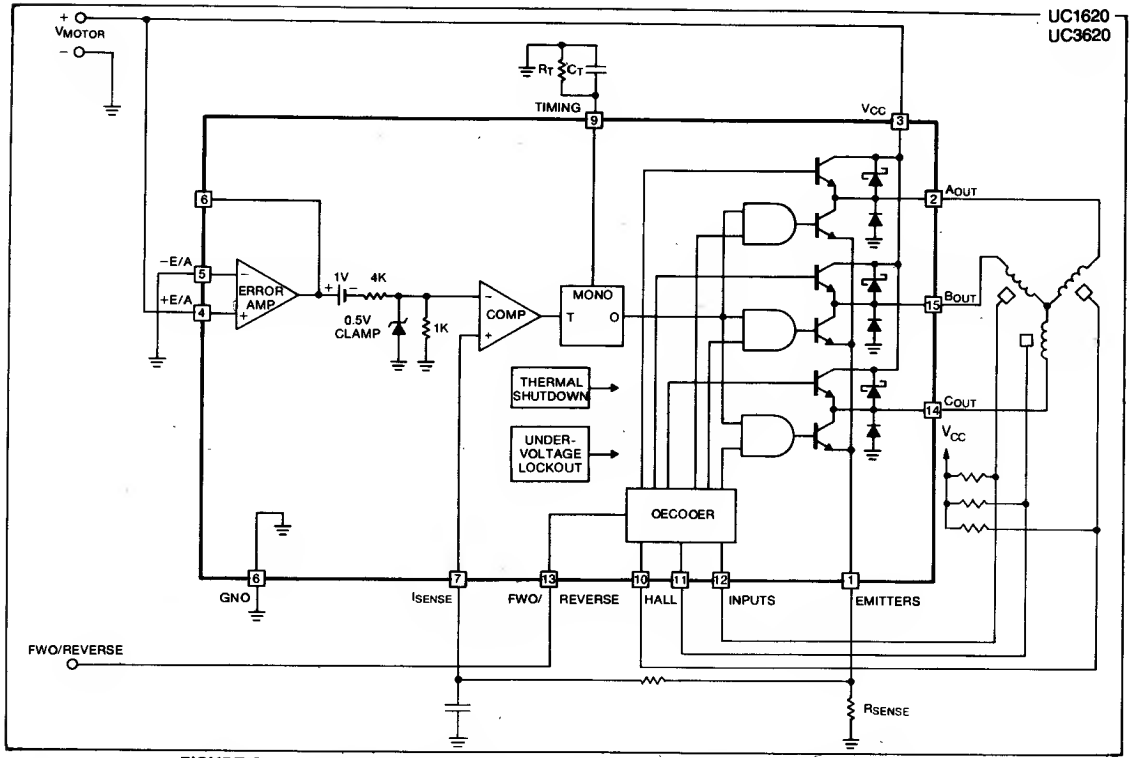
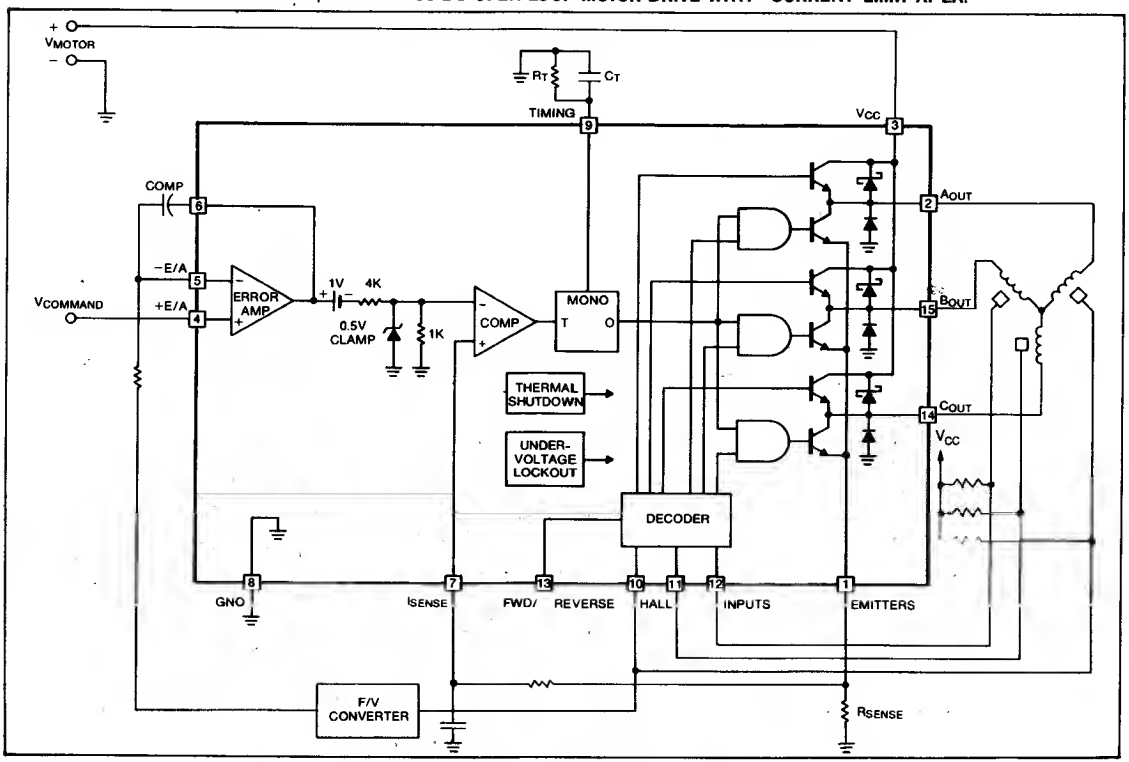


FIGURE 2. — 3-ϕ BRUSHLESS DC OPEN LOOP MOTOR DRIVE WITH CURRENT LIMIT AT 2A.



CLOSED LOOP SPEED CONTROL SERVO

Brushless DC Motor Controller

FEATURES

- Drives Power MOSFETs or Power Darlingtons directly
- 50V Open Collector High-Side Drivers
- Latched Soft Start
- High-speed Current-Sense Amplifier with Ideal Diode
- Pulse-by-pulse and Average Current Sensing
- Over-voltage and Under-voltage Protection
- Direction Latch for Safe Direction Reversal
- Tachometer
- Trimmed Reference Sources 30mA
- Programmable Cross-conduction Protection
- Two-quadrant and four-quadrant operation

DESCRIPTION

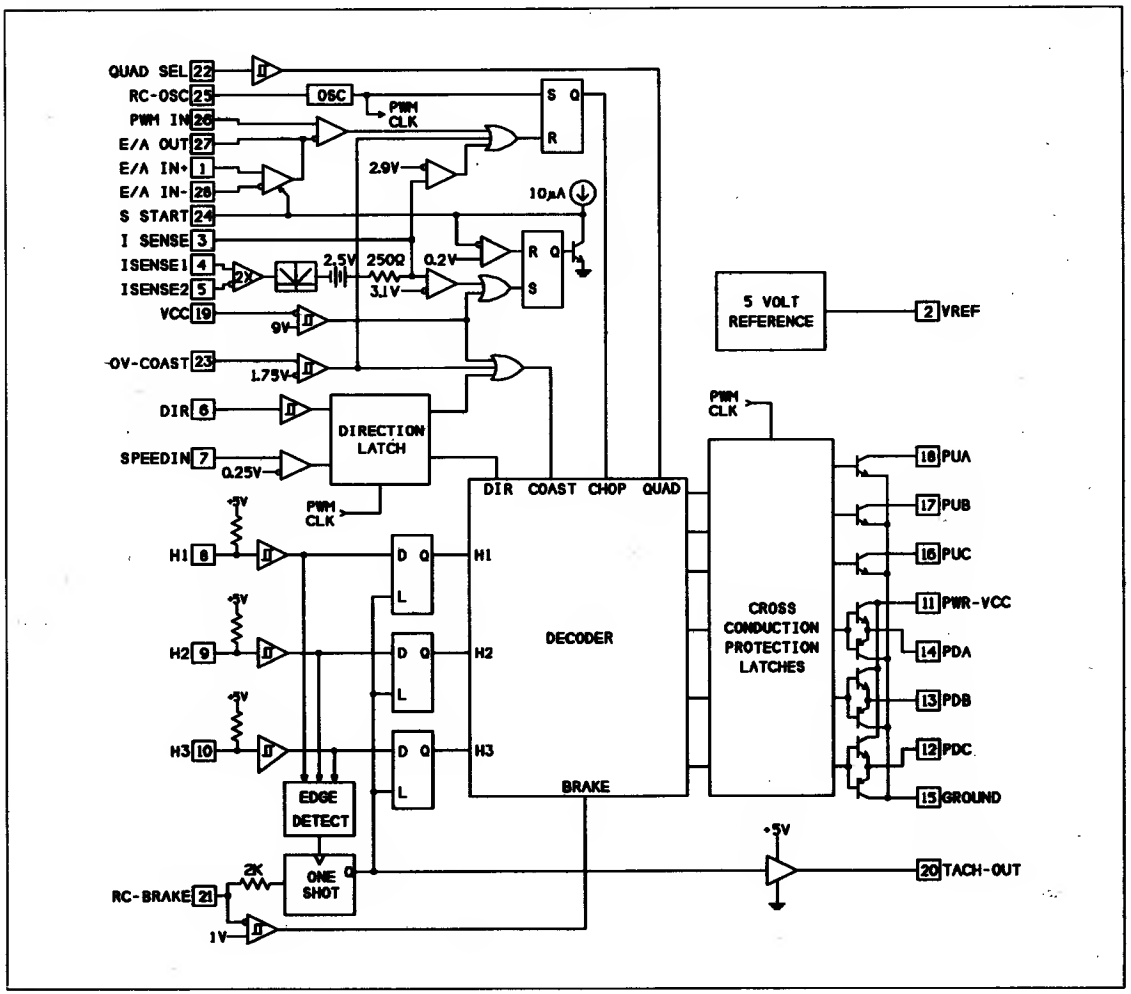
The UC1625 and UC3625 motor controller ICs integrate most of the functions required for high-performance brushless DC motor control into one package. When coupled with external power MOSFETs or Darlingtons, these ICs perform fixed-frequency PWM motor control in either voltage or current mode while implementing closed loop speed control and braking with smart noise rejection, safe direction reversal, and cross–conduction protection.

Although specified for operation from power supplies between 10V and 18V, the UC1625 can control higher voltage power devices with external level-shifting components. The UC1625 contains fast, high-current push-pull drivers for low-side power devices and 50V open-collector outputs for high-side power devices or level shifting circuitry.

The UC1625 is characterized for operation over the military temperature range of –55°C to +125°C; while the UC3625 is characterized from 0°C to 70°C.

NOTE: ESD Protection to 2kV

BLOCK DIAGRAM



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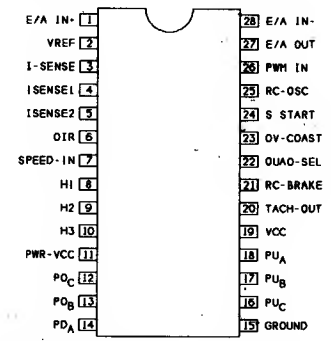
ABSOLUTE MAXIMUM RATINGS (Note 1)

VCC Supply Voltage . . . . . +20V
POWER VCC Supply Voltage . . . . . +20V
PWM IN – . . . . . 0.3 to 6V
E/A IN+, E/A IN– . . . . . –0.3 to 12V
ISENSE1, ISENSE2 . . . . . –1.3 to 6V
OV–COAST, DIR, SPEEDIN, H1, H2, H3,
S START, QUAD SEL . . . . . –0.3 to 8V
PU Output Voltage . . . . . –0.3 to 50V
PU Output Current . . . . . +200 mA continuous
PD Output Current . . . . . ±200 mA continuous
E/A Output Current . . . . . ±10 mA
I SENSE Output Current . . . . . –10 mA
TACH–OUT Output Current . . . . . ±10 mA
VREF Output Current . . . . . –50 mA continuous
Operating Temperature Range UC1625 . . . . . –55°C to 125°C
Operating Temperature Range UC3625 . . . . . 0°C to 70°C

Note 1: Currents are positive into and negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-28 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for: T_A=25°C; PWR-VCC=VCC=12V; R_{OSC}=20K to Vref; C_{OSC}=2nF; R_{TACH}=33K; C_{TACH}=10nF; and all outputs unloaded. T_A=T_j

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
OVERALL					
Supply Current	Over Operating Range		14.5	30.0	mA
VCC Turn–On Threshold	Over Operating Renge	8.85	8.95	9.45	V
VCC Turn–Off Threshold	Over Operating Range	7.75	8.05	8.55	V
OVERVOLTAGE/COAST					
OV–COAST Inhibit Threshold	Over Operating Renge	1.65	1.75	1.85	V
OV–COAST Restart Threshold		1.55	1.65	1.75	V
OV–COAST Hysteresis		0.05	0.10	0.15	V
OV–COAST Input Current		–10	–1	0	µA
LOGIC INPUTS					
H1, H2, H3 Low Threshold	Over Operating Range	0.8	1.0	1.2	V
H1, H2, H3 High Threshold	Over Opereting Renge	1.6	1.9	2.0	V
H1, H2, H3 Input Current	Over Opereting Renge, To 0V	–400	–250	–120	µA
QUAD SEL, DIR Thresholds	Over Operating Renge	0.8	1.4	2.0	V
QUAD SEL, DIR Hysteresis			0.6		V
QUAD SEL Input Current		–30	50	150	µA
DIR Input Current		–30	–1	30	µA
PWM AMP/COMPARATOR					
E/A IN+, E/A IN– Input Current	To 2.5V	–5.0	–0.1	+5.0	µA
PWM IN Input Current	To 2.5V	0	3	30	µA
Error Amp Input Offset	0V<VCOMMON-MODE<3V	–10		10	mV
Error Amp Voltage Gain		70	90		dB
E/A OUT Range		0.25		3.50	V
S START Pull-Up Current	To 0V	–16	–10	–5	µA
S START Discharge Current	To 2.5V	0.1	0.4	3.0	mA
S START Restart Threshold		0.1	0.2	0.3	V

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
CURRENT AMP					
Gain	ISENSE1=.3V, ISENSE2=.5V to .7V	1.75	1.95	2.15	V/V
Level Shift	ISENSE1=.3V, ISENSE2=.3V	2.4	2.5	2.65	V
Peek Current Threshold	ISENSE1=0V, Force ISENSE2	0.14	0.20	0.26	V
Over Current Threshold	ISENSE1=0V, Force ISENSE2	0.26	0.30	0.36	V
ISENSE1, ISENSE2 Input Current	To 0V	–850	–320	0	µA
ISENSE1, ISENSE2 Offset Current	To 0V		±2	±12	µA
Renge ISENSE1, ISENSE2		–1		2	V
TACHOMETER/BRAKE					
TACH/OUT High Level	Over Operating Range, 10K to 2.5V	4.7	5	5.3	V
TACH/OUT Low Level	Over Operating Range, 10K to 2.5V			0.2	V
On Time		170	220	280	µs
On Time Change With Temp	Over Operating Range		.1		%
RC–BRAKE Input Current	To 0V	–4.0	–1.9		mA
Threshold to Brake, RC–BRAKE	Over Operating Range	0.8	1.0	1.2	V
Breke Hysteresis, RC–BRAKE			0.09		V
SPEED IN Threshold	Over Operating Range	220	257	290	mV
SPEED IN Input Current		–30	–5	30	µA
LOW-SIDE DRIVERS					
Voh, –1mA, Down From Vcc	Over Operating Range		1.60	2.1	
V Voh, –50mA, Down From Vcc	Over Operating Range		1.75	2.2	V
Vol, 1mA	Over Opereting Range		0.05	0.4	V
Vol, 50mA	Over Operating Range		0.36	0.8	V
Rise/Fall Time	10% to 90% Slew Time, into 1nF		50		ns
HIGH-SIDE DRIVERS					
Vol, 1mA	Over Operating Range		0.1	0.4	V
Vol, 50mA	Over Operating Range		1.0	1.8	V
Leekage Current	Output Voltage=50V			25	µA
Fall Time	10% to 90% Slew Time, 50mA Loed		50		ns
OSCILLATOR					
Frequency		40	50	60	kHz
Frequency	Over Operating Range	35		65	kHz
REFERENCE					
Output Voltage		4.9	5.0	5.1	V
Output Voltage	Over Operating Range	4.7	5.0	5.3	V
Load Regulation	0mA to –20mA Load	–40	–5		mV
Line Regulation	10V to 18V VCC	–10	–1	10	mV
Short Circuit Current	Over Operating Range	50	100	150	mA
MISCELLANEOUS					
Output Turn-On Delay			1		µs
Output Turn-Off Delay			1		µs

5

PIN DESCRIPTIONS

DIR, SPEED IN

The position decoder logic translates the Hall signals and the DIR signal to the correct driver signals (PUs and PDs). To prevent output stage damage, the signal on DIR is first loaded into a direction latch, then shifted through a two-bit register.

As long as SPEEDIN is less than 250mV, the direction latch is transparent. When SPEEDIN is higher than 250mV, the direction latch inhibits all changes in direction. SPEEDIN can be connected to TACH-OUT through a filter, so that the direction latch is only transparent when the motor is spinning slowly, and has too little stored energy to damage power devices.

Additional circuitry detects when the input and output of the direction latch are different, or when the input and output of the shift register are different, and inhibits all output drives during that time. This can be used to allow the motor to coast to e safe speed before reversing.

The shift register guarantees that direction can't be changed instantaneously. The register is clocked by the PWM oscillator, so the delay between direction changes is always going to be between one and two oscillator periods. At 40kHz, this corresponds to a delay of between 25µs and 50µs. Regardless of output stage, 25µs dead time should be adequate to guarantee no overlap cross-conduction.

E/A IN+, E/A IN-, E/A OUT, PWM IN

E/A IN+ and E/A IN- are not internally committed to allow for a wide variety of uses. They can be connected to the ISENSE, to TACH-OUT through a filter, to an external command voltege, to a D/A converter for computer control, or to another op amp for more elegant feedbeck loops. The error amplifier is compensated for unity gain stebility, so E/A OUT can be tied to E/A IN- for feedback and major loop compensation.

E/A OUT and PWM IN drive the PWM comparator. For voltage-mode PWM systems, PWM IN can be connected to RC-OSC. The PWM comparator clears the PWM latch, commanding the outputs to chop.

The error amplifier can be biased off by connecting E/A IN- to a higher voltage than E/A IN+. When biesed off, E/A OUT will appear to the application as a resistor to ground. E/A OUT can then be driven by an external emplifier.

GND

All thresholds and outputs are referred to the GND pin except for the PD and PU outputs.

H1, H2, H3

The three shaft-position sensor inputs consist of hysteresis comparators with input pull-up resistors. Logic thresholds meet TTL specifications and can be driven by 5V CMOS, 12V CMOS, NMOS, or open-collectors.

Connect these inputs to motor shaft position sensors that are positioned 120 electrical degrees apart. If noisy signals are expected, zener clamp and filter these inputs with 6V zeners and an RC filter. Suggested filtering components are 1K and 2nF. Edge skew in the filter is not a problem, because sensors normelly generate modified Gray code with only one output changing at a time, but rise and fall times must be shorter than 20µs for correct tachometer operation.

Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals is inverted.

ISENSE1, ISENSE2, ISENSE

The current sense amplifier hes a fixed gain of approximately two. It also has a built-in level shift of approximately 2.5 volts. The signal appearing on ISENSE is:

$$ISENSE = 2.5V + (2 * ABS (ISENSE1 - ISENSE2))$$

ISENSE1 and ISENSE2 are interchangeable and can be used as differential inputs. The differential signal applied can be as high as +/-.5V before saturation.

If spikes are expected on ISENSE1 or ISENSE2, they are best filtered by a capacitor from ISENSE to ground. Filtering this way allows fast signal inversions to be correctly processed by the absolute value circuit. The peak-current comparator allows the PWM to enter a current-limit mode with current in the windings never exceeding approximately 0.2V/Rsense. The over current comparator provides a fail-safe shutdown in the unlikely case of cur rent exceeding 0.3V/Rsense. Then, soft start is commanded, and all outputs are turned off until the high current condition is removed.

It is often essential to use some filter driving ISENSE1 and ISENSE2 to reject extreme spikes and to control slew rate. Reasonable starting values for filter components might be 250Ω series resistors and a 5nF capacitor between ISENSE1 and ISENSE2. Input resistors should be kept small and matched to maintain gain eccuracy.

OV-COAST

This input can be used as an over-voltage shutdown in put, as a coast input, or both. This input can be driven by TTL, 5V CMOS, or 12V CMOS.

PDA, PDB, PDC

These outputs can drive the gates of N-Channel power MOSFETs directly or they can drive the bases of power darlingtons if some form of current limiting is used. They ere meant to drive low-side power devices in high-current output stages. Current available from these pins can peak as high as 0.5A. These outputs feature a true totem-pole output stage. Bewere of exceeding IC power dissipation limits when using these outputs for high continuous currents. These outputs pull high to turn a "low-side" device on (active high).

PUA, PUB, PUC

These outputs are open-collector, high-voltage drivers that are meant to drive high-side power devices in high- current output stages. These are active low outputs, meaning that these outputs pull low to command a high-side device on. These outputs can drive low-voltege PNP darlingtons end P-channel MOSFETs directly, and can drive any high-voltage device using external charge-pump techniques, transformer signal coupling, cascode level-shift transistors, or opto-isolated drive. (See applications).

PWR-VCC

This supply pin cerries the current sourced by the PD outputs. When connecting PD outputs directly to the bases of power darlingtons, the PWR-VCC pin can be current limited with a

resistor. Darlington outputs can also be "Baker Clamped" with diodes from collectors back to PWR-VCC. (See Applications)

QUAD SEL

The IC can chop power devices in either of two modes, referred to as "two-quadrant" (QUAD SEL low) and "four-quadrant" (QUAD SEL high). When two-quadrant chopping, the pull-down power devices are chopped by the output of the PWM latch while the pull-up drivers remain on. The load will chop into one commutation diode, and except for back-EMF, will exhibit slow discharge current and faster charge current. Two-quadrant chopping can be more efficient than four-quadrant.

When four-quadrant chopping, all power drivers are chopped by the PWM latch, causing the load current to flow into two diodes during chopping. This mode exhibits better control of load current when current is low, and is preferred in servo systems for equal control over acceleration and deceleration. The QUAD SEL input has no effect on operation during braking.

RC-BRAKE

Each time the TACH-OUT pulses, the capacitor tied to RC-BRAKE discharges from approximately 3.33V down to 1.67V through a resistor. The tachometer pulse width is approximately T = 0.67 RT CT, where RT and CT are a resistor and capacitor from RC-BRAKE to ground. Recommended values for RT are 10K to 500K, and recommended values for CT are 1nF to 100nF, allowing times between 5us and 10ms. Best accuracy and stability are achieved with values in the centers of those ranges.

RC-BRAKE also has another function. If RC-BRAKE pin is pulled below the brake threshold, the IC will enter brake mode. This mode consists of turning off all three high-side devices, enabling all three low-side devices, and disabling the tachometer. The only things that inhibit low-side device operation in braking are low-supply, exceeding peak current, OV-COAST command, and the PWM comparator signal. The last of these means that if current sense is implemented such that the signal in the current sense amplifier is proportional to braking current, the low-side devices will brake the motor with current control. (See applications) Simpler current sense connections will result in uncontrolled braking and potential damage to the power devices.

RC-OSC

The UC3625 can regulate motor current using fixed-frequency pulse width modulation (PWM). The RC-OSC pin sets oscillator frequency by means of timing resistor ROSC from the RC-OSC pin to VREF and capacitor COSC from RC-OSC to GND. Resistors 10K to 100K and capacitors 1nF to 100nF will work best, but frequency should always be below 500kHz. Oscillator frequency is approximately:

$$F = 2 / RoscCosc$$

Additional components can be added to this device to cause it to operate as a fixed off-time PWM rather than a fixed frequency PWM, using the RC-OSC pin to select the monostable time constant.

The voltage on the RC-OSC pin is normally a ramp of about 1.2V peak-to-peak, centered at approximately 1.6V. This ramp can be used for voltage-mode PWM control, or can be used for slope compensation in current-mode control.

S START

Any time that VCC drops below threshold or the sensed current exceeds the over-current threshold, the soft-start latch is set. When set, it turns on a transistor that pulls down on S START. Normally, a capacitor is connected to this pin, and the transistor will completely discharge the capacitor. A comparator senses when the NPN transistor has completely discharged the capacitor, and allows the soft-start latch to clear when the fault is removed. When the fault is removed, the soft-start capacitor will charge from the on-chip current source.

S START clamps the output of the error amplifier, not allowing the error amplifier output voltage to exceed S START regardless of input. The ramp on RC-OSC can be applied to PWM IN and compared to E/A OUT. With S START discharged below 0.2V and the ramp minimum being approximately 1.0V, the PWM comparator will keep the PWM latch cleared and the outputs off. As S START rises, the PWM comparator will begin to duty-cycle modulate the PWM latch until the error amplifier inputs overcome the clamp. This provides for a safe and orderly motor start-up from an off or fault condition.

TACH-OUT

Any change in the H1, H2, or H3 inputs loads data from these inputs into the position sensor latches. At the same time data is loaded, a fixed-width 5V pulse is triggered on TACH-OUT. The average value of the voltage on TACH-OUT is directly proportional to speed, so this output can be used as a true tachometer for speed feedback with an external filter or averaging circuit.

Whenever TACH-OUT is high, the position latches are inhibited, such that during the noisiest part of the commutation cycle, additional commutations are not possible. Although this will effectively set a maximum rotational speed, the maximum speed can be set above the highest expected speed, preventing false commutation and chatter.

VCC

This device operates with supplies between 10V and 18V. Under-voltage lockout keeps all outputs off below 7.5V, insuring that the output transistors never turn on until full drive capability is available. Bypass VCC to ground with an 0.1µF ceramic capacitor. Using a 10µF electrolytic bypass capacitor as well can be beneficial in applications with high supply impedance.

VREF

This pin provides regulated 5 volts for driving Hall-effect devices and speed control circuitry. VREF will reach +5V before VCC enables, ensuring that Hall-effect devices powered from VREF will become active before the UC3625 drives any output. Although VREF is current limited, operation over 30mA is not advised.

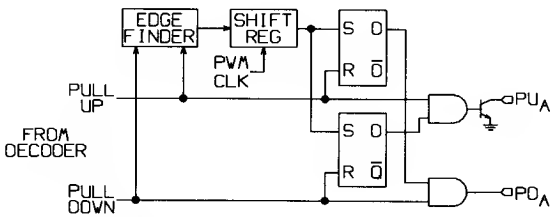
CROSS CONDUCTION PREVENTION

The UC3625 inserts delays to prevent cross conduction due to overlapping drive signals. However, some thought must always be given to cross conduction in output stage design because no amount of dead time can prevent fast slewing signals from coupling drive to a power device through a parasitic capacitance.

The UC3625 contains input latches that serve as noise blanking filters. These latches remain transparant through any phase of a motor rotation and latch immediately after an input transition is detected. They remain latched for two cycles of the PWM oscillator. At a PWM oscillator speed of 20kHz, this corresponds to 50µs to 100µs of blank time which limits maximum rotational speed to 100kRPM for a motor with six transitions per rotation or 50kRPM for a motor with 12 transitions per rotation.

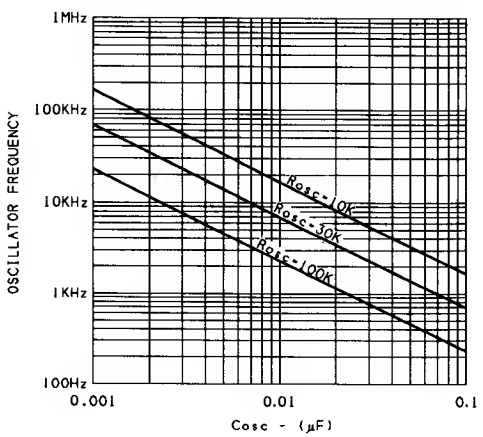
This prevents noise generated in the first 50µs of a transition from propogating to the output transistors and causing cross–conduction or chatter.

The UC3625 also contains six flip flops corresponding to the six output drive signals. One of these flip flops is set every time that an output drive signal is turned on, and cleared two PWM oscillator cycles after that drive signal is turned off. The output of each flip flop is used to inhibit drive to the opposing output. (see below) In this way, it is impossible to turn on driver PUA and PDA at the same time. It is also impossible for one of these drivers to turn on without the other driver having been off for at least two PWM oscillator clocks.

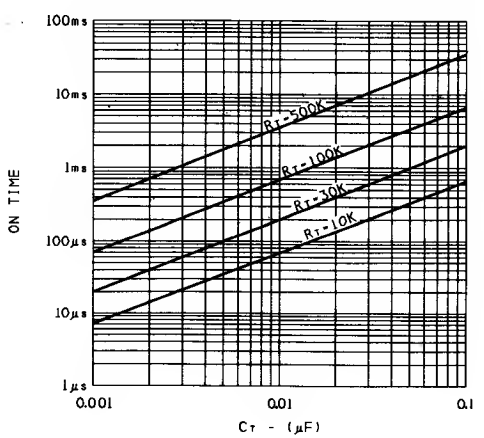


TYPICAL CHARACTERISTICS

Oscillator Frequency vs Cosc and Rosc

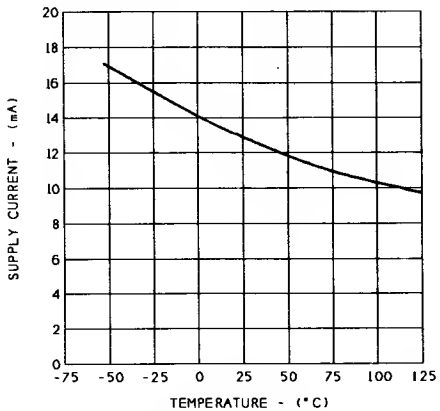


Tachometer On Time vs R_T and C_T

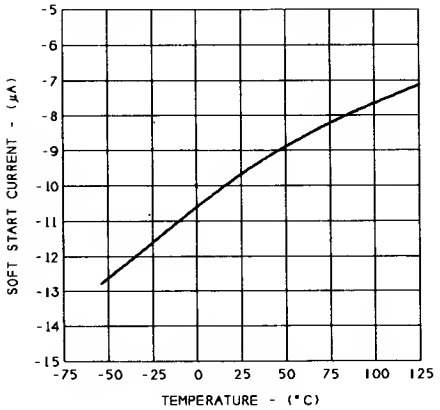


TYPICAL CHARACTERISTICS

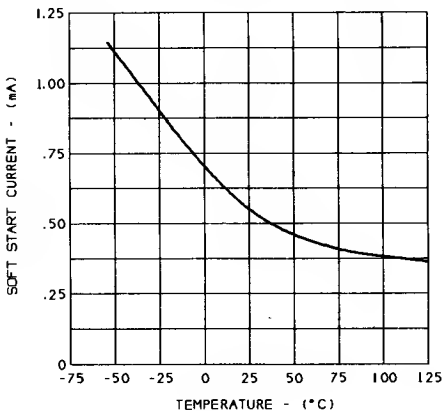
Supply Current vs Temperature



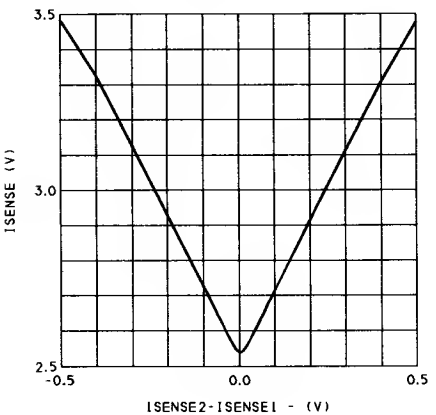
Soft Start Pull-Up Current vs Temperature



Soft Start Diacharge Current vs Temperature



Current Senae Amplifier Transfer Function



POWER STAGE DESIGN

The UC3625 is useful in a wide variety of applications, including high-power in robotics and machinery. The power output stages used in such equipment can take a number of forms, according to the intended performance and purpose of the system. Below are four different power stages with the advantages and disadvantages of each shown.

For high-frequency chopping, fast recovery circulating diodes are essential. Six are required to clamp the windings. These diodes should have a continuous current rating at least equal to the operating motor current, since diode conduction duty-cycle can be high. For low-voltage systems, Schottky diodes are preferred. In higher voltage systems, diodes such as Unitrode UHVP high voltage platinum rectifiers are recommended.

In a pulse-by-pulse current control arrangement, current sensing is done by resistor RT, through which the transistor's currents are passed (Figures A, B, and C). In these cases, RD is not needed. The low-side circulating diodes go to ground and the current sense terminals of the UC3625 (ISENSE1 and ISENSE2) are connected to RT through an RC filter. The input bias current of the current sense amplifier will cause a common mode offset voltage to appear at both inputs, so for best accuracy, keep the filter resistors below 2K and matched.

The current that flows through RT is discontinuous because of chopping. It flows during the on time of the power stage and is zero during the off time. Consequently, the voltage across RT consists of a series of pulses, occuring at the PWM frequency, with a peak value indicative of the peak motor current.

To sense average motor current instead of peak current, add another current sense resistor (RD in Figure D) to measure current in the low-side circulating diodes, and operate in four quadrant mode (pin 22 high). The negative voltage across RD is corrected by the absolute value current sense amplifier. Within the limitations imposed by Table 1, the circuit of Figure B can also sense average current.

POWER STAGE DESIGN

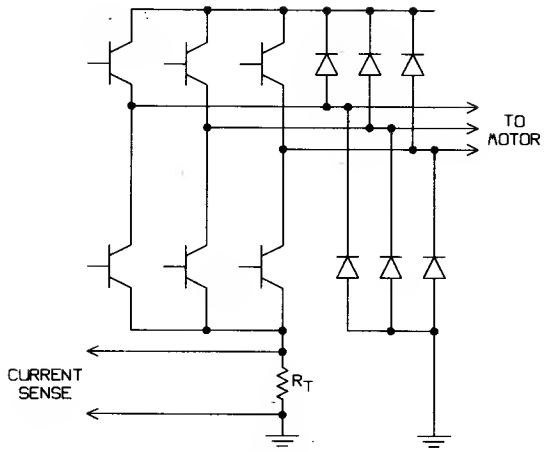


FIGURE A

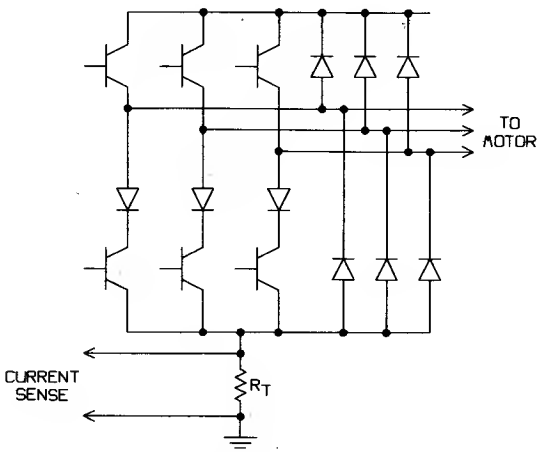


FIGURE B

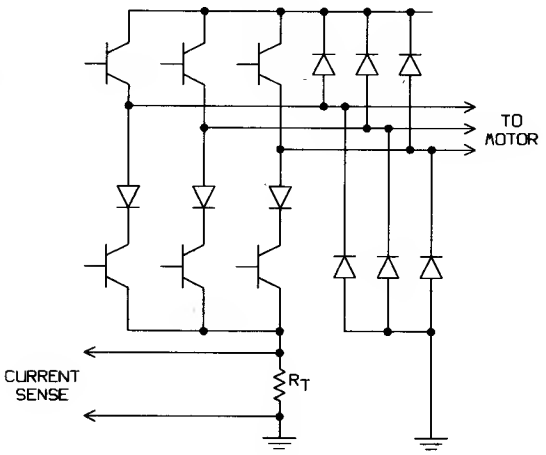


FIGURE C

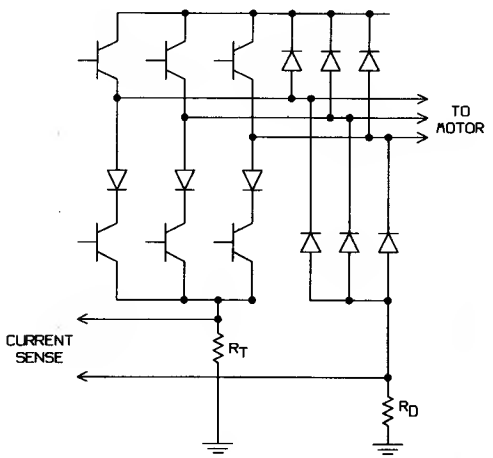
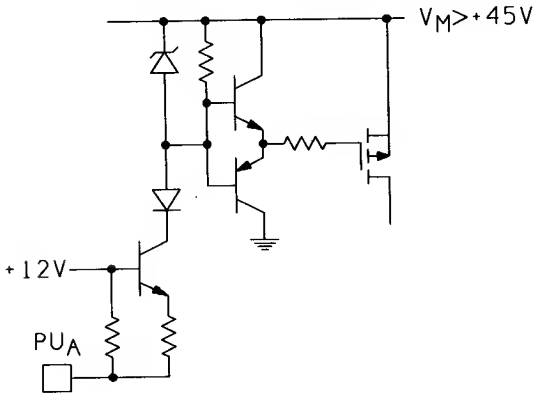


FIGURE D

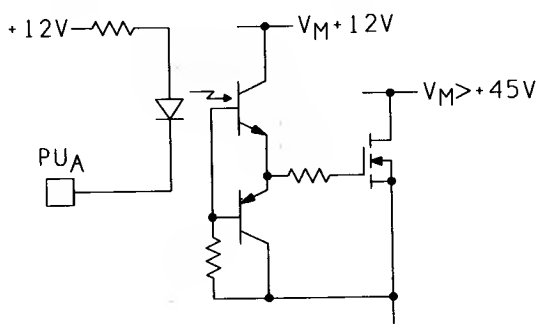
	2 QUADRANT	4 QUADRANT	SAFE BRAKING	POWER REVERSE	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
FIGURE A	YES	NO	NO	NO	YES	NO
FIGURE B	YES	YES	NO	IN 4QUAD MODE ONLY	YES	YES
FIGURE C	YES	YES	YES	YES	YES	NO
FIGURE D	YES	YES	YES	YES	YES	YES

FAST HIGH-SIDE P-CHANNEL DRIVER



For drives where speed is critical, P-Channel MOSFETs can be driven by emitter followers. Here, both the level shift NPN and the PNP must withstand high voltages. A zener diode is used to limit gate-source voltage on the MOSFET. A series gate resistor is not necessary, but always advisable to control overshoot and ringing.

OPTOCOUPLED N-CHANNEL HIGH-SIDE DRIVER



High-voltage optocouplers can quickly drive high-voltage MOSFETs if a boost supply of at least 10 volts greater than the motor supply is provided. To protect the MOSFET, the boost supply should not be higher than 18 volts above the motor supply.

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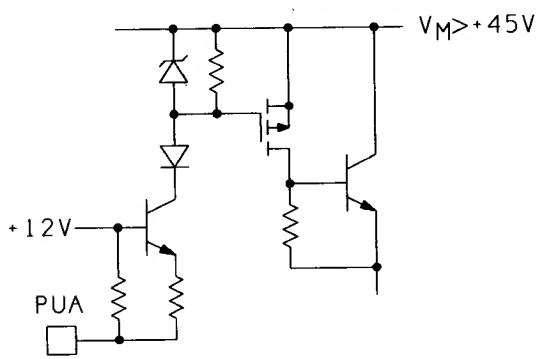
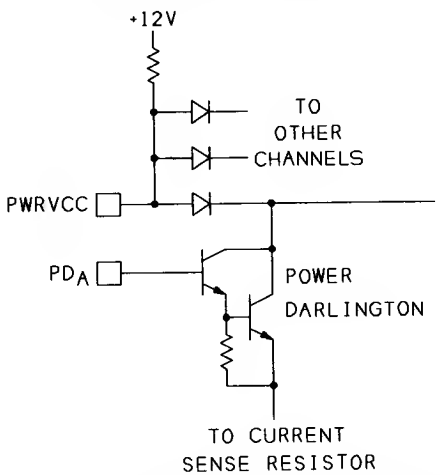
POWER NPN HIGH-SIDE DRIVER



For under 200V 2-quadrent applications, a power NPN driven by a small P-Channel MOSFET will perform well as a high-side driver. A high voltage small-signal NPN is used as a level shift and a high voltage low-current MOSFET provides drive. Although the NPN will not saturate if used within its limitations, the base-emitter resistor on the NPN is still the speed limiting component.

POWER NPN LOW-SIDE DRIVER



This power NPN Darlington drive technique uses a clamp to prevent deep saturation. By limiting saturation of the power device, excessive base drive is minimized and turn-off time is kept fairly short. Lack of base series resistance also adds to the speed of this approach.

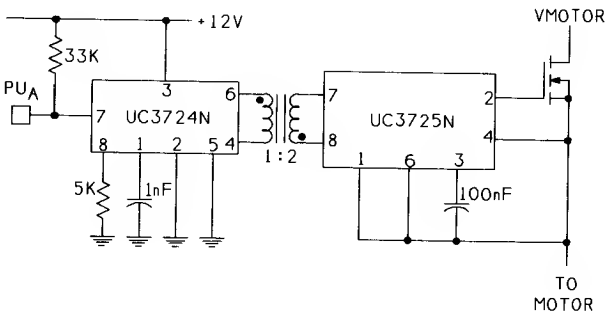
FAST HIGH-SIDE N-CHANNEL DRIVER with TRANSFORMER ISOLATION

A small pulse transformer can provide excellent isolation between the UC3625 and a high-voltage N-Channel MOSFET while also coupling gate drive power. In this circuit, a UC3724 is used as a transformer driver/encoder that duty-cycle modulates the transformer with a 150kHz pulse train. The UC3725 rectifies this pulse train for gate drive power, demodulates the signal, and drives the gate with over 2 amp peak current.

Both the UC3724 and the UC3725 can operate up to 500kHz if the pulse transformer is selected appropriately. To raise the operating frequency, either lower the timing resistor of the UC3724 (1K minimum), lower the timing capacitor of the UC3724 (500pF minimum) or both.

If there is significant capacitance between transformer primary and secondary, together with very high output slew rate, then it may be necessary to add clamp diodes from the transformer primary to +12V and ground. Signal diodes such as 1N4148 are normally adequate.

The UC3725 also has provisions for MOSFET current limiting. Consult the UC3725 data sheet for more information on implementing this.



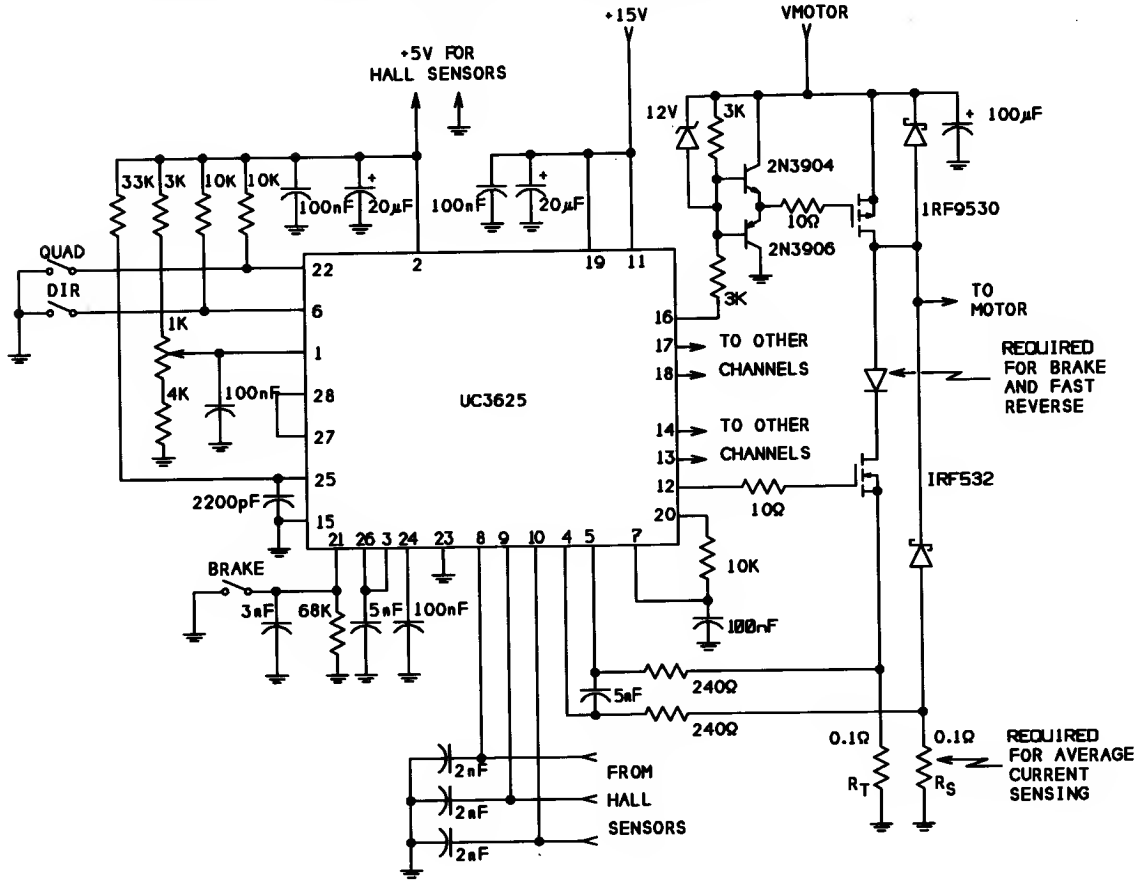
COMMUTATION TRUTH TABLE

This table shows the outputs of the gate drive and open collector outputs for given hall input codes and direction signals. Numbers at the top of the columns are pin numbers.

These ICs operate with position sensor encoding that has either one or two signals high at a time, never all low or all high. This coding is sometimes referred to as "120° Coding" because the coding is the same as coding with position sensors spaced 120 magnetic degrees about the rotor. In response to these position sense signals, only one low-side driver will turn on (go high) and one high-side driver will turn on (pull low) at any time.

INPUTS				OUTPUTS					
DIR	H1	H2	H3	LOW-SIDE			HIGH-SIDE		
6	8	9	10	12	13	14	16	17	18
1	0	0	1	L	H	L	L	H	H
1	0	1	1	L	L	H	L	H	H
1	0	1	0	L	L	H	H	L	H
1	1	1	0	H	L	L	H	L	H
1	1	0	0	H	L	L	H	H	L
1	1	0	1	L	H	L	H	H	L
0	1	0	1	L	L	H	H	L	H
0	1	0	0	L	L	H	L	H	H
0	1	1	0	L	H	L	L	H	H
0	0	1	0	L	H	L	H	H	L
0	0	1	1	H	L	L	H	H	L
0	0	0	1	H	L	L	H	L	H
X	1	1	1	L	L	L	H	H	H
X	0	0	0	L	L	L	H	H	H

TYPICAL APPLICATION: A 45V/8A Brushless DC Motor Drive Circuit



N–Channel power MOSFETs are used for low–side drivers, while P–Channel power MOSFETs are shown for high–side drivers. Resistors are used to level shift the UC3625 open–collector outputs, driving emitter followers into the MOSFET gate. A 12V zener clamp insures that the MOSFET gate–source voltage will never exceed 12V. Series 10Ω gate resistors tame gate reactance, preventing oscillations and minimizing ringing.

The oscillator timing capacitor should be placed close to pins 15 and 25, to keep ground current out of the capacitor. Ground current in the timing capacitor causes oscillator distortion and slaving to the commutation signal.

The potentiometer connected to pin 1 controls PWM duty cycle directly, implementing a crude form of speed control. This control is often referred to as "voltage mode" because the potentiometer position sets the average motor voltage. This controls speed because steady–state motor speed is closely related to applied voltage.

Pin 20 (TACH OUT) is connected to pin 7 (SPEED IN) through an RC filter, preventing direction reversal while the motor is spinning quickly. In two–quadrant operation, this reversal can cause kinetic energy from the motor to be forced into the power MOSFETs.

A diode in series with the low-side MOSFETs facilitates PWM current control during braking by insuring that braking current will not flow backwards through low–side MOSFETs. Dual current–sense resistors give continuous current sense, whether braking or running in four–quadrant operation, an unnecessary luxury for two–quadrant operation.

The 68k ohm and 3nF tachometer components set maximum commutation time at 140µs. This permits smooth operation up to 35,000 RPM for four–pole motors, yet gives 140µs of noise blanking after commutation.

Unitrode Integrated Circuits Corporation
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INTEGRATED CIRCUITS

UNITRODE

Phase Locked Frequency Controller

UC1633
UC2633
UC3633

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

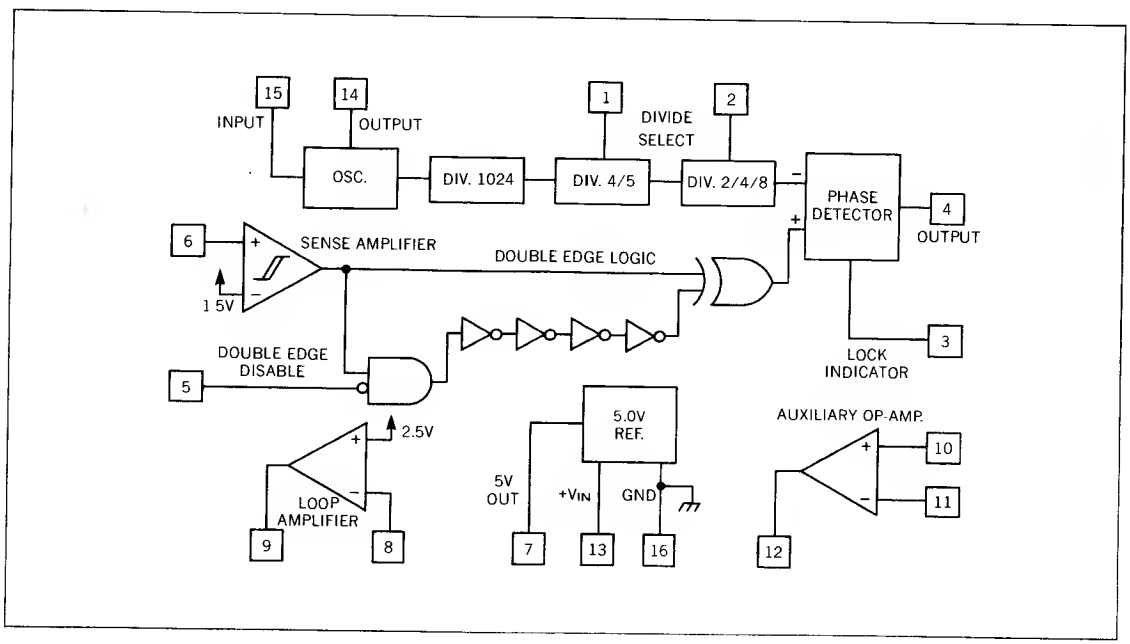
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM



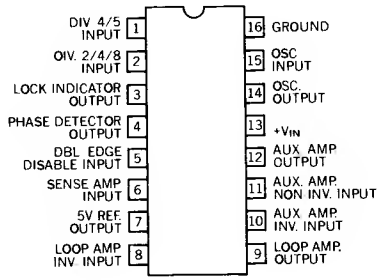
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) ..... +20V
Reference Dutput Current ..... −30mA
Op-Amp Dutput Currents ..... ±30mA
Dp-Amp Input Voltages ..... −.3V to +20V
Phase Detector Dutput Current ..... ±10mA
Lock Indicator Dutput Current ..... +15mA
Lock Indicator Dutput Voltage ..... +20V
Divide Select Input Voltages ..... −.3V to +10V
Double Edge Disable Input Voltage ..... −.3V to +10V
Dscillator Input Voltage ..... −.3V to +5V
Sense Amplifier Input Voltage ..... −.3V to +20V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Dperating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3633, −25°C to +85°C for the UC2633 and −55°C to +125°C for the UC1633, $+V_{IN}$ = 12V.) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$ = 15V		20	28	mA
Reference					
Dutput Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8 to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Dutput	12	16	20	dB
Input DC Level (V_{IB})	Dscillator Input Pin Dpen, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	V_{IN} = V_{IB} ± 0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Dutput DC Level	Oscillator Input Pin Dpen, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{PP}$ at Dscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	−5.0	0.0	5.0	μA
Div. 4/5 Threshold		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	−500	−150		μA
Div. 2/4/8 Dpen Circuit Voltage	Input Current = 0μA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.

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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3633, −25°C to +85°C for the UC2633 and −55°C to +125°C for the UC1633, $+V_{IN}$ = 12V.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	−1.0	−0.2		μA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	μA
	Input = 0V (Enabled)	−5.0	0.0	5.0	μA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 2)	I_{OUT} = −200 to +200μA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	μA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	−0.8	−0.2		μA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	−0.8	−0.2		μA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	μA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.

APPLICATION AND OPERATION INFORMATION

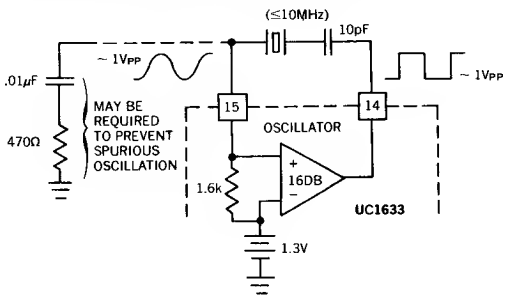
Determining The Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

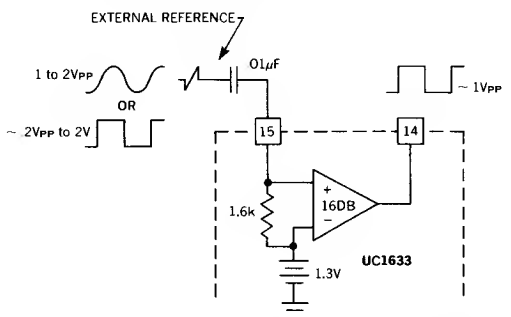
$f_{OSC}(Hz)$ = (Divide Ratio) · (Motor RPM) · (1/60 SEC/MIN) · (No. of Rotor Poles/2) · (× 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

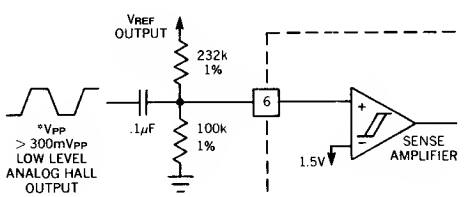
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method For Deriving Rotation Feedback Signal From Analog Hall Effect Device



*This signal may require filtering if chopped mode drive scheme is used.

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APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

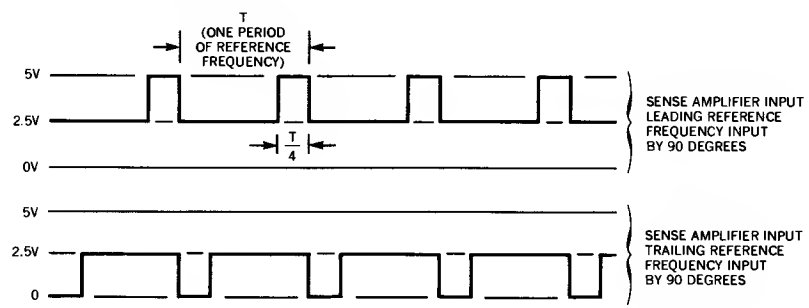
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, typically 6.0kΩ. When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the −input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector, $K\phi$, is $5V/4\pi$ radians, or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

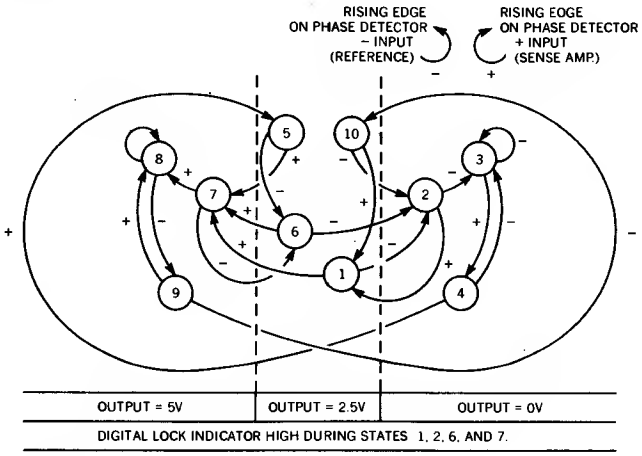
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the −input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

TYPICAL PHASE DETECTOR OUTPUT WAVEFORMS

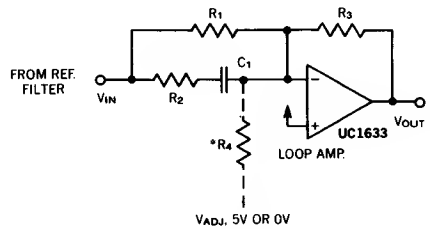


PHASE DETECTOR STATE DIAGRAM



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{\nu_{OUT}}{\nu_{IN}}(s) = \frac{R_3}{R_1} \cdot \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\, C_1}$$

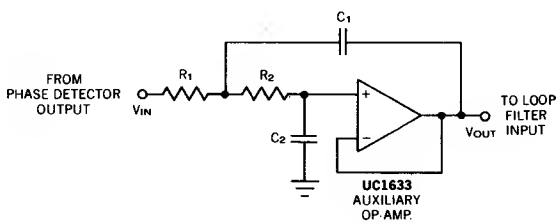
* The static phase error of the loop is easily adjusted by adding resistor, R_4, as shown. To lock at zero phase error R_4 is determined by:

$$R_4 = \frac{2.5V \cdot R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$ R_4 Goes To 0V
$(V_{OUT} - 2.5) < 0$ R_4 Goes To 5.0V

Reference Filter Configuration



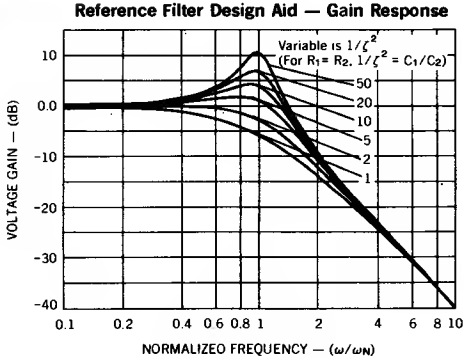
$$\frac{\nu_{OUT}}{\nu_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

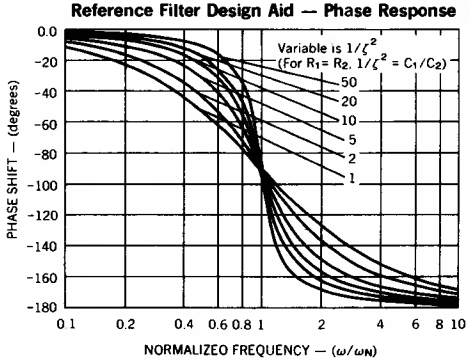
$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\,\frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid — Gain Response



Reference Filter Design Aid — Phase Response



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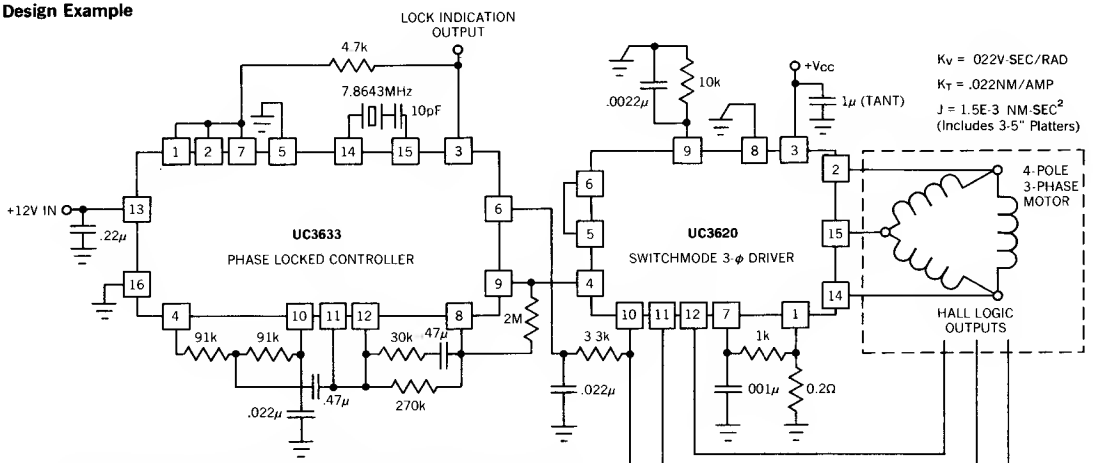
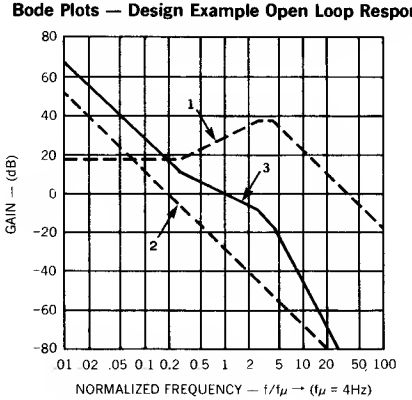
Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots — Design Example Open Loop Response



1 — $K_{LF}(s) \cdot K_{RF}(s)$

2* — $\dfrac{N \cdot K\phi \cdot G_{PO} \cdot K_T}{s^2 \cdot J}$

3 — Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response

$K_{RF}(s)$ = Reference Filter Response

N = 4 (Using Double Edge Sensing With 4 Pole Motor)

$K\phi$ = Phase Detector Gain (.4V/RAD)

G_{PD} = Power Stage Transconductance (1A/V)

K_T = Motor Torque Constant (.022NM/A)

J = Motor Moment of Inertia (.0015NM - SEC^2)

$s = 2\pi jf$

*Note: For a current mode driver the electrical time constant, L_M/R_M, of the motor does not enter into into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2** above, can be approximated by:

$$\frac{N \cdot K\phi \cdot K_{PD} \cdot K_T}{s^2 \cdot J \cdot R_M} \quad \text{if: } R_M \gg K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T^2}{2\pi \cdot J \cdot R_M} < f < \frac{R_M}{2\pi \cdot L_M}$$

Here: K_{PD} = Voltage Gain of Driver Stage

R_M = Motor Winding Resistance

L_M = Motor Winding Inductance

INTEGRATED CIRCUITS

UNITRODE

Phase Locked Frequency Controller

UC1634
UC2634
UC3634

FEATURES

- Precision Phase Locked Frequency Control System
- Commutation Logic for 2-Phase Motors
- Disable Input for Motor Inhibit
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Two High Current Op-Amps
- 5V Reference Output

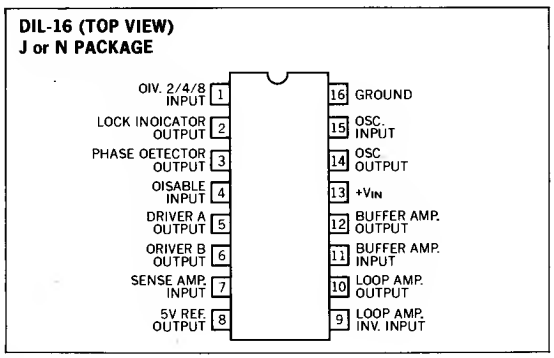
DESCRIPTION

The UC1634 series of devices is optimized to provide precision phase locked frequency control for two phase DC brushless motors. These devices include most of the features of the general purpose UC1633 Phase Locked Control family and also provide the out-of-phase commutation signals required for driving two phase brushless motors. Only an external power booster stage is required for a complete drive and control system.

The two commutation outputs are open collector devices that can sink in excess of 16mA. A disable input allows the user to simultaneously force both of these outputs to an active low state. Double edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at Pin 7.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE

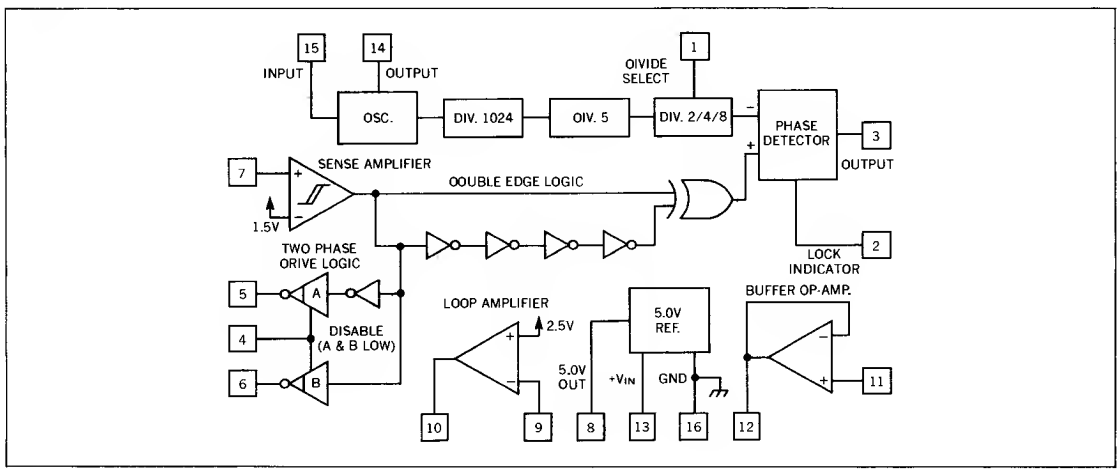


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltage ..... -.3V to +10V
Disable Input Voltage ..... -.3V to +10V
Oscillator Input Voltage ..... -.3V to +5V
Sense Amplifier Input Voltage ..... -.3V to +20V
Driver Output Currents ..... +30mA
Driver Output Voltages ..... +20V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient ..... 100°C/W
Thermal Resistance Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3634, −25°C to +85°C for the UC2634 and −55°C to +125°C for the UC1634, $+V_{IN}$ = 12V.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$ = 15V		20	29	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8 to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator In to Oscillator Out	12	16	20	dB
Input DC Level (V_{IB})	Oscillator In Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	$V_{IN} = V_{IB} \pm 0.5V$, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator In Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{PP}$ at Oscillator In	10			MHz
Div. 4/5 Input Current (Q Package Only, Note 3)	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	−5.0	0.0	5.0	μA
Div. 4/5 Threshold (Q Package Only, Note 3)		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	−500	−150		μA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0μA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	−1.0	−0.2		μA
Two Phase Drive Outputs, A and B					
Saturation Voltage	I_{OUT} = 16mA		0.3	0.6	V
Leakage Current	V_{OUT} = 15V		0.1	5.0	μA
Disable Input					
Input Current	Input = 5V (Disabled, A and B Outputs Active Low)		150	500	μA
	Input = 0V (Enabled)	−5.0	0.0	5.0	μA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 2)	I_{OUT} = −200 to +200μA, T_J = 25°C	4.5	6.0	7.5	kΩ

Note: 2. These impedance levels will vary with T_J at about 1700ppm/°C.
3. This part is also available in a 20 pin plastic leadless chip carrier, Q designator, where a divide by 4/5 select pin is available. Consult factory for details.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3634, −25°C to +85°C for the UC2634 and −55°C to +125°C for the UC1634, $+V_{IN}$ = 12V.) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	μA
Loop Amplifier					
N INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	−0.8	−0.2		μA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Buffer Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	−0.8	−0.2		μA
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

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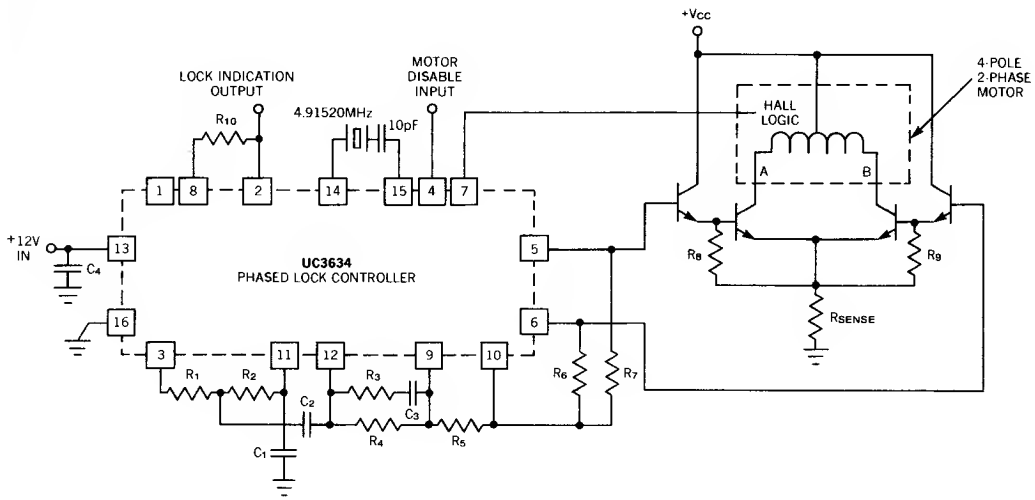
APPLICATION AND OPERATION INFORMATION (For additional information see UC1633 data sheet)

Design Example:

Precision phased locked frequency control of a 2-phase motor at 3600 RPM. Using the commutation logic on the UC3634, a simple discrete drive scheme is possible.



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Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Seperate Divider Outputs and Phase Detector Input Pins
- Double Edge Optioni on the Frequency Feedback Sensing Amplifier
- Two High Current Op Amps
- 5V Reference Output

DESCRIPTION

The UC1635 family of integrated circuits was designed for use in precision speed control of DC motors. An extension to the UC1633 line of phase locked controllers, these devices provide access to the both of the digital phase detector's inputs, and include a reference frequency divider output pin. With this added flexibility, this family of controllers can be used to obtain phase synchronization of multiple motors.

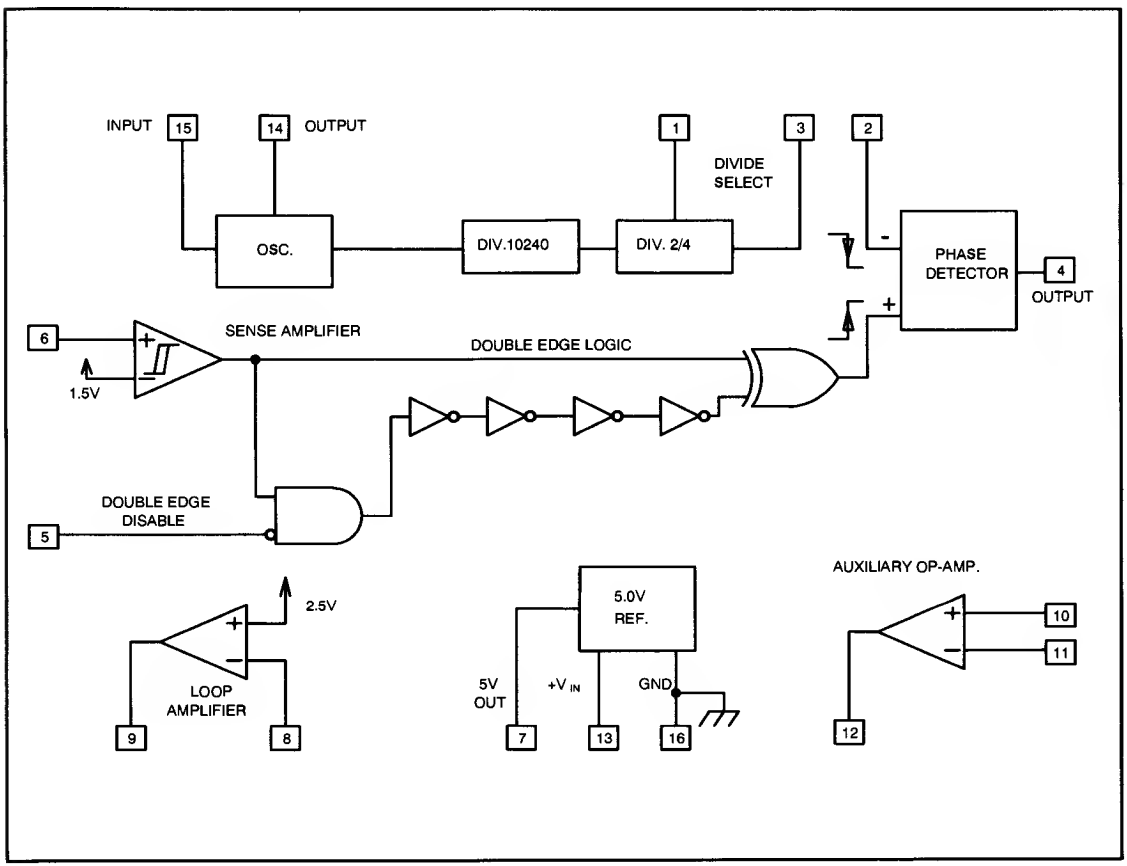
A reference frequency can be generated using the device's crystal oscillator and programmable dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector responds proportionally to the phase error between the detector's minus input pin and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A 5V reference output can be used to accurately set DC operating levels.

BLOCK DIAGRAM



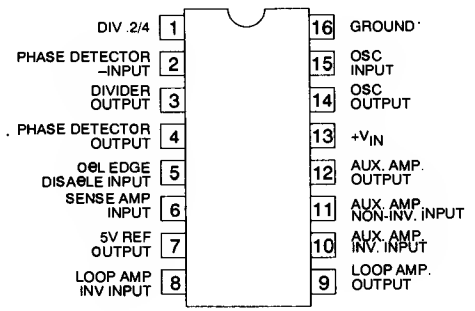
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) . . . . . +20V
Reference Output Current . . . . . -30mA
Op-Amp Output Currents . . . . . ±30mA
Op-Amp Input Voltages . . . . . -.3V to +20V
Phase Detector Input Voltage . . . . . -.3V to +5V
Phase Detector Output Current . . . . . ±10mA
Lock Indicator Output Current . . . . . +15mA
Lock Indicator Output Voltage . . . . . +20V
Divide Select Input Voltages . . . . . -.3V to +10V
Double Edge Disable Input Voltage . . . . . -.3V to +10V
Oscillator Input Voltage . . . . . -.3V to +5V
Sense Amplifier Input Voltage . . . . . -.3V to +20V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/C above 25°C
Power Dissipation at T_C = 25°C 2000mW
Derate at 16mW/°C above 25°C
Thermal Resistance Junction to Ambient . . . . . 100°C/W
Thermal Resistance Junction to Case . . . . . .60°C/W
Operating Junction Temperature . . . . . -55° to + 150°C
Storage Temperature . . . . . -65° to + 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



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ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, specifications hold for T_A =0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, $+V_{IN}$=12V.) $T_A=T_j$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$=15V		20	28	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	1_{OUT} = 0 to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8 to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	15	35		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (V_{IB})	Oscillator Input Pin Open, TJ = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	$V_{IN} = V_{IB} \pm 0.5V$, T_J - 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Piin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{pp}$ at Oscillator Input	10			MHz
Div. 2/4 Input Current	Input = 5V (Div. by 2)		150	500	µA
	Input = 0V (Div. by 4)	–5.0	0.0	5.0	µA
Div. 2/4 Threshold		0.5	1.6	2.2	V
Divider Output	High Level (w/6.8K Load to GND)	4.0	4.5		V
	Low Level (Open Collector Leakage)			10	µA

NOTE 2: These impedance levels will vary with T_J at about 1700ppm/°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, specifications hold for T_A=0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, $+V_{IN}$=12V.) $T_A=T_J$

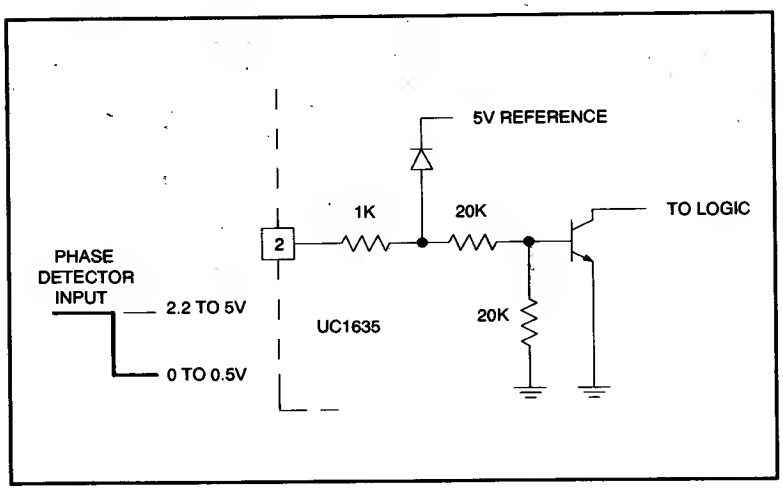
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input =1.5V	–1.0	–0.2		µA
Double Edge Disable Input					
Input Current	Input =5V (Disabled)		150	500	µA
	Input =0V (Enabled)	–5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
-Input Threshold	Detector Responds to Falling Edge	0.5	1.6	2.2	V
-Input Current	Input=2.2V		100	250	µA
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT}=4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT}=0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 2)	I_{OUT}=–200 to+200µA, T_J=25°C	4.5	6.0	7.5	kΩ
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input=2.5V	–0.8	–0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$=8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT}=0V	16	35		mA
	Sink, V_{OUT}=5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM}=2.5V			8	mV
Input Bias Current	V_{CM}=2.5V	–0.8	–0.2		µA
Input Offset Current	V_{CM}=2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$=8 to 15V	70	100		dB
CMRR	V_{CM}=0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT}=0V	16	35		mA
	Sink, V_{OUT}=5V	16	30		mA

NOTE 2: These impedance levels will vary with T_J at about 1700ppm/°C.

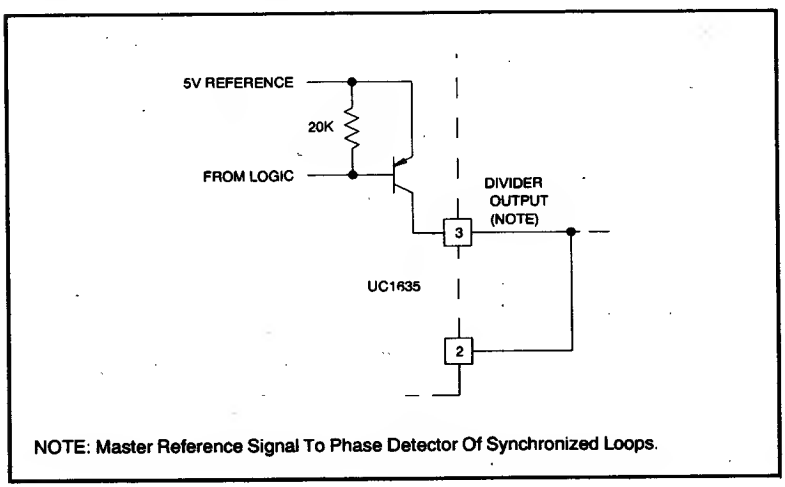
Application and Operation Information

(For Additional Application Information see the UC1633 Data Sheet)

Phase Detector Input Detail



Reference Divider Output Detail



NOTE: Master Reference Signal To Phase Detector Of Synchronized Loops.

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INTEGRATED CIRCUITS

UNITRODE

Switched Mode Controller for DC Motor Drive

UC1637
UC2637
UC3637

FEATURES

- Single or dual supply operation
- ± 2.5V to ± 20V input supply range
- ± 5% initial oscillator accuracy; ± 10% over temperature
- Pulse-by-pulse current limiting
- Under-voltage lockout
- Shutdown input with temperature compensated 2.5V threshold
- Uncommitted PWM comparators for design flexibility
- Dual 100mA, source/sink output drivers

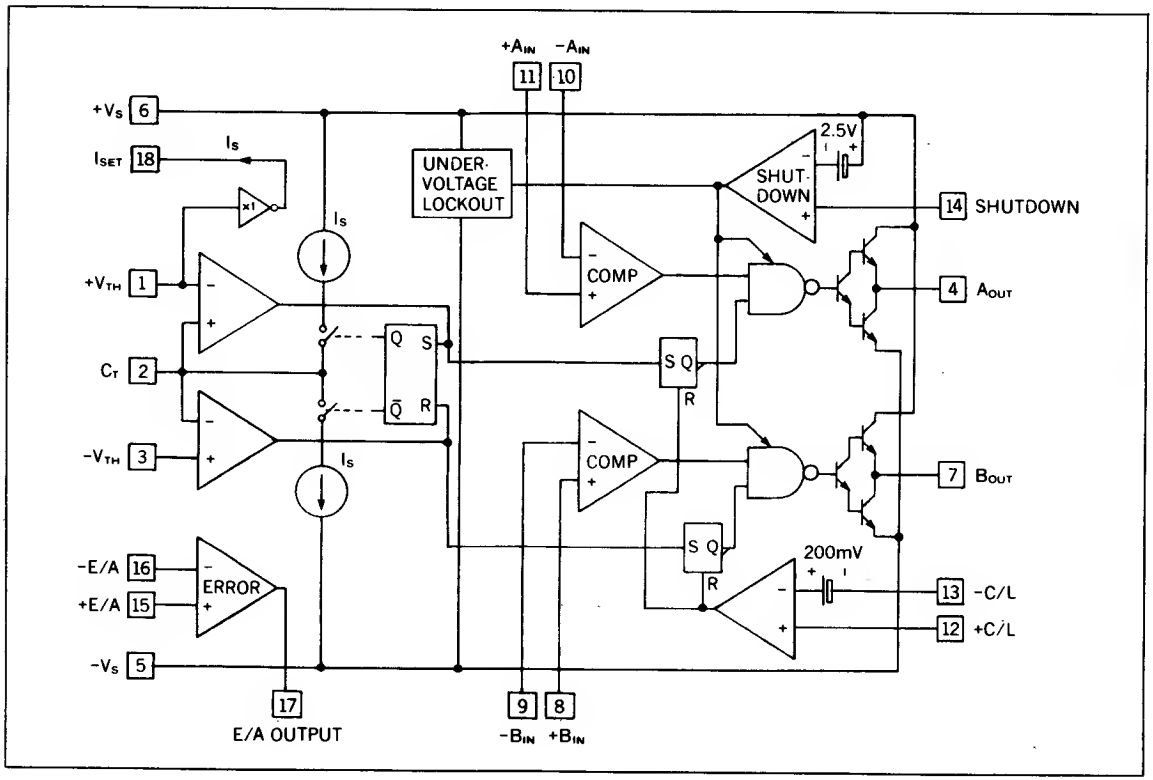
DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ± 100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

The UC1637 is characterized for operation over the full military temperature range of −55°C to +125°C, while the UC2637 and UC3637 are characterized for −25°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



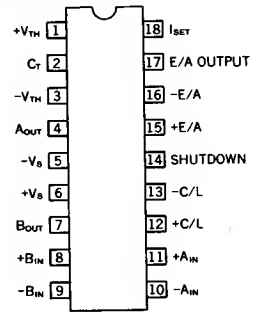
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($\pm V_S$) ..... ±20V
Output Current, Source/Sink (Pins 4, 7) 500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15, 16) ..... $\pm V_S$
Error Amplifier Output Current (Pin 17) ..... ±20mA
Oscillator Charging Current (Pin 18) ..... -2mA
Power Dissipation at T_A = 25°C 1000mW
  Derate at 10mW/°C For T_A above 50°C
Power Dissipation at T_C = 25°C 2000mW
  Derate at 16mW/°C for T_C above 25°C
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note: 1. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; $+V_S$ = +15V, $-V_S$ = -15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator								
Initial Accuracy	T_j = 25°C	9.4	10	10.6	9	10	11	kHz
Voltage Stability	V_S = ± 5V to ± 20V, $V_{PIN\ 1}$ = 3V $V_{PIN\ 3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range		0.5	2		0.5	2	%
$+V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
$-V_{TH}$ Input Bias Current	$V_{PIN\ 2}$ = 0V	-10	-0.5		-10	-0.5		µA
$+V_{TH}$, $-V_{TH}$ Input Range		$+V_S$-2		$-V_S$+2	$+V_S$-2		$-V_S$+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	V_S = ± 2.5 to 20V	$-V_S$+2		$+V_S$	$-V_S$+2		$+V_S$	V
Open Loop Voltage Gain	R_L = 10K	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		mHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	V_S = ± 2.5V to ± 20V	75	110		75	110		dB
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode Range	V_S = ± 5 to ± 40V	$-V_S$+1		$+V_S$-2	$-V_S$+1		$+V_S$-2	V

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ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for UC1637; $-25°C$ to $+85°C$ for the UC2637; and $0°C$ to $+70°C$ for the UC3637; $+V_S = +15V$, $-V_S = -15V$, $+V_{TH} = 5V$, $-V_{TH} = -5V$, $R_T = 16.7k\Omega$, $C_T = 1500pF$) $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_j = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	V_S = ± 2.5V to ± 20V	$-V_S$		$+V_S-3$	$-V_S$		$+V_S-3$	V
Shutdown								
Shutdown Threshold	(Note 3)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = $+V_S$ to $-V_S$	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 4)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		-14.9	-13		-14.9	-13	V
	I_{SINK} = 100mA		-14.5	-13		-14.5	-13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 2) C_L = 1nf, T_j = 25°C		100	600		100	600	ns
Fall Time	(Note 2) C_L = 1nf, T_j = 25°C		100	300		100	300	ns

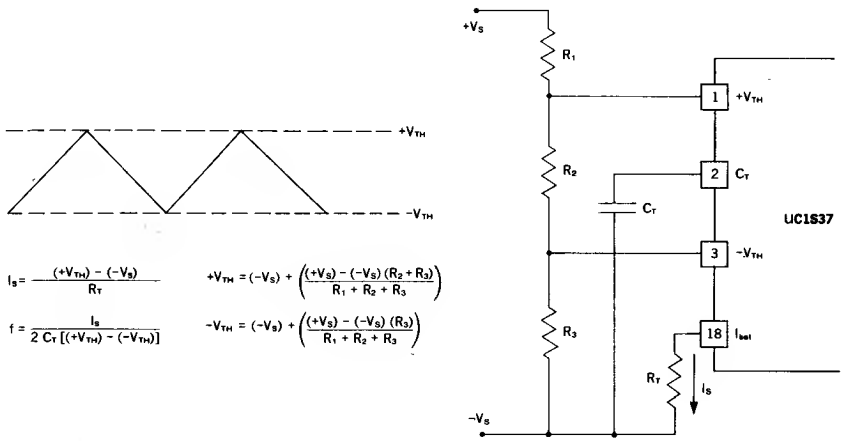
Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. Parameter measured with respect to $+V_S$ (Pin 6).
4. Parameter measured at $+V_S$ (Pin 6) with respect to $-V_S$ (Pin 5).

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{set}, and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{set} terminal to develop the capacitor charging current through R_T. If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.



$$I_S = \frac{(+V_{TH}) - (-V_S)}{R_T}$$

$$f = \frac{I_S}{2\,C_T\,[(+V_{TH}) - (-V_{TH})]}$$

$$+V_{TH} = (-V_S) + \left(\frac{(+V_S) - (-V_S)\,(R_2 + R_3)}{R_1 + R_2 + R_3}\right)$$

$$-V_{TH} = (-V_S) + \left(\frac{(+V_S) - (-V_S)\,(R_3)}{R_1 + R_2 + R_3}\right)$$

Figure 1. Oscillator Set Up

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexability. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high-state of output A and shorten the high-state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

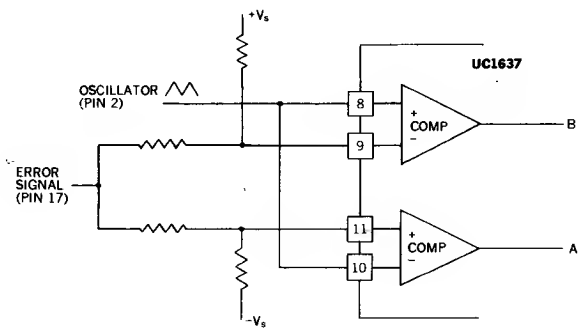


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)

In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)

A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)

With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

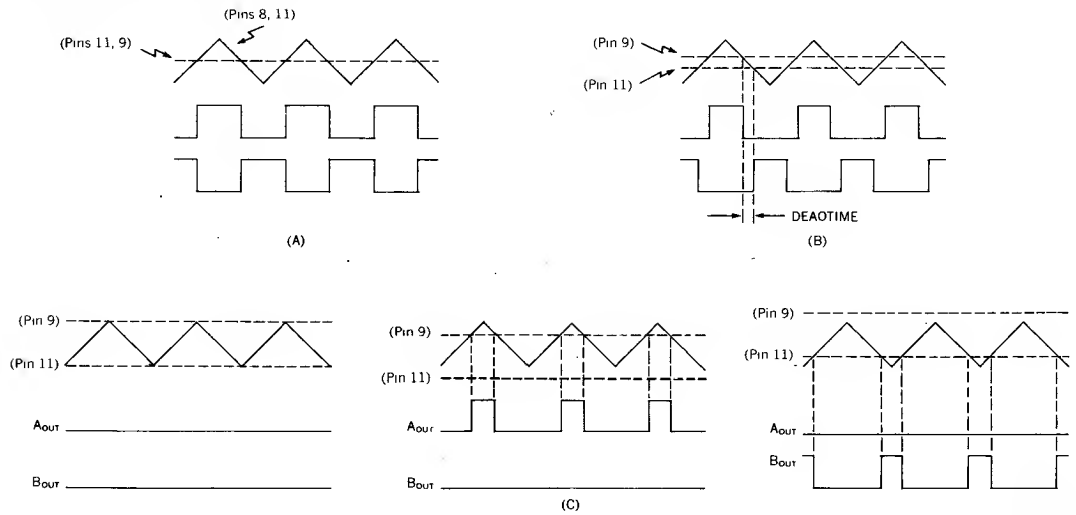


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations.

Output Drivers
Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_S$ +0.2V @ 50mA low level and $+V_S$ — 2.0V @ 50mA high level.

Error Amplifier
The error amplifier consists of a high slew rate (15V/μs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the $\pm V_S$ supply voltage, the common-mode input range and the voltage output swing is within 2V of the V_S supply.

Under-Voltage Lockout
An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

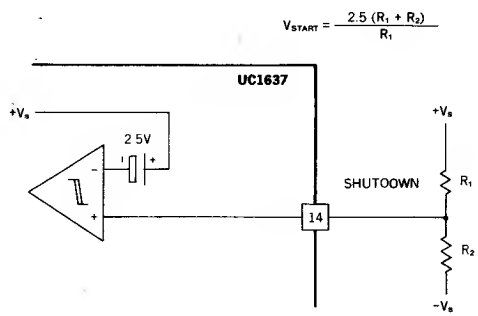


Figure 4. External Under-Voltage Lockout

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below V_{IN}, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

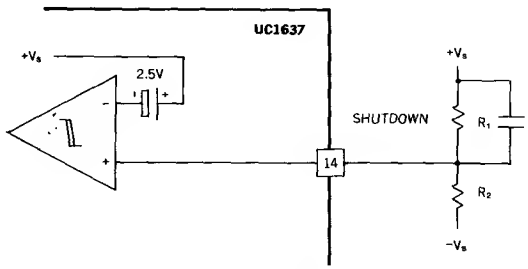


Figure 5. Delayed Start-Up

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from $-V_S$ to within 3V of the $+V_S$ supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

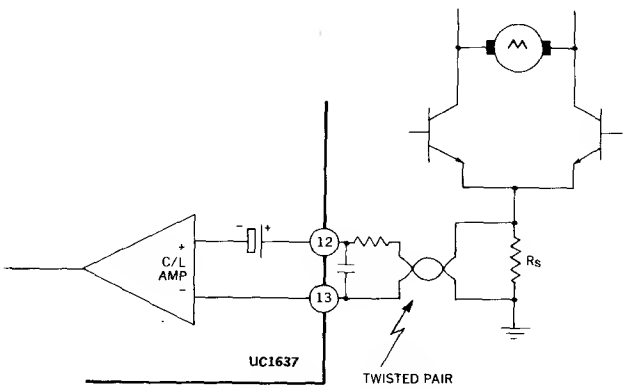


Figure 6. Current Limit Sensing

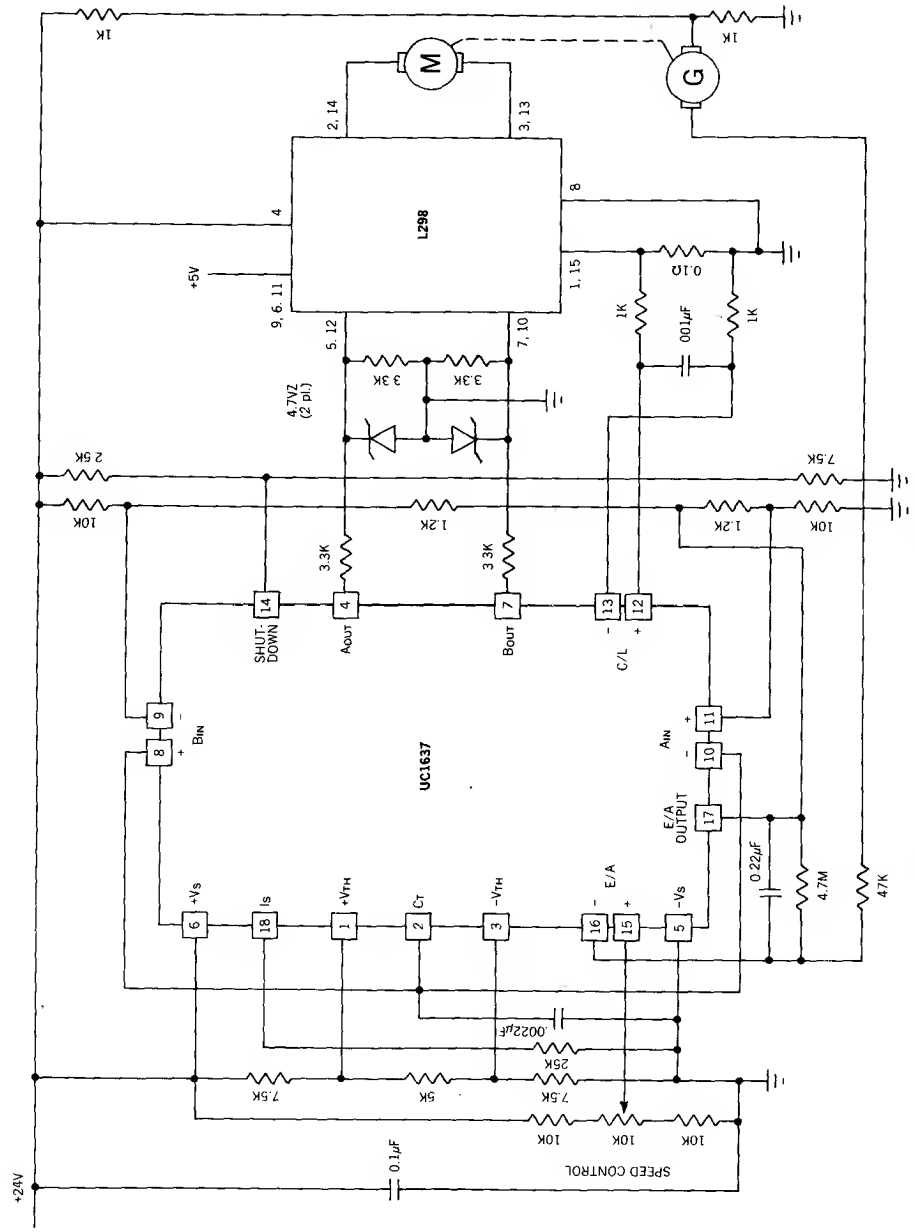


Figure 7. Bi-Directional Motor Drive with Speed Control and Power-Amplifier

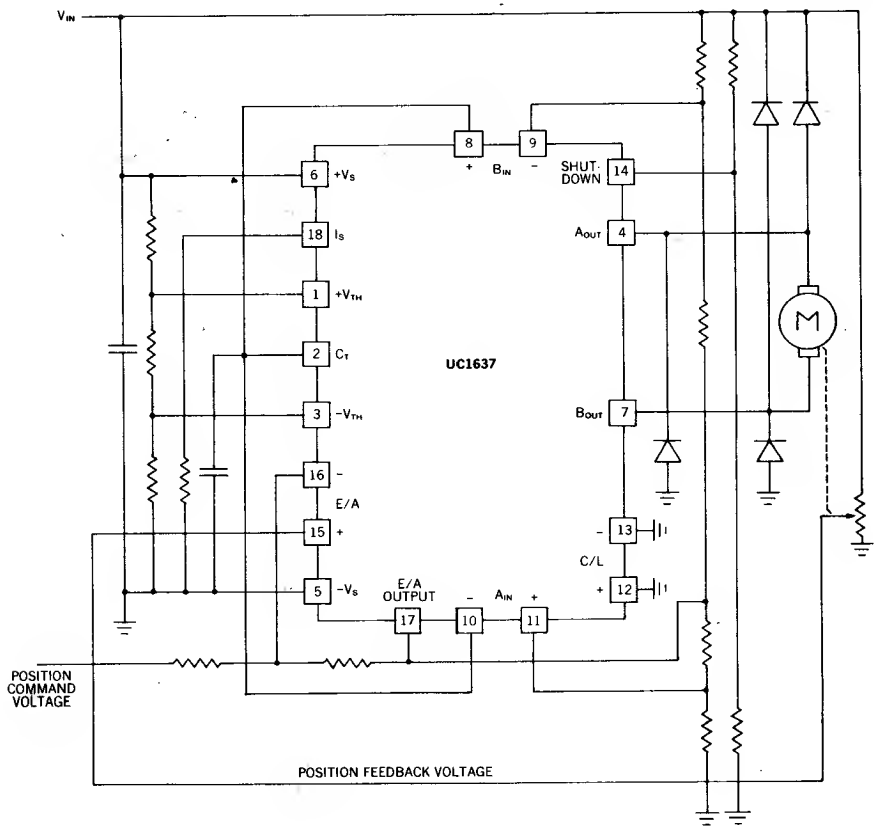


Figure 8. Single Supply Position Servo Motor Drive

5

INTEGRATED CIRCUITS

UNITRODE

Stepper Motor Drive Circuit

UC1717
UC3717

FEATURES

- Half-step and full-step capability
- Bipolar constant current motor drive
- Built-in fast recovery Schottky commutating diodes
- Wide range of current control 5-1000mA
- Wide voltage range 10-45V
- Designed for unregulated motor supply voltage
- Current levels can be selected in steps or varied continuously
- Thermal overload protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717 JP is characterized for operation over the full military temperature range of −55°C to +125°C, while the UC3717 is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{cc} 7V
- Output Supply, V_m 45V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) ..... V_{cc}
- Reference Input (Pin 11) 15V

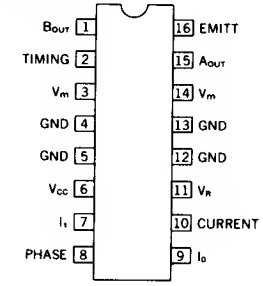
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1,15) ..... ±1A
Junction Temperature, T_j ..... +150°C
Thermal Resistance, Junction to Ambient (N Package) ..... 45°C/W
Thermal Resistance, Junction to Case (N Package) ..... 11°C/W
Thermal Resistance, Junction to Ambient (JP Package) ..... 45°C/W
Thermal Resistance, Junction to Case (JP Package) ..... 11°C/W
Storage Temperature Range, T_s ..... -55°C to +150°C

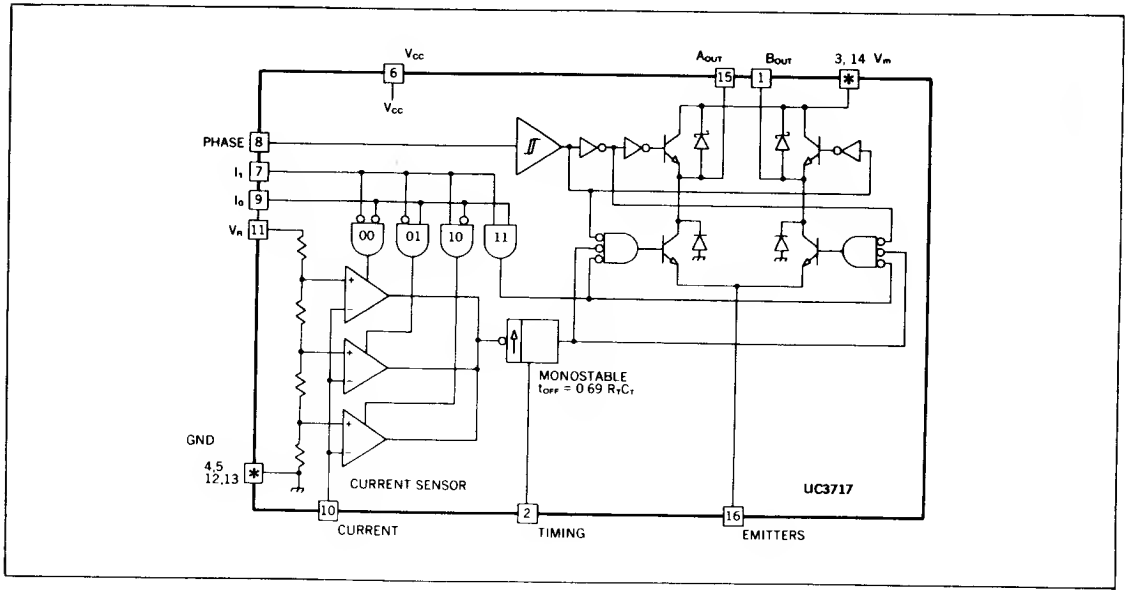
Note: 1. All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
JP, N PACKAGE



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_{cc}	4.75	5	5.25	V
Supply Voltage, V_m	10		40	V
Output Current, I_m	20		800	mA
Rise Time Logic Inputs, t_r			2	μs
Fall Time Logic Inputs, t_f			2	μs
Ambient Temperature, t_a UC1717 UC3717	 -55 0		 125 70	 °C °C

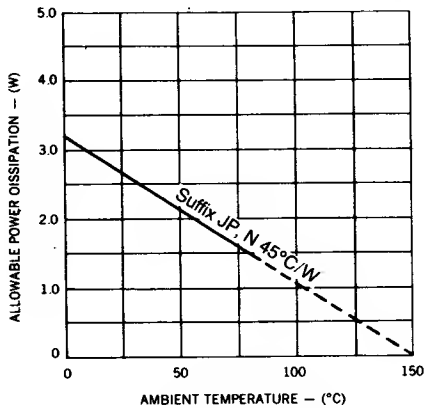


Figure 1.

ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise stated) $T_A=T_J$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, I_{cc}				25	mA
High-Level Input Voltage, Pins 7, 8, 9		2.0			V
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V
High-Level Input Current, Pins 7, 8, 9	V_I = 2.4V			20	μA
Low-Level Input Current, Pins 7, 8, 9	V_I = 0.4V	-0.4			mA
Comparator Threshold Voltage	I_0 = 0, I_1 = 0; V_R = 5.0V	390	420	440	mV
	I_0 = 1, I_1 = 0; V_R = 5.0V	230	250	270	mV
	I_0 = 0, I_1 = 1; V_R = 5.0V	65	80	90	mV
Comparator Input Current		-20		20	μA
Output Leakage Current	I_0 = 1, I_1 = 1, T_A = + 25°C			100	μA
Total Saturation Voltage Drop	I_m = 500mA			4.0	V
Total Power Dissipation	I_m = 500mA, f_s = 30kHz		1.4	2.1	W
	I_m = 800mA, f_s = 30kHz		2.9	3.1	W
Cut Off Time, t_{OFF}	See Figure 5 and 6, V_m = 10V, $t_{ON} \geq 5\mu$s	25	30	35	μs
Turn Off Delay, t_d	See Figure 5 and 6, T_A = +25°C; $dV_C/dt \geq 50mV/\mu s$		1.6	2.0	μs
Thermal Shutdown Junction Temperature		+160		+180	°C

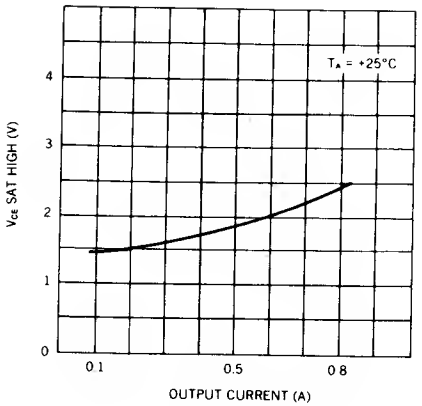


Figure 2. Typical Source Saturation Voltage vs Output Current

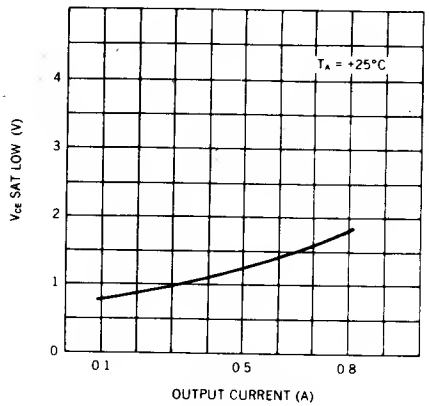


Figure 3. Typical Sink Saturation Voltage vs Output Current

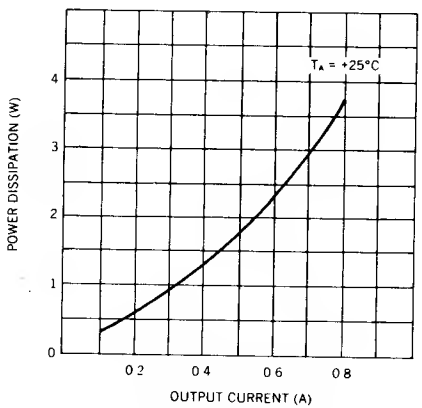


Figure 4. Typical Power Losses vs Output Current

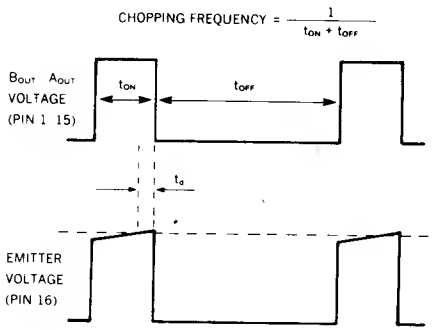


Figure 5. Connections and Component Values as in Figure 6

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions.

(1) Phase Logic and H-Bridge Output Stage
(2) Voltage Divider with three Comparators for current control
(3) Two Logic inputs for Digital current level select
(4) Monostable for off time generation

Input Logic
If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input
The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage
The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used across the source transistors. The Schottky diodes allow the current to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

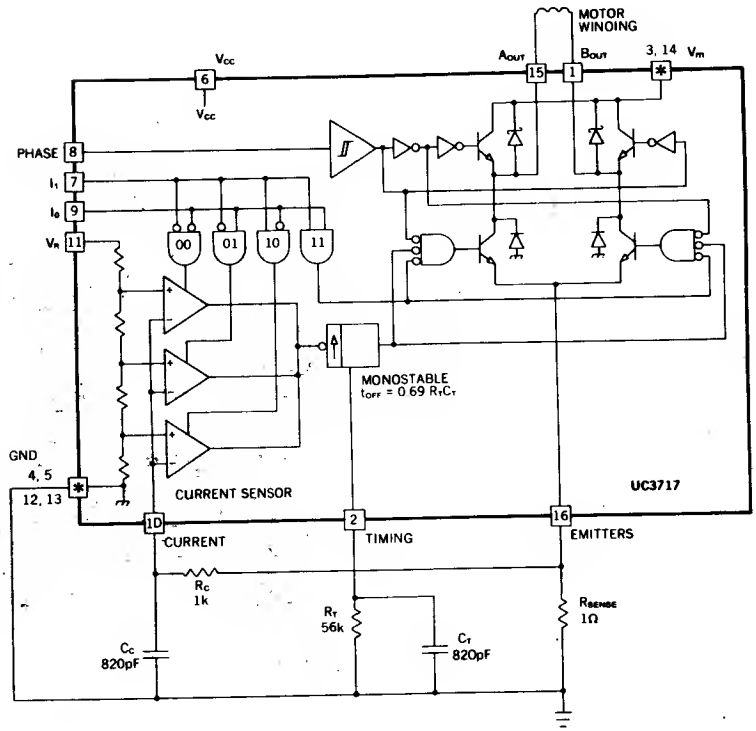


Figure 6.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	CURRENT INHIBIT

Current Control

The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I_0, I_1) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by R_T and C_T connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and micro-stepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor R_s (pin 16).

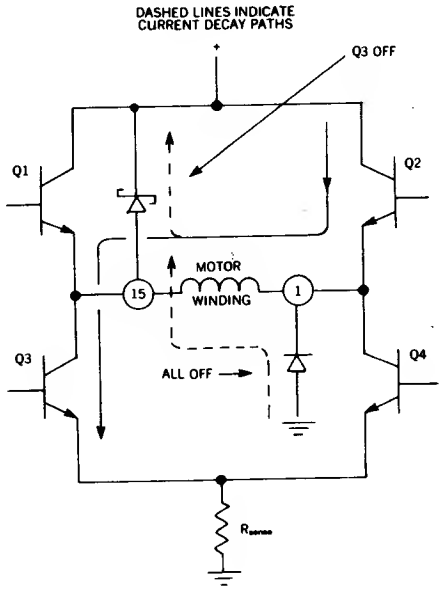


Figure 7. Simplified Schematic of Output Stage

Single-Pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components R_T and C_T as:

$$t_{OFF} = 0.69\ R_T C_T$$

If a new trigger signal should occur during t_{OFF}, it is ignored.

Overload Protection

The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation

When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low-pass filter R_C, C_C to the the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noticed at this time that the slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

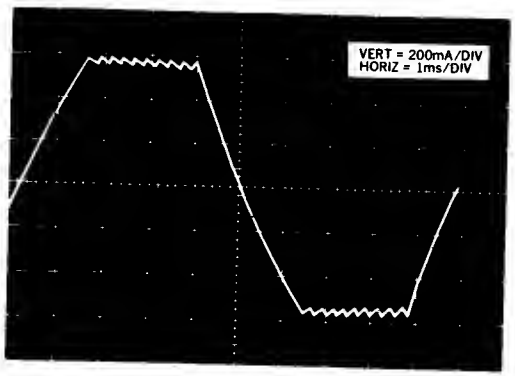


Figure 8.

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

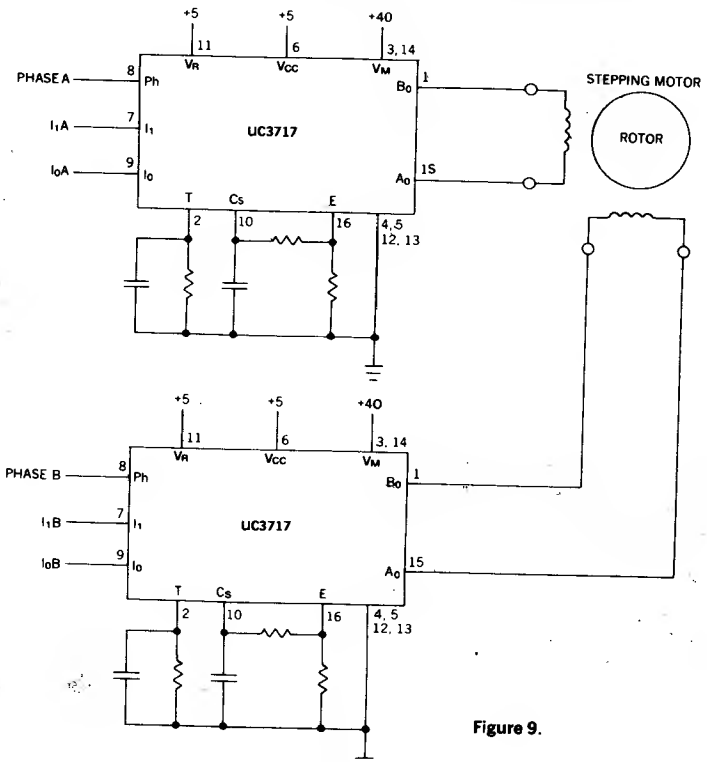


Figure 9.

The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

The UC3717 can also be used to drive an external high power output stage such as the Unitrode PIC900 hybrid circuit in an 18-Pin dual-in-line package. The 5A output of the PIC900 can be controlled with as little as 5mA base drive. Using the UC3717 to drive the PIC900 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

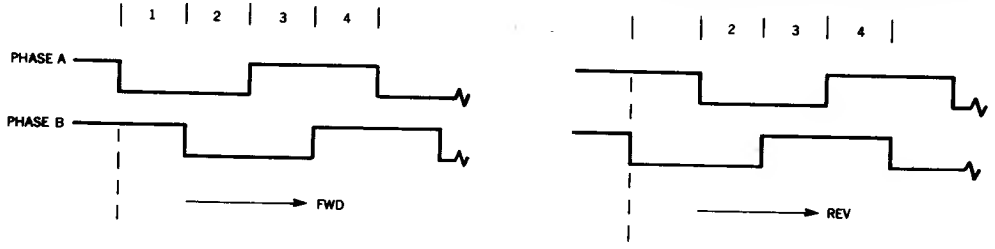


Figure 10. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

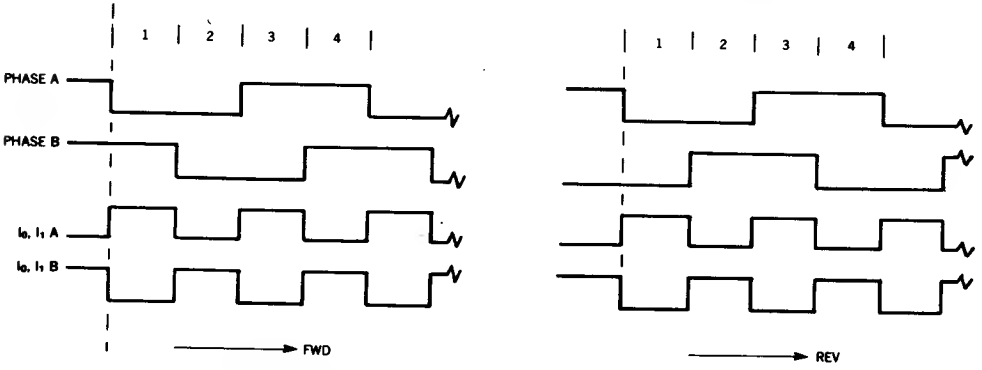


Figure 11. Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

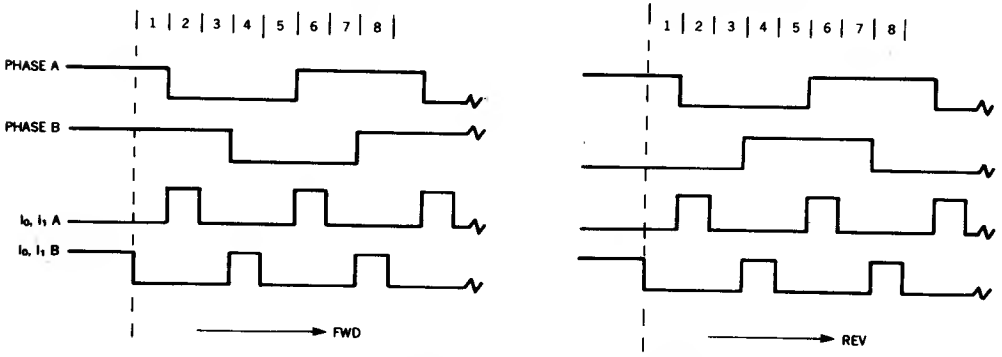


Figure 12. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

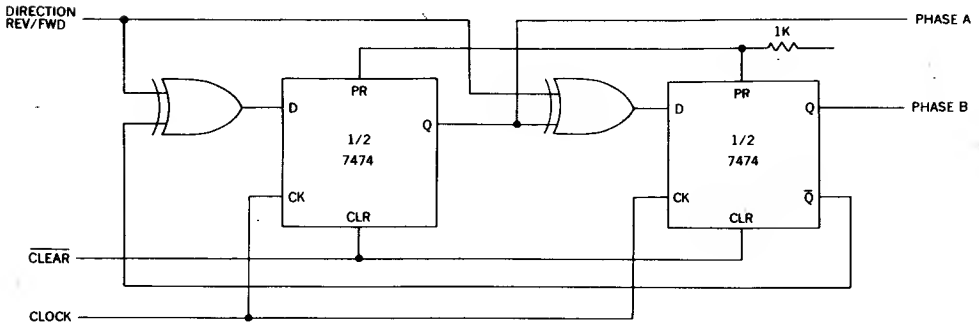


Figure 13. Full Step, Bidirectional Two Phase Drive Logic

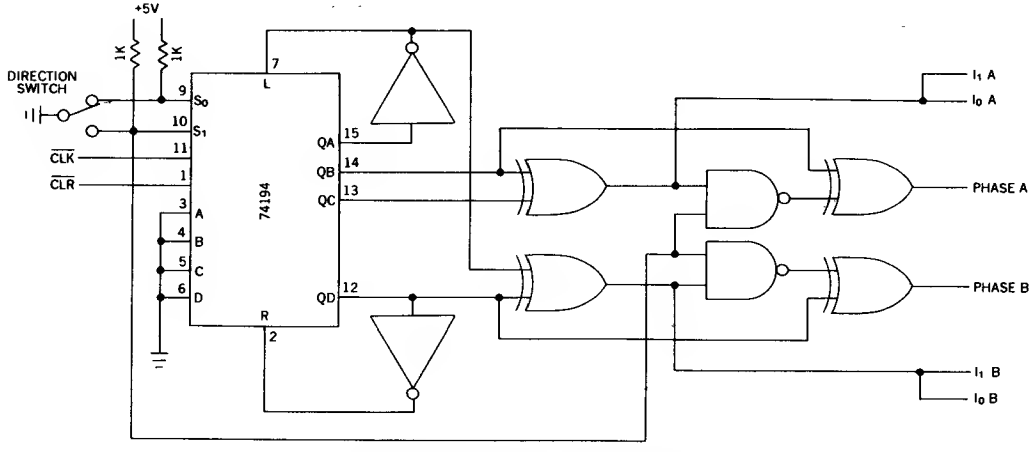


Figure 14. Half Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping

In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

Ramping

Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses

Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponental manner as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference

Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

UNITRODE TYPE NUMBER
UC3717N — 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC1717JP — 16 Pin Dual-in-line Power Ceramic Package

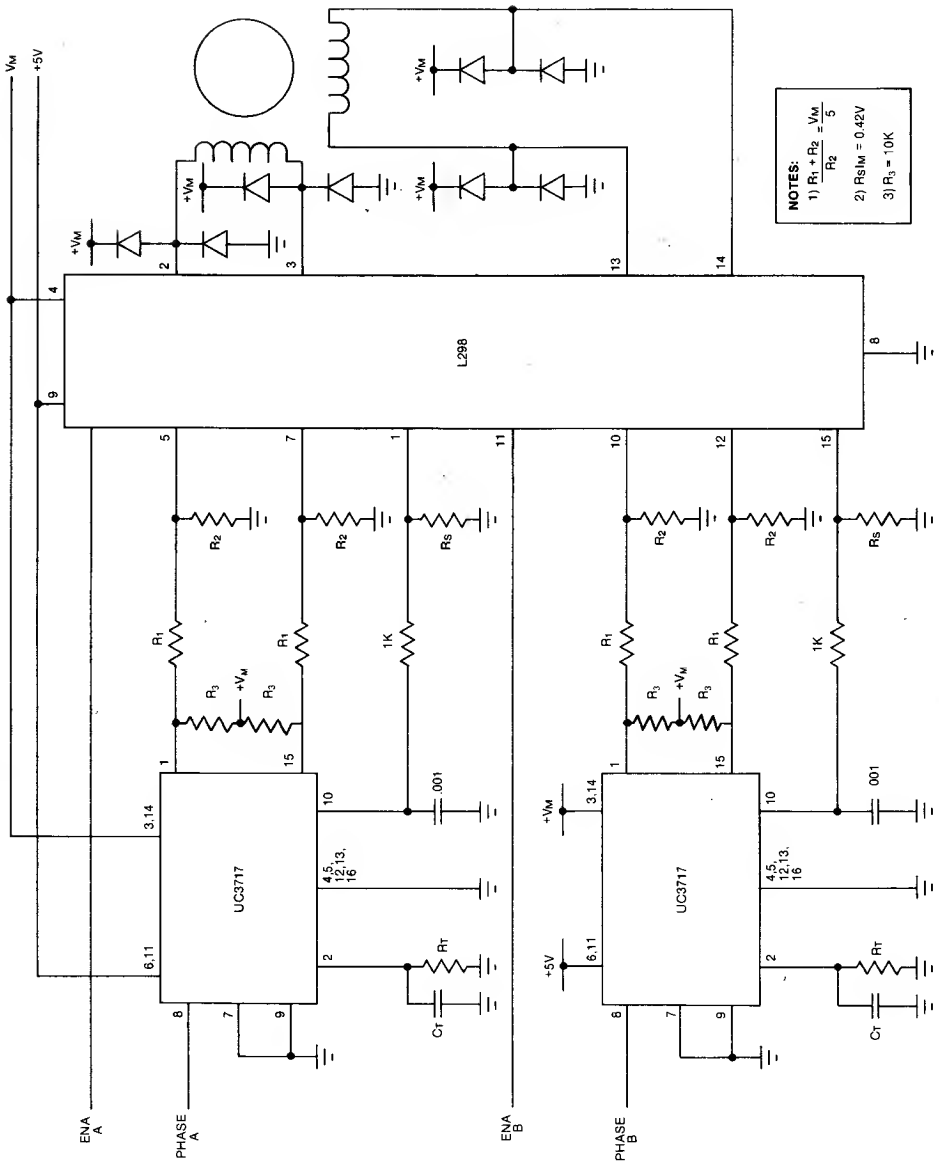


Figure 15 - UC3717 with L298 Power Amplifier.

5

INTEGRATED CIRCUITS

UNITRODE

UC3174
UC3175

Full-Bridge Power Amplifier

PRELIMINARY

FEATURES

- Precision Current Control
- ±800mA Load Current
- 1.25V Total Vsat at 800mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Limit Input to Force Output Extremes
- Inhibit Input and UVLO
- 4V to 15V operation

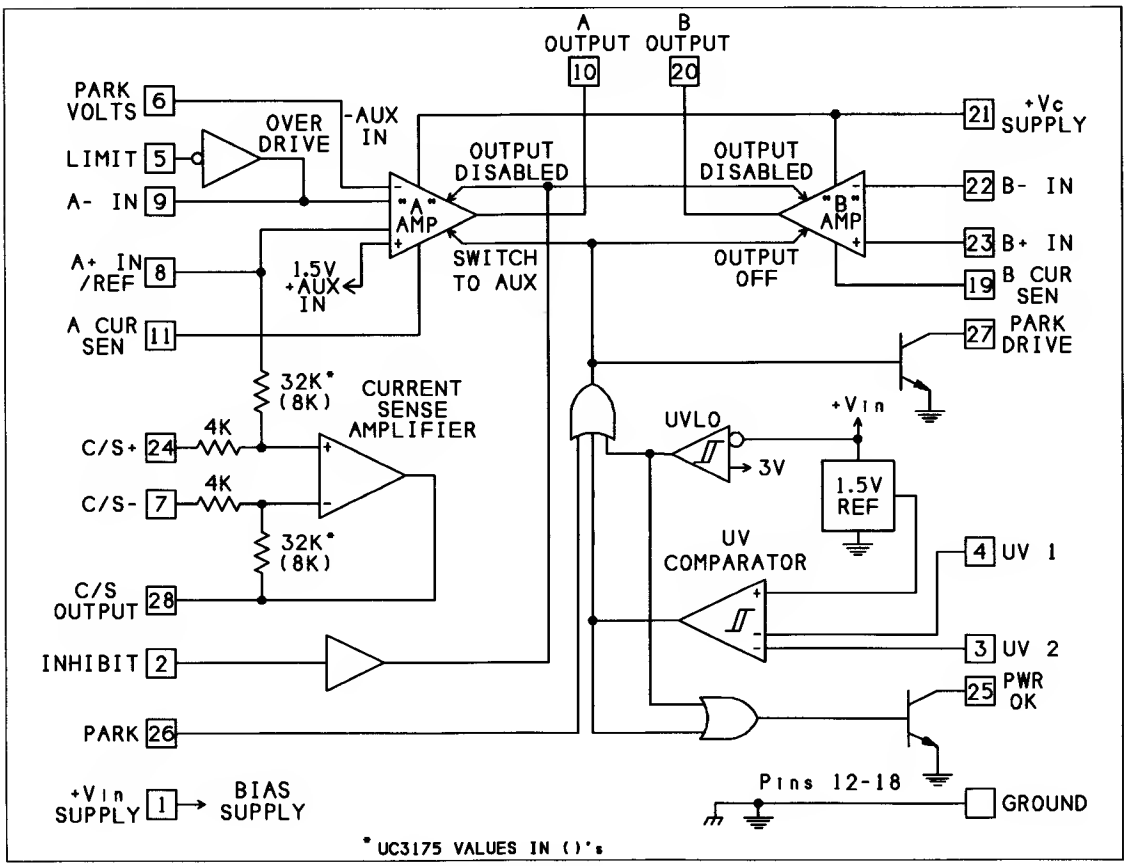
DESCRIPTION

These full-bridge power amplifiers are rated for continuous output current of 0.8 Amperes and are intended for use in demanding servo applications such as head positioning for high-density disk drives. Both of these devices include a precision current sense amplifier that provides accurate control of load current. The UC3174 is designed for ground referenced current sensing using the device's Current Sense pins, while the UC3175 is optimized for sensing current with a single resistor in series with the load. These power amplifiers have a very low output saturation voltage and will operate down to 4V supply levels. Power output stage protection includes current limiting and thermal shutdown.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and force a built-in head park function when either is below minimum. When activated by either the UV comparator, or a command at the separate PARK input, the park circuitry will override the amplifier inputs to convert the power outputs to a programmable constant voltage source which will hold regulation as the supply voltage falls to below 3.0 Volts. Added features include a POWER OK flag output, a LIMIT input to force the drive output to its maximum level in either polarity, and a over-riding INHIBIT input to disable all amplifiers and reduce quiescent supply current.

This device is packaged in a power PLCC surface mount configuration which maintains a standard 28-pin outline, but with 7 pins along one edge allocated to ground for optimum thermal transfer.

BLOCK DIAGRAM



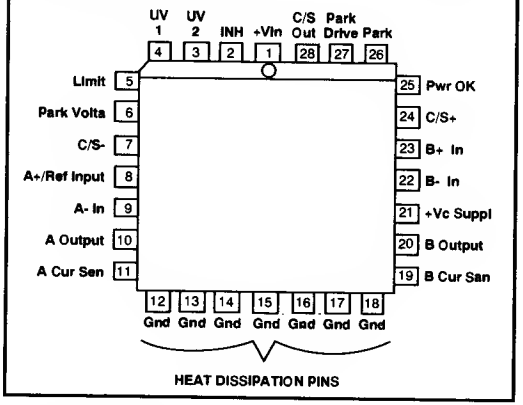
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+Vin,+Vc) 20V
UV Comparator, and Digital Inputs
  maximum forced voltage . . . . . – 0.3V to 10V
  maximum forced current . . . . . ± 10mA
C/S Inputs
  maximum forced voltage . . . . . – 0.3V to 20V
A and B Amplifier Inputs . . . . . – 0.3V to +Vin
Open Collector Output Voltages 20V
A and B Output Currents (continuous)
  source . . . . . Internally Limited
  sink 1.0A
Parking Drive Output Current
  continuous 150mA
  pulsed 1A
Output Diode Current (pulsed) 1A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

NOTE: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.

CONNECTION DIAGRAM

QP Package (Top View)



THERMAL DATA

QP Package:
Thermal Resistance Junction to Leads, θ_{JA} 15°C/W
Thermal Resistance Junction to Ambient, θ_{JA} 40°C/W

(See packaging section of UICC data book for more details on thermal performance)

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications apply for $0^{\circ}C \le T_A \le 70^{\circ}C$, +Vin=12V, +Vc=+Vin, A+/REF INPUT=6V. $T_A=T_J$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
INPUT SUPPLY					
+Vin Supply Current	All amplifier outputs=6V		35	42	mA
+Vc Supply Current	Iout=0A		1		mA
+Vin UVLO Threshold	low to high		2.8	3.0	V
UVLO Threshold Hysteresis			200		mV
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current		–1.5	–0.5		µA
UV Thresholds	low to high, other input=5V	1.48	1.50	1.52	V
UV Threshold Hysteresis		15	25	40	mV
PWR OK Vsat	Iout=5mA			0.45	V
PWR OK Leakage	Vout=20V			5	µA
POWER AMPLIFIERS A and B					
Input Offset Voltage	Vcm=6V, A amplifier			8	mV
	B Amplifier			12	mV
Input Offset Drift	Note 1, A amplifier only			25	µV/°C
Input Bias Current	Vcm=6V, except A+/REF input	–500	–150		nA
Input Offset Current	Vcm=6V, B amplifier only			200	nA
Input Bias Current at A+/Ref Input	(A+/Ref–C/S+)/36K, T_J=25°C, UC3174 Only	23	28	35	µA/V
	(A+/Ref–C/S+)/12K, T_J=25°C, UC3175 Only	69	84	105	µA/V
Differential Sense Error Current	Note 2, IL=5mA	–500		500	µA
	IL=500mA		3	8	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications apply for $0^{o}C \le T_A \le 70^{o}C$, +Vin=12V, +Vc=+Vin, A+/REF INPUT=6V. $T_A=T_j$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER AMPLIFIERS A and B (Cont.)					
CMRR	1V≤Vcm≤10V	70	90		dB
PSRR	+Vin=4V to 15V, Vcm=1.5V	70	90		dB
Large Signal Voltage Gain	Vout=1V, Sinking 500mA to Vout=11V, Sourcing 500mA	3.0	15.0		V/mV
Slew Rate	Note 1		1		V/μs
Unity Gain Bandwidth	Note 1, A amplifier		2		MHz
	Note 1, B amplifier		1		MHz
High-Side Current Limit		0.8	1.0		A
Output Saturation Voltage	High-Side, Isource=250mA		0.7		V
	High-Side, Isource=800mA		0.85		V
	Low-Side, Isink=250mA		0.3		V
	Low-Side, Isink=800mA		0.4		V
	Total, I_{out}=250mA		1.0	1.2	V
	Total, I_{out}=800mA		1.25	1.6	V
High Side Diode Vf	Id=800mA, Inhibit activated		1.0		V
Low Side Diode Vf	Id=800mA, Inhibit activated		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	Vcm=6V			2.0	mV
	Vcm=0V, UC3174 only			5.0	mV
Input Offset Change with Ref Input	2V≤A+/Ref≤10V, UC3174 only			500	μV/V
Input Offset Change with Common Mode Input	0V≤Vcm≤12V, UC3175 only			1500	μV/V
Input Offset Drift	Note 1			8	μV/°C
Voltage Gain	−0.5V≤Vdiff≤+0.5V, Vcm=0V, UC3174 only	7.8	7.9	8.0	V
	−1.0V≤Vdiff≤+1.0V, Vcm=6V, UC3175 only	1.95	2.00	2.05	V
Output Saturation Voltage	Low-Side, I_{sink}=1.5mA		0.3	0.5	V
	High-Side, Isource=1.5mA		0.4	0.7	V
Maximum A+/Ref Input	Volts below +Vin, C/S+ & C/S- = Boutput Max @ 10mA output current, +Vin = 4.5V, UC3175 only, C/S VIO ≤5mV		2.6	3.0	V
PARKING FUNCTION					
Park Input Threshold		0.7	1.1	1.7	V
Park Input Current	Park Input=1.7V		60	100	μA
Park Drive Saturation Voltage, PD_{VSAT}	Isink=50mA		0.3	0.5	V
Parking Drive Leakage	Vout=20V			100	μA
Amplifier A Aux Input Bias Current		−500	−150		nA
Amplifier A Saturation Voltage, A_{HVSAT}	Isource=50mA, +Vin=3V		0.65	0.8	V
Regulating Voltage at Park Volts		1.47	1.50	1.53	V
Minimum Parking Supply Voltage	A_{HVSAT} + PD_{VSAT} ≤1.3V @ 50mA		1.7	1.9	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications apply for $0^{\circ}C \le T_A \le 70^{\circ}C$, +Vin=12V, +Vc=+Vin, A+/REF INPUT=6V. $T_A=T_j$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
AUXILIARY FUNCTIONS					
Limit Input Low Voltage	A Output Forced Low	0.7	0.8		V
Limit Input High Voltage	A Output Forced High		2.2	2.3	V
Limit Inactive		1.2		1.8	V
Limit Open Circuit Voltage		1.45	1.50	1.55	V
Limit Input Resistance	1.2V≤Limit Input≤1.8V		10		KΩ
Inhibit Input Threshold		0.7	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V		400	700	µA
Supply Current when Inhibited	The sum of +Vin and +Vc currents		2	6	mA
Thermal Shutdown Temperature			165		°C

NOTES:

1: This specification not tested in production.

2: This specification is a measure of the accuracy of the differential current sense scheme using the Current Sense pins of the UC3174. The error current specified is defined as $I_{CSA}-I_{CSB}-I_L$, where I_{CSA}, and I_{CSB}, are, respectively, the currents out of the A, and B current sense pins, with a load current, I_L, flowing out of the B and into the A amplifier outputs. Similarly, the error current is measured as $I_{CSB}-I_{CSA}-I_L$, with I_L flowing from A into B.

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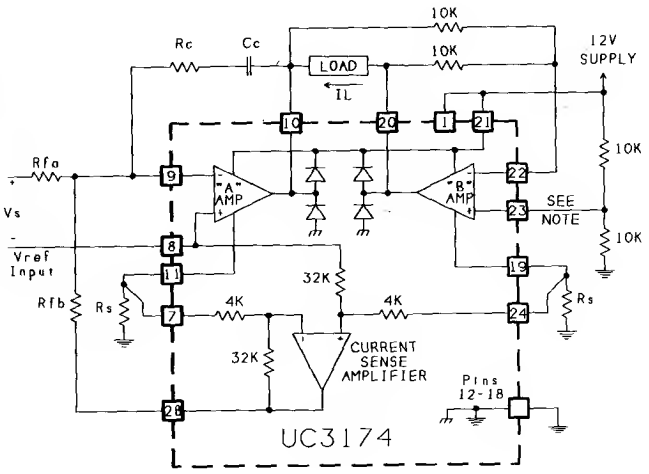
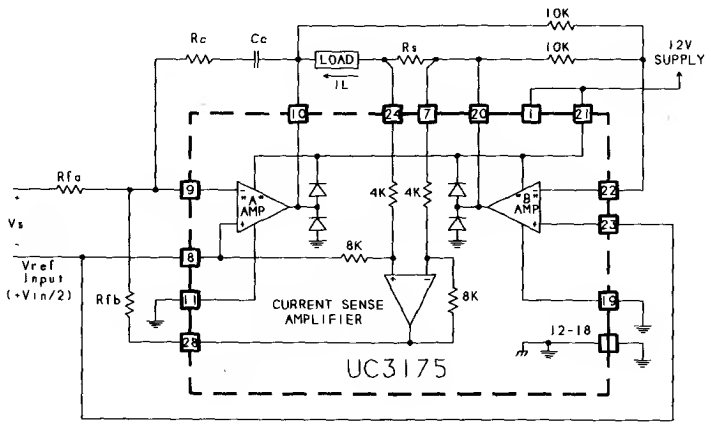
UC3174 GROUND-REFERENCED CURRENT SENSING



For maximum voltage swing, Pin 23 should see +Vin/2. If Vref at PIN 8 is at this level, then the divider is not necessary and PIN 23 can also be connected to the Vref input.

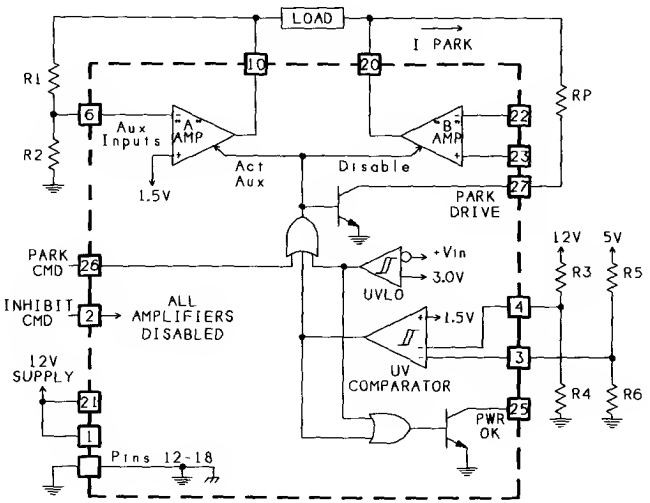
$$G_O = \frac{IL}{VS} = \frac{RFB}{(RFA*8*RS)}$$

UC3175 SERIES CURRENT SENSING



$$G_O = \frac{IL}{VS} = \frac{RFB}{(RFA*2*RS)}$$

PARKING FUNCTION



NOTES:

1. Parking voltage = $1.5V*(R_1+R_2)/R_2 - (I_L*R_P)$
2. R_P is optional for current limiting.
3. INHIBIT and PARK Inputs are active high.
4. PWR OK is low on power failure.

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INTEGRATED CIRCUITS

UNITRODE

FULL BRIDGE POWER AMPLIFIER

UC3176
UC3177

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

DESCRIPTION

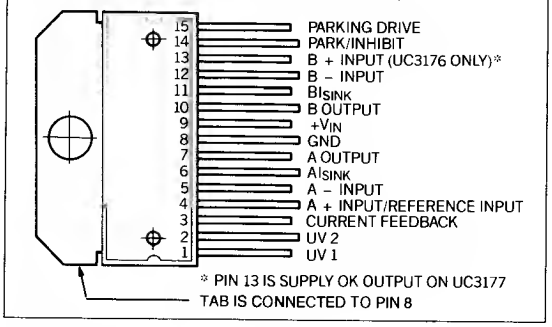
The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit logic level input is also available to force this state. The above functions are easily combined to provide a head parking function in disk head positioning applications. In addition, on the UC3177 device a separate supply OK output is available to distinguish between a supply fault and a Park/Inhibit command input.

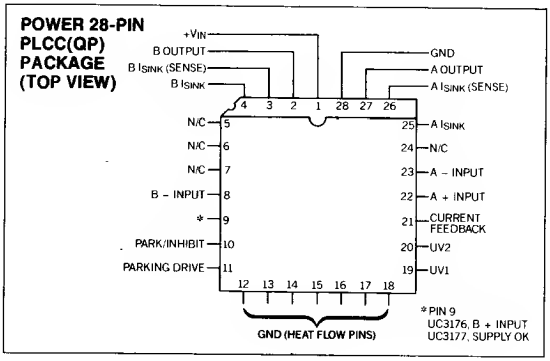
The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics. The parts are packaged in the 15 pin Multiwatt package with a maximum θ_{jc} of 3°C/Watt. For lower power applications a surface mount 28 pin PLCC package is available. Consult packaging section of catalog for package details.

CONNECTION DIAGRAMS

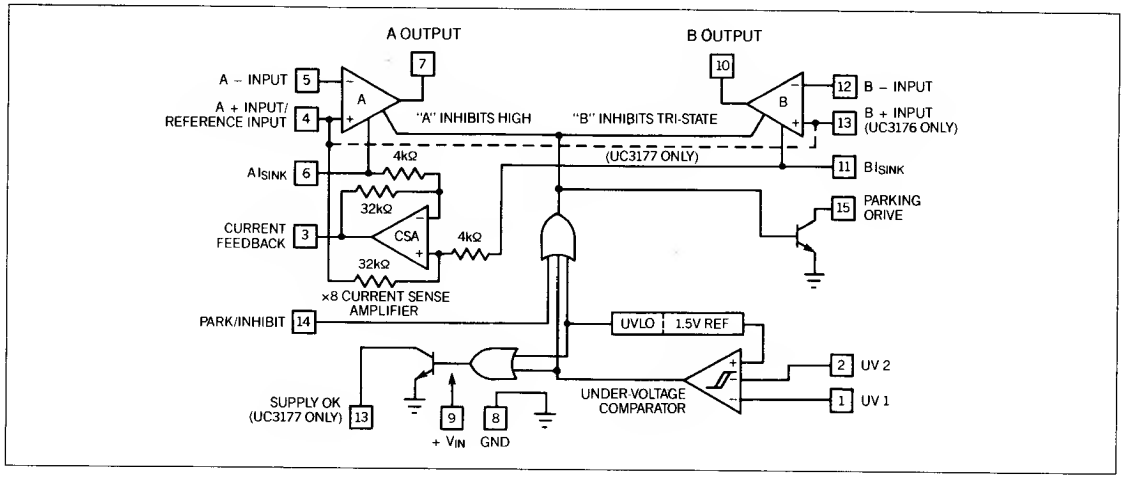
MULTIWATT 15-PIN V(VH) PACKAGE (TOP VIEW)



POWER 28-PIN PLCC(QP) PACKAGE (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (note 1)

Input Supply Voltage, ($+V_{IN}$) 40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)
  Maximum forced voltage ..... −0.3V to 10V
  Maximum forced current ..... ±10mA
Other Input Voltages ..... −0.3V to $+V_{IN}$
AI_{sink} and BI_{sink} Voltages ..... −0.3V to 6V
Open Collector Output Voltages 40V
A and B Output Currents (Continuous)
  Source ..... Internally Limited
  Sink 2.5A
Total Supply Current (Continuous) 4A
Parking Drive Output Current (Continuous) 200mA
Supply OK Output Current, UC3177 (Continuous) 30mA
Operating Junction Temperature ..... −55°C to +150°C
Power Dissipation at T_C = +75°C
  V package 25W
  QP package 4W
Storage Temperature ..... −65°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

THERMAL DATA

V package:
  Thermal Resistance Junction to Case, θ_{jc} ..... 3°C/W
  Thermal Resistance Junction to Ambient, θ_{ja} ..... 35°C/W
QP package:
  Thermal Resistance Junction to Leads, θ_{jc} ..... 15°C/W
  Thermal Resistance Junction to Ambient, θ_{ja} ..... 50°C/W

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications hold for T_A = 0 to 70°C, $+V_{in}$ = 12V. T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	$+V_{in}$ = 12V $+V_{in}$ = 35V		18 21	25 30	mA mA
UVLO Threshold	$+V_{in}$ low to high Threshold hysteresis		2.8 220	3.0 300	V mV
Power Amplifiers, A and B					
Input Offset Voltage	V_{cm} = 6V, V_{out} = 6V			8	mV
Input Bias Current	V_{cm} = 6V, Except A+ input	−500	−100		nA
Input Bias Current at A+ /Reference Input	(A+ /Ref − BI_{sink})/36Kohms T_j = 25°C	23	28	35	μA/V
Input Offset Current B Amp Only on UC3176	V_{cm} = 6V			200	nA
CMRR	V_{cm} = 1 to 33V, $+V_{in}$ = 35V, V_{out} = 6V	70	100		dB
PSRR	$+V_{in}$ = 5 to 35V, V_{cm} = 2.5V	70	100		dB
Large Signal Voltage Gain	V_{out} = 3V w/I_{out} = 1A, to V_{out} = 9V w/I_{out} = −1A	1.5	4		V/mV
Thermal Feedback	$+V_{in}$ = 20V, Pd = 20W at opposite output		25	200	μV/W
Saturation Voltage	I_{out} = −2A, High side, T_j = 25°C I_{out} = 2A, Low side, T_j = 25°C Total V_{sat} at 2A, T_j = 25°C		1.9 1.6 3.5	 3.7	V V V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/μs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications hold for T_A = 0 to 70°C, $+V_{in}$ = 12V. $T_A=T_J$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Amplifiers, A and B (continued)					
Differential I_{out} Sense Error Current in Bridge Configuration	$I_{out}(A) = -I_{out}(B)$, $/I_{out}/ - /AI_{sink} - BI_{sink}/$				
	$I_{out} \leq 200mA$		3.0	6.0	mA
	$I_{out} \leq 2A$		5.0	10	mA
High Side Current Limiting	$+V_{in} - V_{out} < 12$ V		−2.7	−2.0	A
Current Sense Amplifier					
Input Offset Voltage	V_{cm} = 0V, A+/Ref at 6V			3	mV
	Ref = 2V to 20V, $+V_{in}$ = 35, change with Reference input voltage			600	μV/V
Thermal Gradient Sensitivity	$+V_{in}$ = 20V, Ref = 10V, Pd = 20W @ A or B output		5.0	75	μV/W
PSRR	Ref = 2.5V, $+V_{in}$ = 5 to 35V	70	100		dB
Gain	$/AI_{sink} - BI_{sink}/ \leq 0.5V$	7.8	8	8.1	V/V
Slew Rate			2		V/μS
3dB Bandwidth			1		MHz
Max Output Current	I_{source}, $+V_{in} - V_{out}$ = 0.5V	2.5	3.5		mA
Output Saturation Voltage	I_{source} = 1.5mA, High side		0.15	0.30	V
	I_{sink} = 5mA, Low side		1.4	1.7	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	−2	−0.5		μA
Supply OK V_{sat} UC3177 Only	I_{out} = 5mA			0.45	V
Supply OK Leakage UC3177 Only	V_{out} = 35V			5	μA
Park/Inhibit					
Park/Inhibit Thl'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	μA
Parking Drive Saturation Voltage	I_{out} = 100mA		0.3	0.7	V
Parking Drive Leakage	V_{out} = 35V			15	μA
Thermal Shutdown					
Shutdown Temperature			165		°C

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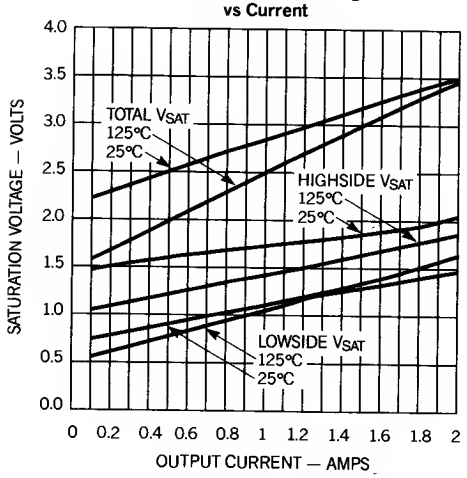
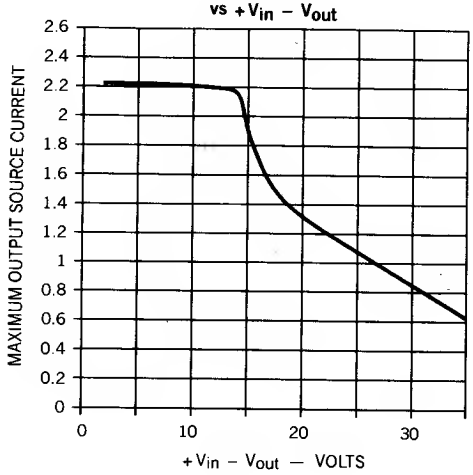
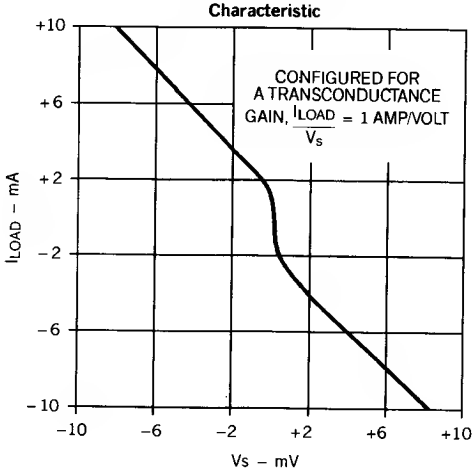
Output Saturation Voltage vs Current



Maximum Source Current vs $+V_{in} - V_{out}$

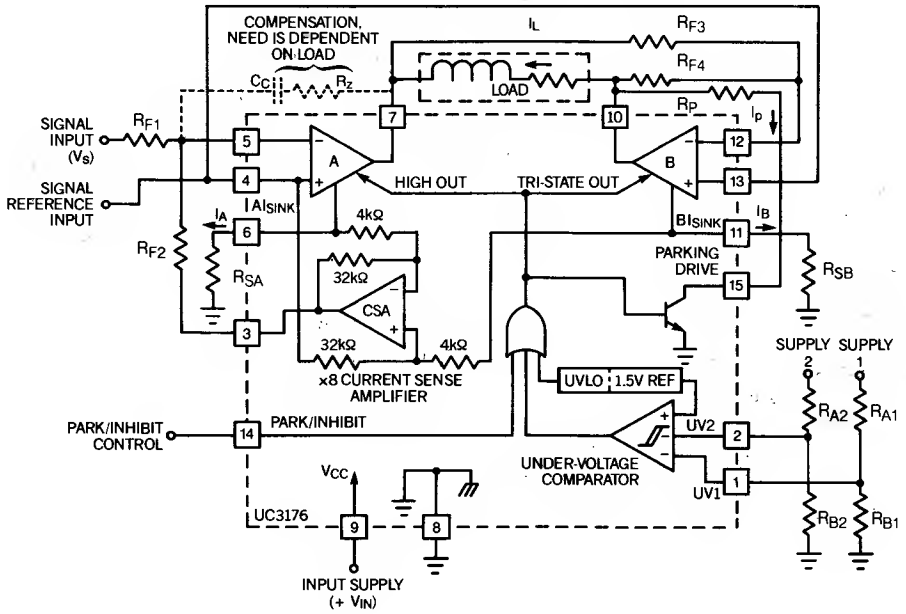


Crossover Current Error Characteristic

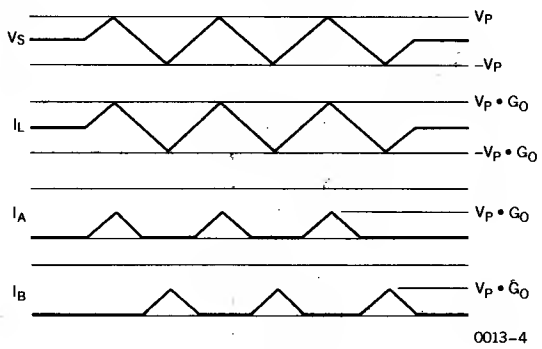


APPLICATION AND OPERATION INFORMATION

THE UC3176 IN A FULL BRIDGE TRANSCONDUCTANCE AMPLIFIER



WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

$$\text{Transconductance } (G_O) = \frac{I_L}{R_S} = \frac{R_{F2}}{R_{F1}} \cdot \left(\frac{1}{8R_S}\right)$$

With: $R_{SA} = R_{SB} = R_S$, and $R_{B1} = R_{B2}$

$$\text{Parking Current } (I_P) = \frac{V_{IN} - 1.5}{R_P + R_L}$$

Where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
High to Low Threshold, $(V_{LH}) = 1.425\,(R_A + R_B)/R_B$
Low to High Threshold, $(V_{HL}) = 1.5\,(R_A + R_B)/R_B$

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INTEGRATED CIRCUITS

UNITRODE

UC3622

Switchmode Driver For 3-ϕ Brushless DC Motors

FEATURES

- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Fixed-Frequency Pulse-Width Modulation for Servo Applications
- TTL Compatible Hall Inputs
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt® Package
- 24 Lead, 25W Power Ceramic Dil

DESCRIPTION

The UC3622 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board oscillator and latched PWM comparator provide the necessary circuitry for implementing a fixed-frequency, pulse width modulated servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been reduced by limiting the output dv/dt to 150μs for any load condition.

The UC3622 will decode and drive all 3-phase motors with hall decode schemes compatible with Table 1. All other schemes can be decoded with the additional of a single external inverter. This product is available in military versions.

ABSOLUTE MAXIMUM RATINGS (Note 1)

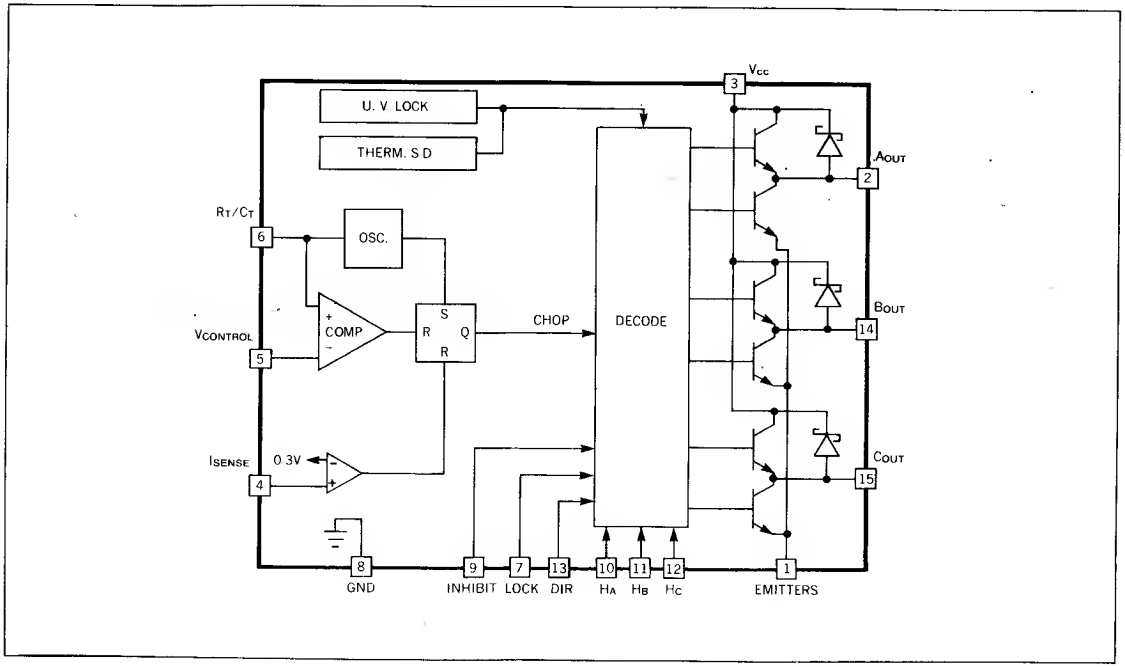
Supply Voltage, V_{cc} 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), I_O 3A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
  DC Operation 2A
Analog Inputs ..... -0.3 to $+V_{cc}$
Logic Inputs ..... -0.3 to $+V_{cc}$
Total Power Dissipation (at T_{CASE} = 75°C) 25W
Storage and Junction Temperature ..... −40°C to +150°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

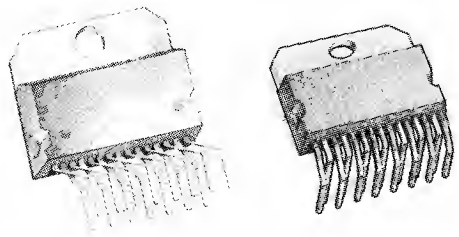
Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max
Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

BLOCK DIAGRAM

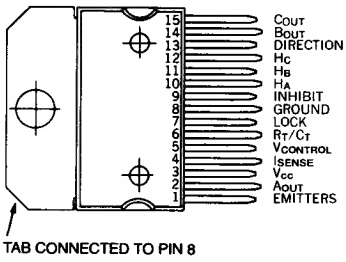


STANDARD PACKAGES

V Package **VH Package**



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{CC(PIN\ 3)}$ = 20V, R_T = 47k, C_T = .015μF) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM Comparator Section					
Input Offset Voltage				10	mV
Input Bias Current				5	μA
Current Sense Section					
Input Bias Current				5	μA
Internal Offset Voltage		.25	0.3	.35	V
Oscillator Section					
Initial Accuracy	T_j = 25°C	9	10	11	kHz
Temperature Stability	Over Operating Range		2		%
Ramp Peak			3.6		V
Ramp Valley			1.3		V
Decoder Section					
High-Level Input Voltage		2.5			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	μA
Low-Level Input Current		-10			μA
Output Section					
Output Leakage Current	V_{CC} = 40V			500	μA
V_F, Schottky Diode	I_O = 2A		1.5	2.0	V
Total Output Voltage Drop	I_O = 2A, Note 3		3.0	3.6	V
Output Rise Time	RL=44Ω		150		ns
Output Fall Time	RL=44Ω		150		ns
Under-Voltage Lockout					
Start-Up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current			32	55	mA

Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. The total voltage drop is defined as the sum of both top and bottom side driver.

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TABLE 1

STEP	INHIBIT	DIR	H_a	H_b	H_c	LOCK		A_{OUT}	B_{OUT}	C_{OUT}
1	0	1	1	0	0	1		ϕ	H	L
2	0	1	1	1	0	1		L	H	ϕ
3	0	1	1	1	1	1		L	ϕ	H
4	0	1	0	1	1	1		ϕ	L	H
5	0	1	0	0	1	1		H	L	ϕ
6	0	1	0	0	0	1		H	ϕ	L
1	0	0	1	1	1	1		H	ϕ	L
2	0	0	1	1	0	1		H	L	ϕ
3	0	0	1	0	0	1		ϕ	L	H
4	0	0	0	0	0	1		L	ϕ	H
5	0	0	0	0	1	1		L	H	ϕ
6	0	0	0	1	1	1		ϕ	H	L
—	1	X	X	X	X	X		ϕ	ϕ	ϕ
—	0	X	X	X	X	0		H	ϕ	L

H = HIGH OUTPUT L = LOW OUTPUT ϕ = OPEN (TRISTATE) OUTPUT

CIRCUIT DESCRIPTION

The UC3622 is designed for implementation of a complete 3-phase brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

Table 1 shows the logic scheme employed to decode and drive each of three high current, totem pole, output stages. A forward/reverse signal, Pin 13, is used to provide direction. At any time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by chopping all drivers during current control (fixed-frequency PWM), producing a four-quadrant, regenerative mode drive. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses.

HALL INPUTS

The Hall input pins (#10, 11, 12) are not provided with internal pull-up resistors. If these are required for the Hall devices, they must be added externally.

CURRENT LIMIT

Referring to Figure 1, emitter current is sensed across R_{LIMIT} and fed back through a low pass filter to the current sense, Pin 4. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1k and 1000pF range. An internal 0.3V reference voltage limits the motor current to

$$I_{max} = \frac{0.3}{R_{LIMIT}}$$

TIMING

An RC circuit at Pin 6 is used to set the PWM frequency, as shown in Figure 2. The frequency is determined by the formula

$$f \approx \frac{V_{OSC} - 2.43}{2.27\ R_T\ C_T}\ [\text{Hz}]$$

Note: R_T should be chosen so that

$$50\mu A < \frac{V_{OSC} - 2.27}{2.27\ R_T} < 1mA$$

INHIBIT

The INHIBIT input (Pin 9) must be low during normal operation. A high level at this pin forces all three outputs to the open state, and can be used to allow the motor to coast.

LOCK

A low level at LOCK (Pin 7), together with a low level at INHIBIT, sets the following output condition:

A_{OUT} ------- HIGH
B_{OUT} ------- OPEN
C_{OUT} ------- LOW

This can be used as part of a circuit intended to force the motor shaft to a desired parking position.

PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-stated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

APPLICATION MATERIAL

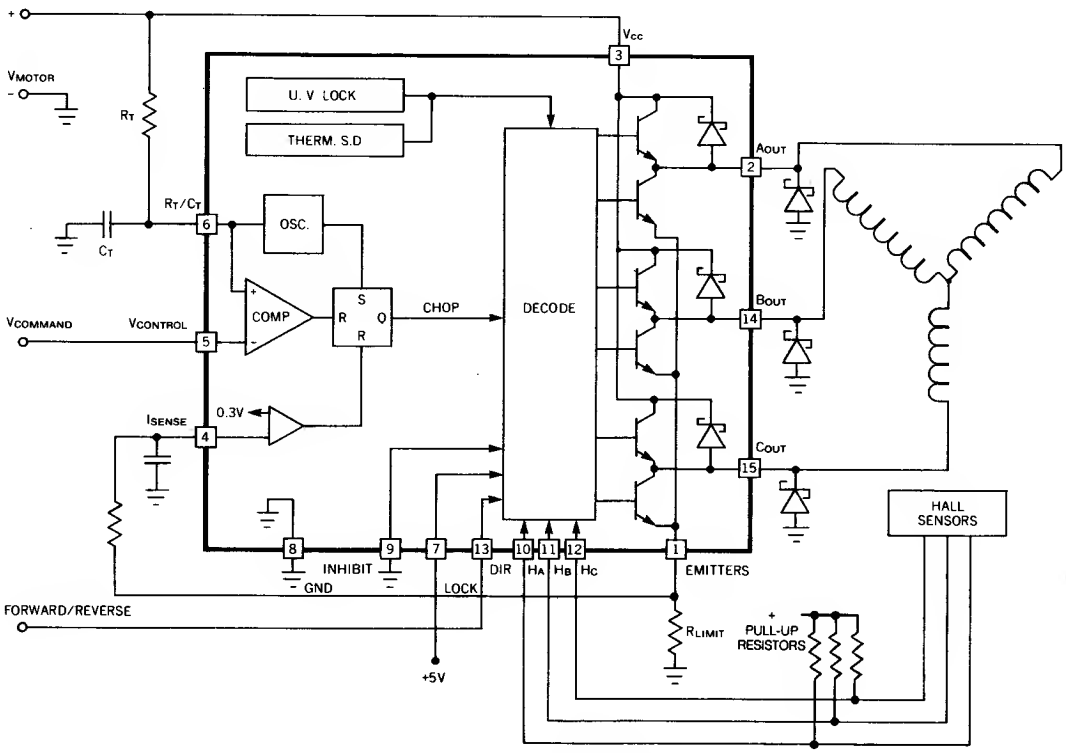

Figure 1. Open Loop Speed Control with Current Limiting

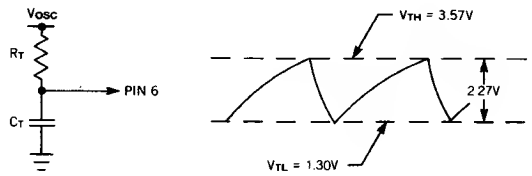

Figure 2. PWM Oscillator Waveform

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INTEGRATED CIRCUITS
UNITRODE

Low Noise Switchmode Driver For 3-ϕ Brushless DC Motors

FEATURES

- 1A Continuous, 2A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Servo Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt® Package

DESCRIPTION

Designed specifically for noise-sensitive environments, the UC3623V monolithic driver IC offers the high efficiency of a chopper drive and the low EMI attainable with controlled output slew rates.

The UC3623 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/μs for any load condition.

The UC3623 offers standard 120 electrical degree. Hall decoding per Table 1.

ABSOLUTE MAXIMUM RATINGS (Note 1)

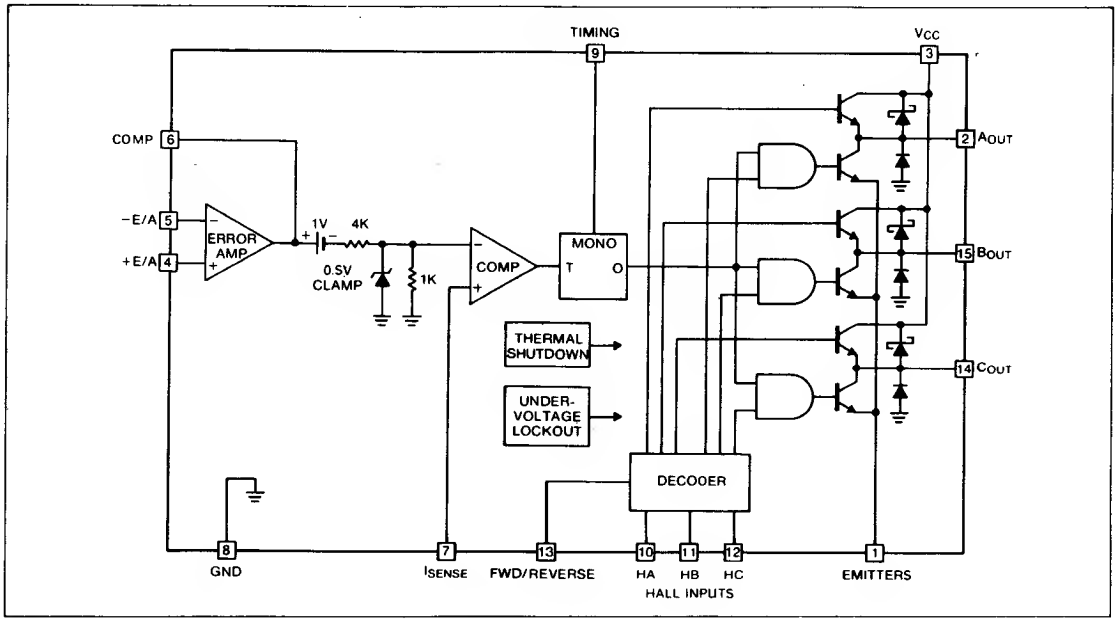
Supply Voltage, V_{CC} 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), I_O 2A
  Repetitive (80% on - 20% off; t_{ON} = 10ms) 1.5A
  DC Operation 1A
Analog Inputs ..... -0.3 to $+V_{CC}$
Logic Inputs ..... -0.3 to $+V_{CC}$
Total Power Dissipation (at T_{CASE} = 75°C) 25W
Storage and Junction Temperature ..... -40°C to +150°C

Note: 1. All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

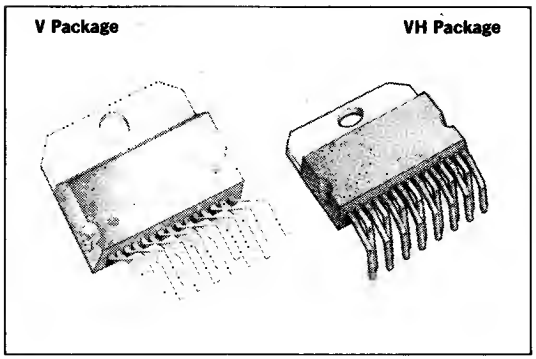
THERMAL DATA

Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max
Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

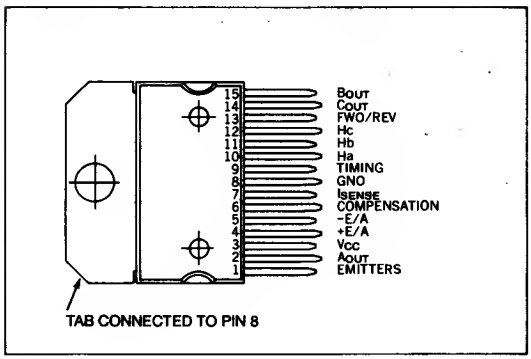
BLOCK DIAGRAM



MECHANICAL DATA



CONNECTION DIAGRAM (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{CC(PIN\ 3)}$ = 20V, R_T = 10k, C_T = 2.2nF) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Error Amplifier Section					
Input Offset Voltage			1.5	10	mV
Input Bias Current			-.25	-2.0	μA
Input Offset Current			15	250	nA
Common Mode Range	V_{CC} = 8V to 40V	0		V_{IN}-2	V
Open Loop Gain	$\Delta V_{PIN\ 6}$ = 1V to 4V	80	100		dB
Unity Gain Bandwidth	T_j = 25°C, Note 2		0.8		MHz
Output Sink Current	$V_{PIN\ 6}$ = 1V		2		mA
Output Source Current	$V_{PIN\ 6}$ = 4V		8		mA
Current Sense Section					
Input Bias Current			-2.0	-5	μA
Internal Clamp		.425	0.5	.575	V
Divider Gain		.180	0.2	.220	V/V
Internal Offset Voltage		.8	1.0	1.2	V
Timing Section					
Output Off Time		18	20	22	μs
Upper Mono Threshold			5.0		V
Lower Mono Threshold			2.0		V
Decoder Section					
High-Level Input Voltage		2.2			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	μA
Low-Level Input Current		-10			μA
Output Section					
Output Leakage Current	V_{CC} = 40V			500	μA
V_F, Schottky Diode	I_o = 1A		1.5	2.0	V
V_F, Substrate Diode	I_o = 1A		2.2	3.0	V
Total Output Voltage Drop	I_o = 1A, Note 3		3.0	3.6	V
Output Rise Time	RL = 44Ω		350		ns
Output Fall Time	RL = 44Ω		170		ns

Notes: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. The total voltage drop is defined as the sum of both top and bottom side driver.

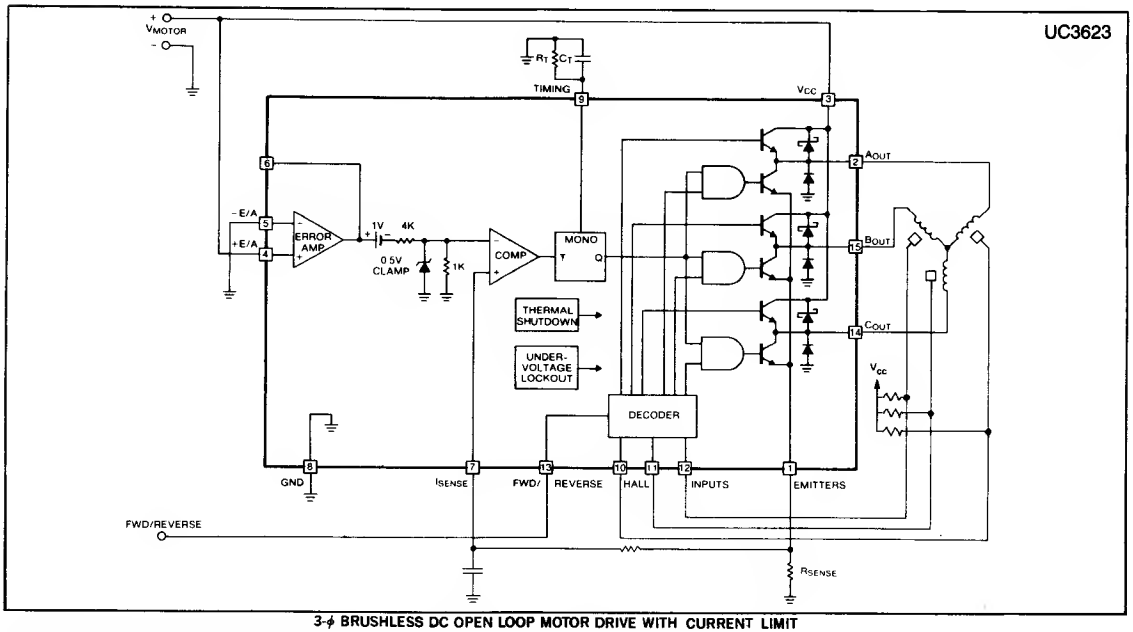
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; $V_{cc(PIN\ 3)}$ = 20V, R_T 10k, C_T = 2.2nF) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Under-Voltage Lockout					
Start-Up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current			32	55	mA

TABLE 1

STEP	FWD/ REV	Ha	Hb	Hc		AOUT	BOUT	COUT
1	1	1	0	1		H	L	0
2	1	1	0	0		H	0	L
3	1	1	1	0		0	H	L
4	1	0	1	0		L	H	0
5	1	0	1	1		L	0	H
6	1	0	0	1		0	L	H
1	0	1	0	1		L	H	0
2	0	1	0	0		L	0	H
3	0	1	1	0		0	L	H
4	0	0	1	0		H	L	0
5	0	0	1	1		H	0	L
6	0	0	0	1		0	H	L

TYPICAL APPLICATIONS



3-ϕ BRUSHLESS DC OPEN LOOP MOTOR DRIVE WITH CURRENT LIMIT

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UC3655

Low Saturation, Linear Brushless DC Motor Driver

FEATURES

- Total saturation voltage of less than one volt
- Sink current capability of up to three amps
- Quiescent current less than 10 mA
- Single supply 5 volt operation
- Motor voltage of 5 to 40 volts
- Full decode for 3 phase TTL hall sensors
- 120 electrical degree logic
- Linear closed-loop motor current control

DESCRIPTION

The UC3655 DC motor driver achieves extremely efficient operation by using external PNP transistors selected for low saturation voltage as high side drivers. These are complemented with low side NPN drivers internal to the UC3655 which also have very low saturation losses. The PNP's can be low power devices as they are always switched into saturation by the action of internal 100 mA base drivers, while the on-chip NPN's are driven linearly to control motor current. The result is a total source/sink saturation voltage drop of less than one Volt at one Amp load current.

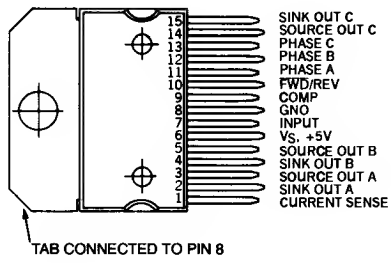
This controller offers further efficiency by using only a five volt supply with a current requirement proportional to motor current. The quiescent supply current with the outputs off is less than 10 mA.

In addition to the power output stages, the UC3655 contains 120 electrical degree hall logic decoding with forward, reverse, and inhibit functions selectable by a single pin. Also included in control amplifier to drive the sink output current linearly reposonse to an input command voltage.

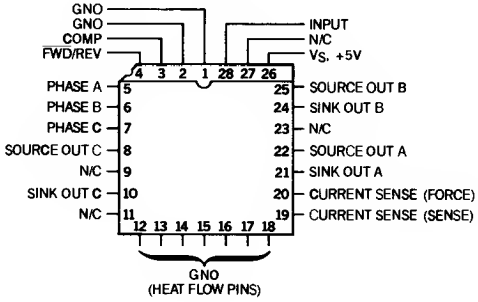
Finally, full protection is offered with under-voltage lockout, current limiting, and thermal shutdown. The UC3655 is packaged in both a high-power 15-pin Multiwatt® plastic package and, for low power requirements, a 28-pin PLCC surface mount configuration.

CONNECTION DIAGRAMS (TOP VIEW)

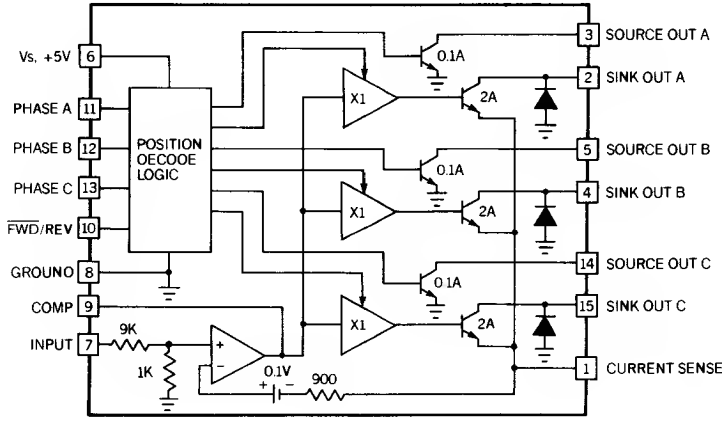
UC3655V(H)



UC3655QP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_S 7V
Output Voltage, V_C (Source and Sink) 40V
Sink Output Current 3A
Source Drive Current . . . . . Internally Limited
Logic and Analog Inputs . . . . . −0.3 to 7V
Total Power Dissipation (At T_{tab} = 75°C)
V Package 25W
QP Package 4.0W
Storage and Junction Temperature . . . . . −40°C to 150°C

Note: 1. All voltages are with respect to ground.
Currents are positive into, negative out of the specified terminal.

THERMAL DATA:

V Package: Thermal Resistance to Tab, θ_{jc} . . . . . 3°C/W
Thermal Resistance to Ambient, θ_{ja} . . . . . 35°C/W
QP Package: Thermal Resistance to Leads, θ_{jc} . . . . . 15°C/W
Thermal Resistance to Ambient, θ_{ja} . . . . . 50°C/W

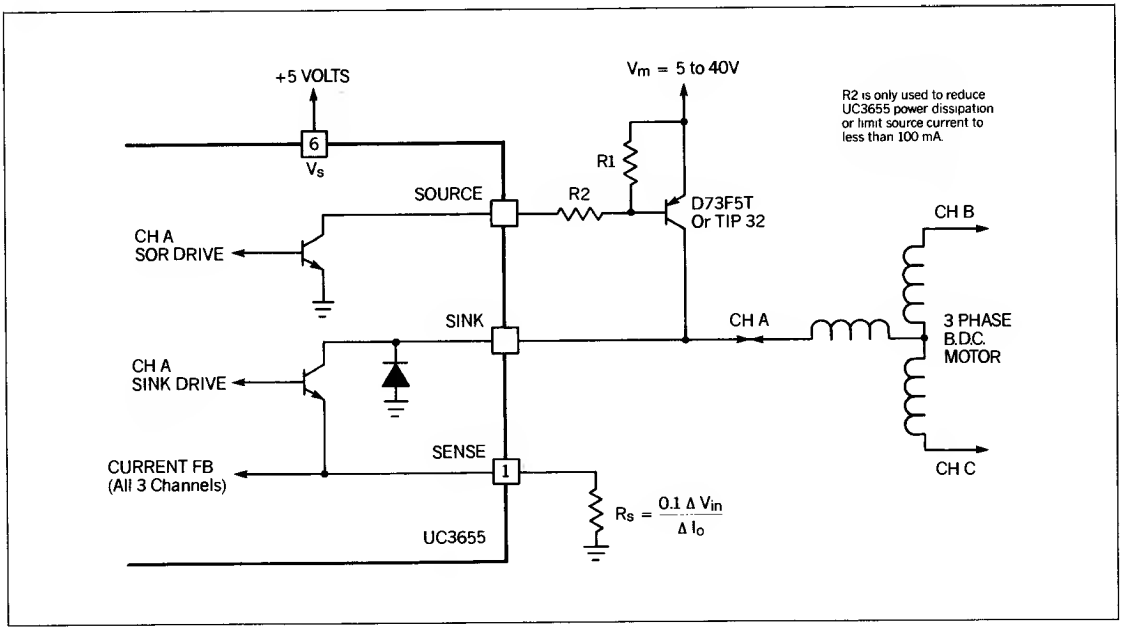
ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, V_S = 5.0 Volts, and R_{SENSE} = 0.2 Ohm). T_A=T_J

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Sink Driver Section					
Collector Leakage	V_C = 40V			500	μA
Saturation Voltage	I_C = 2A, R_S = 0		0.8	1.0	V
	I_C = 1A, R_S = 0		0.4	0.5	V
Coll. Diode V_f	I_f = −1A			2.0	V
Source Driver Section					
Collector Leakage	V_C = 40V			100	μA
Saturation Voltage	I_C = 0.1A		1.9	2.3	V
Current Limit	V_C = 5V, T_A = 25°C	100	175	300	mA
Amplifier Section					
Input Low Voltage	Sink Current= 0A	0.8	1.0	1.2	V
Input High Voltage	Sink Current = 2A	4.5	5.0	5.5	V
Closed Loop Transconductance	Sink Current = 0-2A	.45	0.5	.55	S
Control Amp Transconductance	I_{COMP} = ±50μA		0.2		mS
Voltage Gain to Current Sense	V_{IN} = 2-3V		−20		dB
Input Bias Current	V_{IN} = 5V		0.5	1.0	mA
Comp. Source Current	V_{IN} = 5V, V_{COMP} = .9V	−50	−100	−150	μA
Comp. Sink Current	V_{IN} = 0V, V_{COMP} = .9V	50	100	150	μA
Decoder Section					
High-level Input Voltage	Phase Input	2.2			V
Low-level Input Voltage	Phase Input			0.8	V
High-level Input Current	Phase Input			10	μA
Low-level Input Current	Phase Input	−10			μA
Input Voltage to Inhibit	$\overline{FWD}$/REV	1.8		3.2	V
Forward Command Input V	$\overline{FWD}$/REV			0.6	V
Reverse Command Input V	$\overline{FWD}$/REV	4.4			V
Supply Section					
Turn-on Threshold	V_S Low to High	3.5	4.0	4.7	V
Threshold Hysteresis			0.5		V
Supply Current	Outputs Inhibited		6.0	10	mA
Supply Current	Sink Current = 2A		25	100	mA
Thermal Shutdown	Junction Temperature		150		°C
Shutdown Hysteresis	Junction Temperature		25		°C

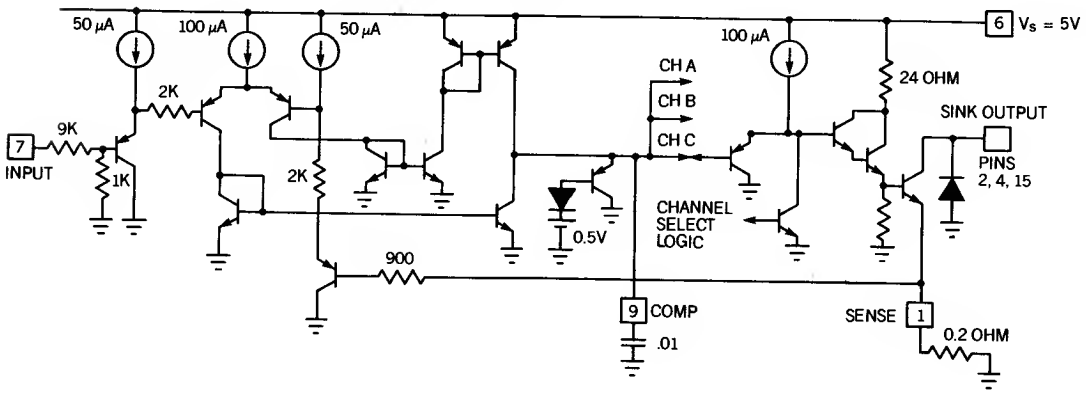
DECODE LOGIC TRUTH TABLE: (Note: X = Don't Care, Inh = 2.5 ±1V, H and L levels defined by application, Motor Term O = High Impedance).

Inhibit / Fwd/Rev	Phase Input			Source Drive			Sink Output			Motor Term		
	A	B	C	A	B	C	A	B	C	A	B	C
X	0	0	0	Off	Off	Off	Off	Off	Off	O	O	O
X	1	1	1	Off	Off	Off	Off	Off	Off	O	O	O
Inhibit	X	X	X	Off	Off	Off	Off	Off	Off	O	O	O
L	1	0	1	On	Off	Off	Off	On	Off	H	L	O
L	1	0	0	On	Off	Off	Off	Off	On	H	O	L
L	1	1	0	Off	On	Off	Off	Off	On	O	H	L
L	0	1	0	Off	On	Off	On	Off	Off	L	H	O
L	0	1	1	Off	Off	On	On	Off	Off	L	O	H
L	0	0	1	Off	Off	On	Off	On	Off	O	L	H
H	1	0	1	Off	On	Off	On	Off	Off	L	H	O
H	1	0	0	Off	Off	On	On	Off	Off	L	O	H
H	1	1	0	Off	Off	On	Off	On	Off	O	L	H
H	0	1	0	On	Off	Off	Off	On	Off	H	L	O
H	0	1	1	On	Off	Off	Off	Off	On	H	O	L
H	0	0	1	Off	On	Off	Off	Off	On	O	H	L

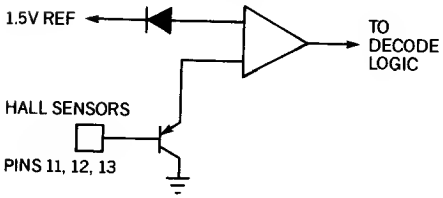
TYPICAL MOTOR DRIVE APPLICATION



Linear Transconductance Amplifier

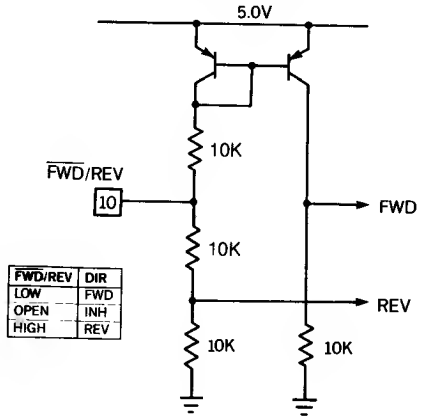


Phase Inputs



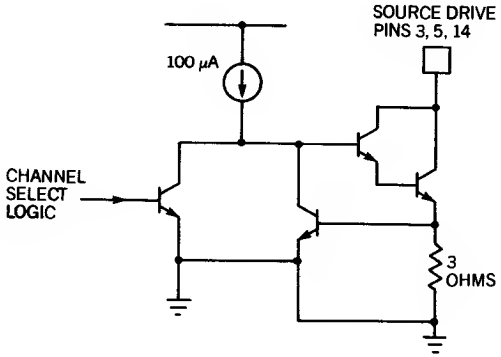
Note: Input pull-up resistors are not included.

Forward/Reverse Input

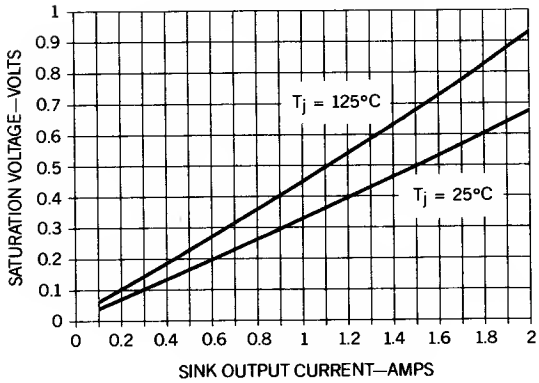


$\overline{\text{FWD/REV}}$	DIR
LOW	FWD
OPEN	INH
HIGH	REV

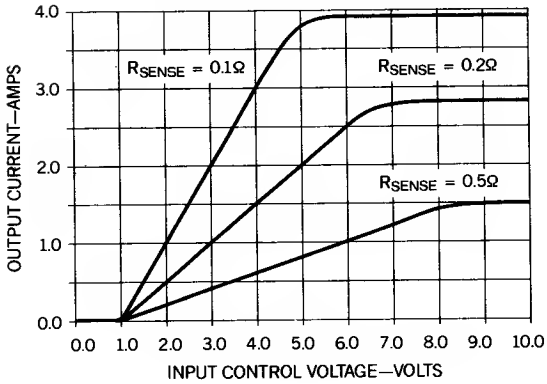
Source Drivers



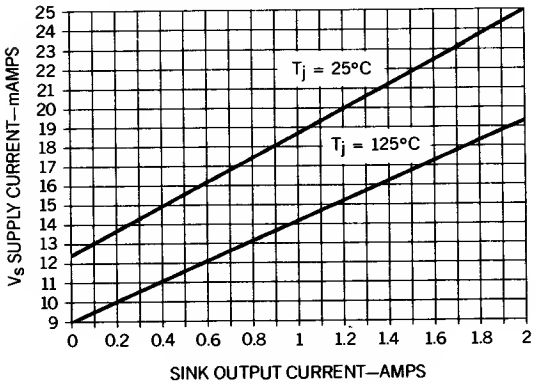
Sink Output V_{SAT} vs Current



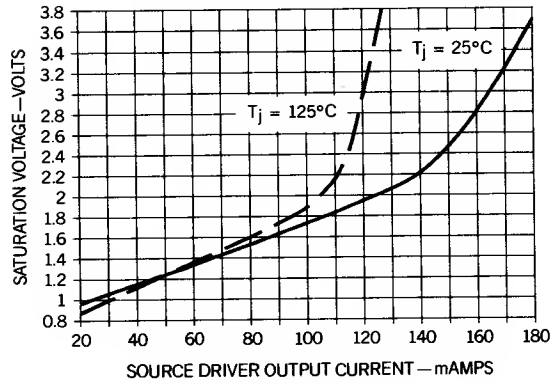
Control Transfer Characteristics



V_S Supply Current vs Sink Current



Source Driver Output V_{SAT} vs Current



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INTEGRATED CIRCUITS

UNITRODE

UC3717A

Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability
- Bipolar Output Current up to 1A
- Wide Range of Motor Supply Voltage 10-46V
- Low Saturation Voltage with Integrated Bootstrap
- Built-In Fast Recovery Commutating Diodes
- Current Levels Selected in Steps or Varied Continuously
- Thermal Protection with Soft Intervention

DESCRIPTION

The UC3717A is an improved version of the UC3717, used to switch drive the current in one winding of a bipolar stepper motor. The UC3717A has been modified to supply higher winding current, more reliable thermal protection, and improved efficiency by providing integrated bootstrap circuitry to lower recirculation saturation voltages. The diagram shown below presents the building blocks of the UC3717A. Included are an LS-TTL compatible logic input, a current sensor, a monostable, a thermal shutdown network, and an H-bridge output stage. The output stage features built-in fast recovery commutating diodes and integrated bootstrap pull up. Two UC3717As and a few external components form a complete control and drive unit for LS-TTL or microprocessor controlled stepper motor systems.

The UC3717A is characterized for operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{CC} 7V
- Output Supply, V_m 50V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) ..... V_{CC}
- Reference Input (Pin 11) 15V

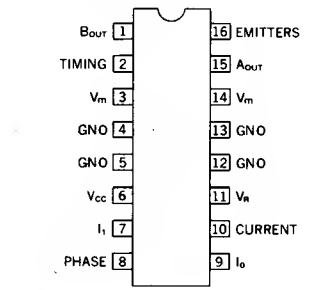
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1.2A
Junction Temperature, T_j ..... +150°C
Thermal Resistance, Junction to Ambient (NE Package) ..... 45°C/W
Thermal Resistance, Junction to Case (NE Package) ..... 11°C/W
Thermal Resistance, Junction to Ambient (J Package) ..... 100°C/W
Thermal Resistance, Junction to Case (J Package) ..... 60°C/W
Storage Temperature Range, Ts ..... -55°C to +150°C

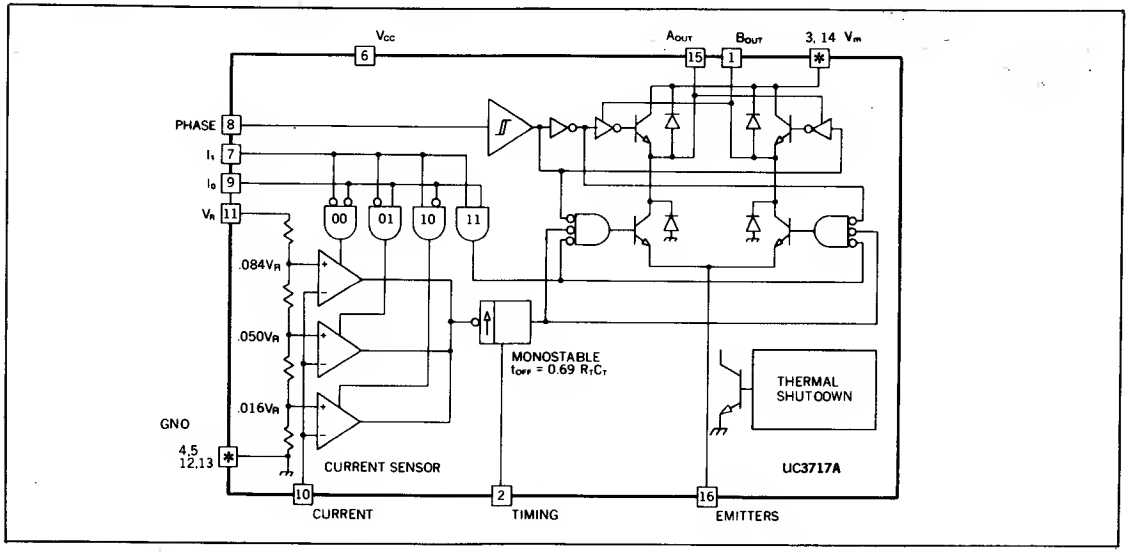
Note: 1. All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or NE PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, Figure 6. V_m = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to +70°C, unless otherwise stated). T_A=T_J

PARAMETERS	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_m (Pins 3, 14)			10		46	V
Logic Supply Voltage, V_{CC} (Pin 6)			4.75		5.25	V
Logic Supply Current, I_{CC} (Pin 6)	I_0 = I_1 = 0			7	15	mA
Thermal Shutdown Temperature			+160		+180	°C
Logic Inputs						
Input Low Voltage (Pins 7, 8, 9)					0.8	V
Input High Voltage (Pins 7, 8, 9)			2		V_{CC}	V
Low Voltage Input Current (Pins 7, 8, 9)	V_i = 0.4V	Pin 8			-100	μA
		Pins 7, 9			-400	
High Voltage Input Current (Pins 7, 8, 9)	V_i = 2.4V				10	μA
Comparators						
Comparator Low Threshold Voltage (Pin 10)	V_R = 5V	I_0 = L, I_1 = H	66	80	90	mV
Comparator Medium Threshold Voltage (Pin 10)	V_R = 5V	I_0 = H, I_1 = L	236	250	266	mV
Comparator High Threshold Voltage (Pin 10)	V_R = 5V	I_0 = L, I_1 = L	396	420	436	mV
Comparator Input Current (Pin 10)					±20	μA
Cutoff Time, t_{OFF}	R_T = 56KΩ	C_T = 820pF	25		35	μs
Turn Off Delay, t_d	(See Figure 5)				2	μs
Source Diode-Transistor Pair						
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = -0.5A	Conduction Period		1.7	2.1	V
	(See Figure 5)	Recirculation Period		1.1	1.35	
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = -1A	Conduction Period		2.1	2.8	V
	(See Figure 5)	Recirculation Period		1.7	2.5	
Leakage Current	V_m = 40V				300	μA
Diode Forward Voltage V_F	I_m = -0.5A			1	1.25	V
	I_m = -1A			1.3	1.7	
Sink Diode-Transistor Pair						
Saturation Voltage, V_{sat} (Pins 1, 15)	I_m = 0.5A			1.1	1.35	V
	I_m = 1A			1.6	2.3	
Leakage Current	V_m = 40V				300	μA
Diode Forward Voltage V_F	I_m = 0.5A			1.1	1.5	V
	I_m = 1A			1.4	2	

5

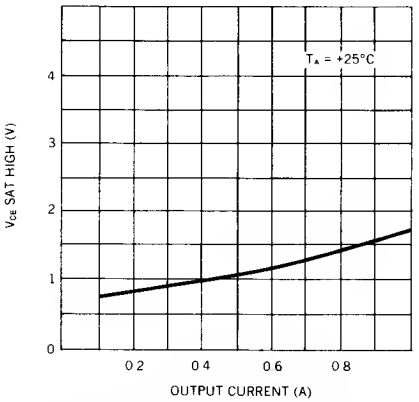


Figure 1. Typical Source Saturation Voltage vs Output Current (Recirculation Period)

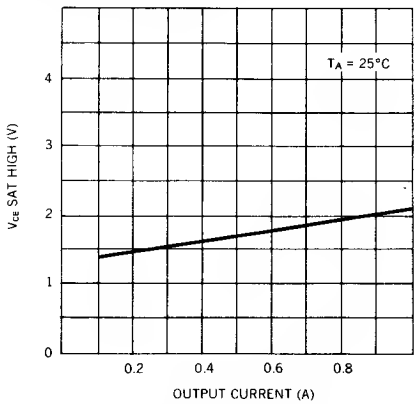


Figure 2. Typical Source Saturation Voltage vs Output Current (Conduction Period)

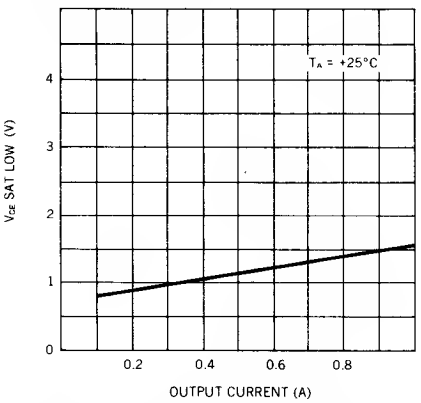


Figure 3. Typical Sink Saturation Voltage vs Output Current

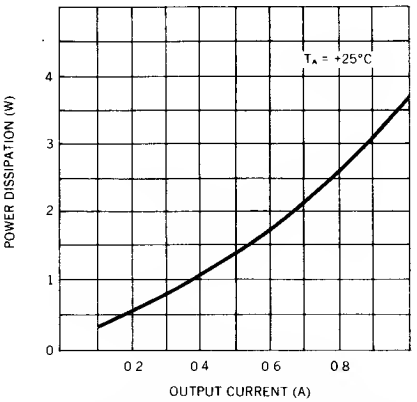


Figure 4. Typical Power Dissipation vs Output Current

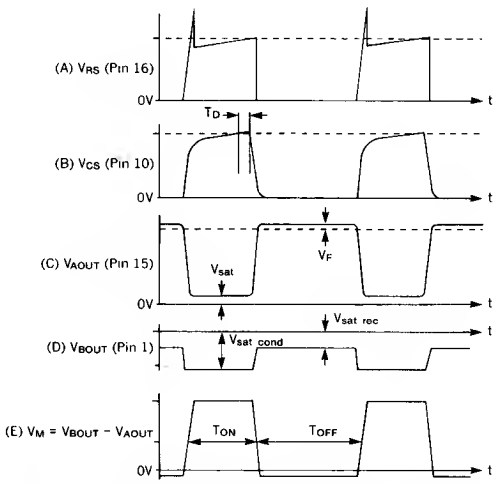


Figure 5. Typical Waveforms with MA Regulating (phase = 0)

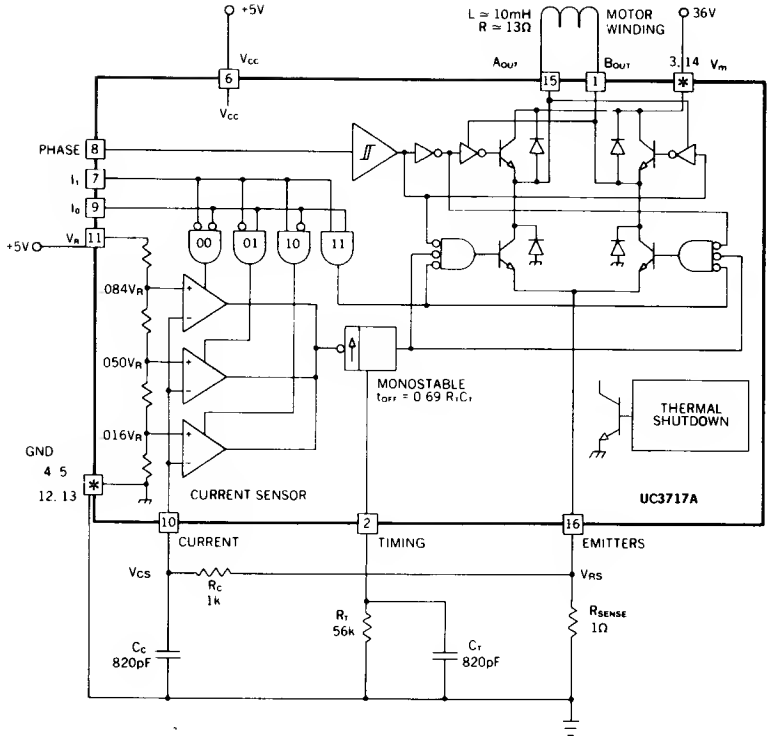


Figure 6. UC3717A Test Circuit

FUNCTIONAL DESCRIPTION

The UC3717A's drive circuit shown in the block diagram includes the following components:

(1) H-bridge output stage
(2) Phase polarity logic
(3) Voltage divider coupled with current sensing comparators
(4) Two-bit D/A current level select
(5) Monostable generating fixed off-time
(6) Thermal protection

OUTPUT STAGE

The UC3717A's output stage consists of four Darlington power transistors and associated recirculating power diodes in a full H-bridge configuration as shown in Figure 7. Also presented, is the new added feature of integrated bootstrap pull up, which improves device performance during switched mode operation. While in switched mode, with a low level phase polarity input, Q2 is on and Q3 is being switched. At the moment Q3 turns off, winding current begins to decay through the commutating diode pulling the collector of Q3 above the supply voltage. Meanwhile, Q6 turns on pulling the base of Q2 higher than its previous value. The net effect lowers the saturation voltage of source transistor Q2 during recirculation, thus improving efficiency by reducing power dissipation.

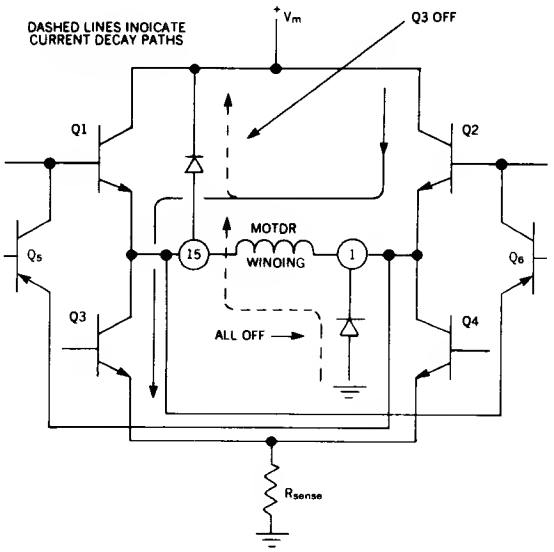


Figure 7. Simplified Schematic of Output Stage

PHASE POLARITY INPUT

The UC3717A phase polarity input controls current direction in the motor winding. Built-in hysteresis insures immunity to noise, something frequently present in switched-drive environments. A low level phase polarity input enables Q2 and Q3 as shown in Figure 7. During phase reversal, the active transistors are both turned off while winding current decays through the commutating diodes shown. As winding current decays to zero, the inactive transistors Q1 and Q4 turn on and charge the winding with current of the reverse direction. This delay insures noise immunity and freedom from power supply current spikes caused by overlapping drive signals.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

CURRENT CONTROL

The voltage divider, comparators, monostable, and two-bit D/A provide a means to sense winding peak current, select winding peak current, and disable the winding sink transistors.

The UC3717A switched driver accomplishes current control using an algorithm referred to as "fixed off-time." When a voltage is applied across the motor winding, the current through the winding increases exponentially. The current can be sensed across an external resistor as an analog voltage proportional to instantaneous current. This voltage is normally filtered with a simple RC low-pass network to remove high-frequency transients, and then compared to one of the three selectable thresholds. The two-bit D/A input signal determines which one of the three thresholds is selected, corresponding to a desired winding peak current level. At the moment the sense voltage rises above the selected threshold, the UC3717A's monostable is triggered and disables both output sink drivers for a fixed off-time. The winding current then circulates through the source transistor and appropriate diode. The reference terminal of the UC3717A provides a means of continuously adjusting the current threshold to allow microstepping. Table 1 presents the relationship between the two-bit D/A input signal and selectable current level.

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	CURRENT INHIBIT

OVERLOAD PROTECTION

The UC3717A is equipped with a new, more reliable thermal shutdown circuit which limits the junction temperature to a maximum of 180°C by reducing the winding current.

PERFORMANCE CONSIDERATIONS

In order to achieve optimum performance from the UC3717A careful attention should be given to the following items.

External Components

The UC3717A requires a minimal number of external components to form a complete control and switch drive unit. However, proper selection of external components is necessary for optimum performance. The timing pin, (pin 2) is normally connected to an RC network which sets the off-time for the sink power transistor during switched mode. As shown in Figure 8, prior to switched mode, the winding current increases exponentially to a peak value. Once peak current is attained the monostable is triggered which turns off the lower sink drivers for a fixed off-time. During off-time winding current decays through the appropriate diode and source transistor. The moment off-time times out, the motor current again rises exponentially producing the ripple waveform shown. The magnitude of winding ripple is a direct function of off-time. For a given off-time t_{OFF}, the values of R_T and C_T can be calculated from the expression:

$$T_{OFF} = 0.69 R_T C_T$$

with the restriction that R_T should be in the range of 10-100k. As shown in Figure 5, the switch frequency F_S is a function of T_{OFF} and T_{ON}. Since T_{ON} is a function of the reference voltage, sense resistor, motor supply, and winding electrical characteristics, it generally varies during different modes of operation. Thus, F_S may be approximated nominally as:

$$F_S = 1 \; / \; 1.5 \; (T_{OFF})$$

Normally, switch frequency is selected greater than 20kHz to prevent audible noise, and lower than 100kHz to limit power consumed during the switching cycle.

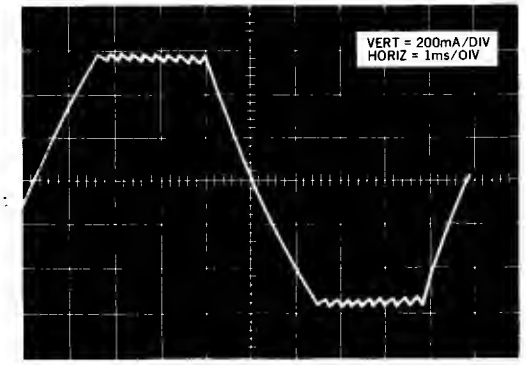


Figure 8. A typical winding current waveform. Winding current rises exponentially to a selected peak value. The peak value is limited by switched mode operation producing a ripple in winding current. A phase polarity reversal command is given and winding current decays to zero, then increases exponentially in the reverse direction.

Low-pass filter components R_C C_C should be selected so that all switching transients from the power transistors and commutating diodes are well smoothed, but the primary signal, which can be in the range of $1/T_{OFF}$ or higher must be passed. Figure 5a shows the waveform which must be smoothed, Figure 5b presents the desired waveform that just smooths out overshoot without radical distortion.

The sense resistor should be chosen as small as practical to allow as much of the winding supply voltage to be used as overdrive to the motor winding. V_{RS}, the voltage across the sense resistor, should not exceed 1.5V.

Voltage Overdrive

In many applications, maximum speed or step rate is a desirable performance characteristic. Maximium step rate is a direct function of the time necessary to reverse winding current with each step. In response to a constant motor supply voltage, the winding current changes exponentially with time, whose shape is determined by the winding time constant and expressed as:

$$I_m = V_m/R\ [1\text{-}EXP(-RT/L)]$$

as presented in Figure 9. With rated voltage applied, the time required to reach rated current is excessive when compared with the time required with over-voltage applied, even though the time constant L/R remains constant. With over-voltage however, the final value of current is excessive and must be prevented. This is accomplished with switch drive by repetitively switching the sink drivers on and off, so as to maintain an average value of current equal to the rated value. This results in a small amount of ripple in the controlled current, but the increase in step rate and performance may be considerable.

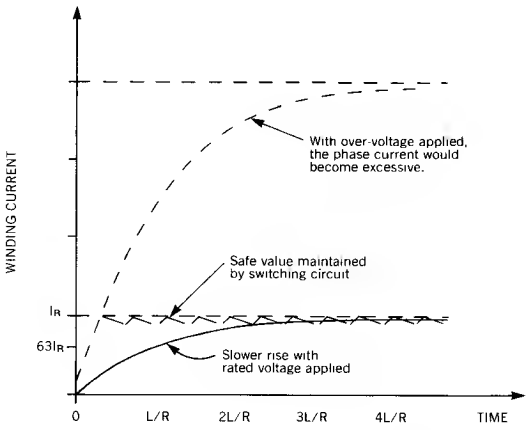


Figure 9. With rated voltage applied, winding current does not exceed rated value, but takes L/R seconds to reach 63% of its final value—probably too long. Increased performance requires an increase in applied voltage, or overdrive, and therefore a means to limit current. The UC3717A motor driver performs this task efficiently.

Interference

Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Half-Stepping

In half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90°. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

MOUNTING INSTRUCTIONS

The $R_{thj\text{-}amb}$ of the UC3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

The diagram of Figure 11 shows the maximum package power P_{tot} and the θ_{ja} as a function of the side " ℓ " of two equal square copper areas having a thickness of 35μ (see Figure 10).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

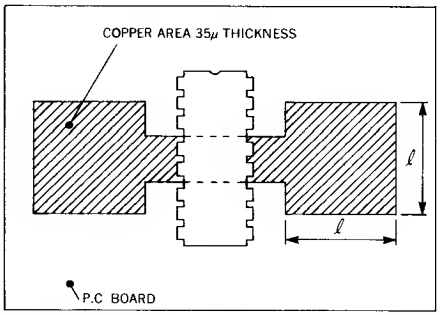


Figure 10. Example of P.C. Board Copper Area which is used as Heatsink

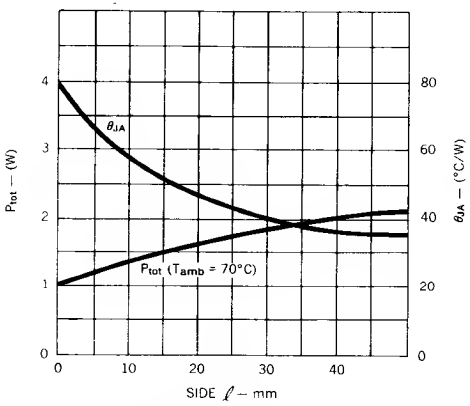


Figure 11. Maximum Package Power and Junction to Ambient Thermal Resistance vs Side " ℓ "

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 12. The input can be controlled by a microprocessor, TTL, LS, or CMOS logic.

The timing diagram in Figure 13 shows the required signal input for a two phase, full step stepping sequence. Figure 14 shows the requred input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 15 provides the signal shown in Figure 13, and in conjunction with the circuit shown in Figure 12 will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 16 shows a pulse to half step circuit generating the signal shown in Figure 14. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at high step rates.

Ordering Information
UNITRODE TYPE NUMBER
UC3717ANE — 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC3717AJ — 16 Pin Dual-in-line Ceramic Package

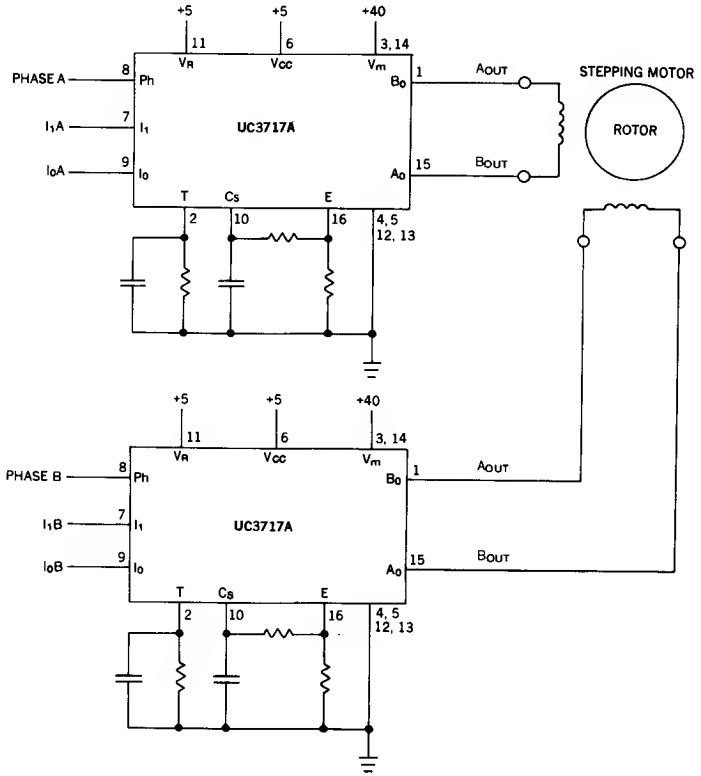


Figure 12. Typical Chopper Drive for a Two Phase Permanent Magnet Motor

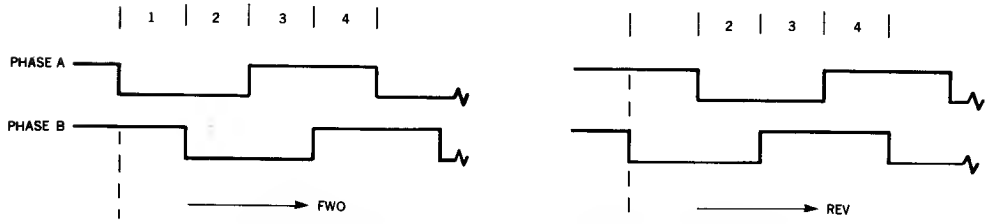


Figure 13. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

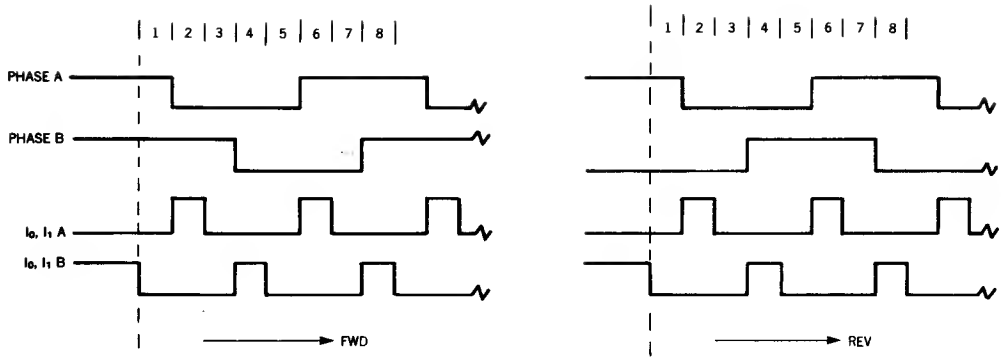


Figure 14. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

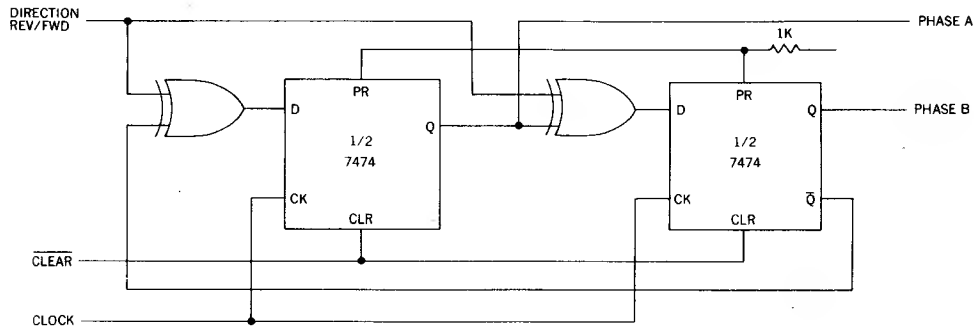


Figure 15. Full Step, Bidirectional Two Phase Drive Logic

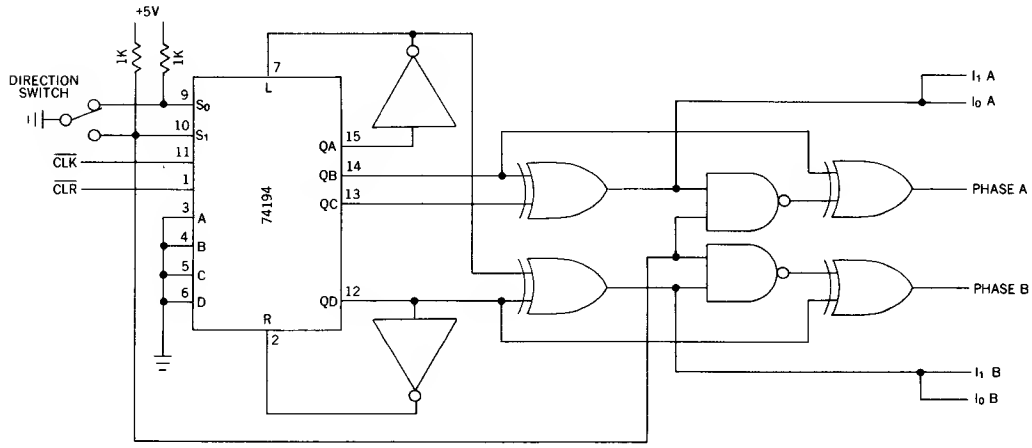


Figure 16. Half Step, Bidirectional Drive Logic

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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

UC3770A
UC3770B

High Performance Stepper Motor Drive Circuit

PRELIMINARY

FEATURES

- Full-Step, Half-Step and Micro-Step Capability.
- Bipolar Output Current up to 2A.
- Wide Range of Motor Supply Voltage: 10–50V
- Low Saturation Voltage
- Wide Range of Current Control: 5mA–2A.
- Current Levels Selected in Steps or Varied Continuously.
- Thermal Protection and Soft Intervention.

DESCRIPTION

The UC3770A and UC3770B are high-performance full bridge drivers that offer higher current and lower saturation voltage than the UC3717 and the UC3770. Included in these devices are LS-TTL compatible logic inputs, current sense, monostable, thermal shutdown, and a power H-bridge output stage. Two UC3770As or UC3770Bs and a few external components form a complete microprocessor-controllable stepper motor power system.

Unlike the UC3717, the UC3770A and the UC3770B require external high-side clamp diodes. The UC3770A and UC3770B are identical in all regards except for the current sense thresholds. Thresholds for the UC3770A are identical to those of the older UC3717 permitting drop-in replacement in applications where high-side diodes are not required. Thresholds for the UC3770B are tailored for half stepping applications where 50%, 71%, and 100% current levels are desirable.

The UC3770A and UC3770B are specified for operation from 0°C to 70°C ambient.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Logic Supply Voltage, V_{CC} 7V
Output Supply Voltage, V_{MM} 50V
Logic Input Voltage (Pins 7, 8, 9) 6V
Analog Input Voltage (Pin 10) . . . . . .V_{CC}
Reference Input Voltage (Pin 11) 15V
Logic Input Current (Pins 7, 8, 9) . . . . . -10mA
Analog Input Current (Pins 10, 11) . . . . . -10mA
Output Current (Pins 1, 15) . . . . . ±2A
Junction Temperature, Tj . . . . . +150°C

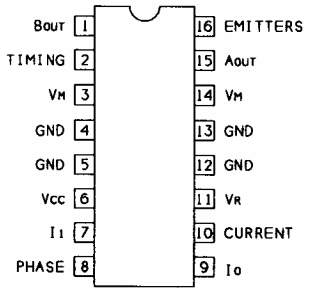
NOTE 1: All voltages are with respect to GND (Pins 4, 5, 12, 13)
Currents are positive into and negative out of the specified terminal.

THERMAL CHARACTERISTICS

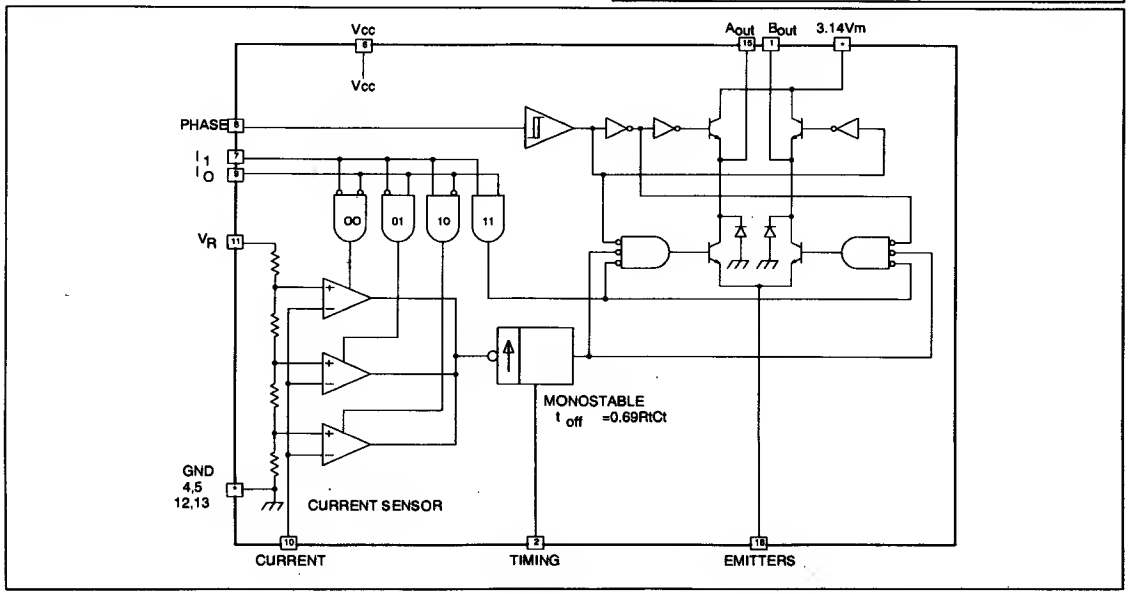
Thermal Resistance, Junction to Ground Pins (N Package) . .11°C/W
Thermal Resistance, Junction to Case, (J Package) . . . . .30°C/W

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(All tests apply with V_M=36V, V_{CC}=5V, V_R=5V, No Load, and 0°C<T_A<70°C, unless otherwise stated.) $T_A=T_j$

		UC3770A			UC3770B			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Supply Voltage V_M (Pins 3, 14)		10		45	10		45	V
Logic Supply Voltage V_{CC} (Pin 6)		4.75	5	5.3	4.75	5	5.3	V
Logic Supply Current I_{CC} (Pin 6)	I_O=I_1=H,I_M=0		15	25		15	25	mA
Logic Supply Current I_{CC} (Pin 6)	I_O=I_1=L,I_M=0		18	28		18	28	mA
Logic Supply Current I_{CC} (Pin 6)	I_O=I_1=H,I_M=1.3A		33	40		33	40	mA
Thermal Shutdown Temperature			+170			+170		°C
Logic Threshold (Pins 7, 8, 9)		0.8		2.0	0.8		2.0	V
Input Current Low (Pin 8)	V_i=0.4V			-100			-100	µA
Input Current Low (Pins 7, 9)	V_i=0.4V			-400			-400	µA
Input Current High (Pins 7, 8, 9)	V_i=2.4V			10			10	µA
Comparator Threshold (Pin 10)	V_R=5V, i_O=L, I_1=L	400	415	430	400	415	430	mV
Comparator Threshold (Pin 10)	V_R=5V, i_O=H, I_1=L	240	255	265	290	300	315	mV
Comparator Threshold (Pin 10)	V_R=5V, i_O=L, I_1=H	70	80	90	195	210	225	mV
Comparator Input Current (Pin 10)				±20			±20	µA
Off Time	R_T=56K, C_T=820pF	25	30	35	25	30	35	ms
Turn Off Delay				2			2	ms
Sink Driver Saturation Voltage	I_M=1.0A			0.8			0.8	V
Sink Driver Saturation Voltage	I_M=1.3A			1.3			1.3	V
Source Driver Saturation Voltage	I_M=1.0A			1.3			1.3	V
Source Driver Saturation Voltage	I_M=1.3A			1.6			1.6	V
Output Leakage Current	V_M=45V			100			100	µA

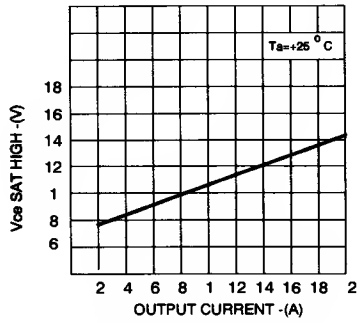


Figure 1. Typical Source Saturation Voltagee vs. Load Current

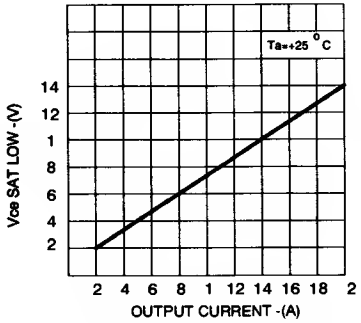


Figure 2. Typical Sink Saturation Voltages vs. Load Current

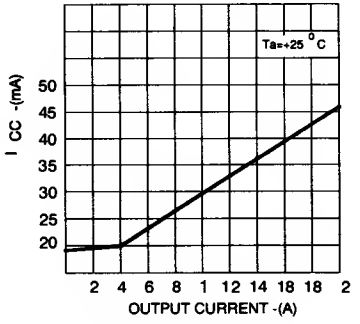


Figure 3. Typical Supply Current vs. Load Current

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POWER DRIVER & INTERFACE CIRCUITS

6

POWER DRIVERS SWITCHES AND INTERFACE

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
L295	Dual Solenoid Driver with Current Control	• High Current Capability (Up to 2.5A per channel) • High Voltage Operation (Up to 46V for Power Stage) • High Efficiency Switchmode Operation • Regulated Output Current (Adjustable) • Few External Components • Separate Logic Supply • Thermal Protection	15 Pin Power Tab
UC195/295/395	Smart Power Switch	These devices act as high gain power transistors and have on-chip, current limiting, power limiiting, and thermal overload protection. • Greater than 1.0A Ouput • 3.0μ Typical Base Current (Adjustable) • 500ns Switching Time • 2.0V Saturation Voltage • Direclty Interfaces with CMOS or TTL • Internal Thermal Limiting	TO-5 TO-220
UC1710/3710	High Current/Speed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8 Pin DIL 5 Pin TO-220
UC1728/3728	PWM Dual Driver	Load Control and Status monitoring for two inductive loads up to 1A each. • PWM Current Control • Dual, Floating Switches • Supply Voltage up to 60V • Tri-State Status Outputs • 60V Operation	28 Pin DIL 28 PLCC
UC2950	Half-Bridge Bipolar Switch	• Source or Sink 4.0A • Supply Voltage to 35V • High-Current Output Diodes • Tri-State Operation • TTL and CMOS Input Compatability • Thermal Shutdown Protection • 300KHz Operation	5 Pin TO-220
UC3657	Triple Half-Bridge Power Driver	• Three 2A Drivers • On Board Clamp Diodes	15 Pin Power Tab
UC3720	Smart Switch	Independent high and low side switching, up to 2.5A capability • Full Protection • Over-and Under-Current Fault Indication • 50V Operation	15 Pin Power Tab
UC3722	Five Channel Programmable Current Switch	• Five Current-Sinking Switches • Programmable Currents from .5 to 2.5A • Internal Current Sensing • 40V Operation • Protection Features	15 Pin Power Tab
UC3724 UC3725 (Pair)	Isolated HIgh Side Drive for N-Channel Power MOSFET Gates.	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600KHz Carrier Capability • Local Current Limiting Feature	8 Pin DIL (Pair)

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5Pin TO-220
UC1706/3706	Dual High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion (1706 Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible	16 Pin DIL "Batwing"
UC1707/3707	Dual Uncommitted High Current MOSFET Compatible Output Driver	• Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25nSec Rise and Fall Times • 25 nSec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8-Pin DIL 16-Pin DIL
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8 Pin DIL
UC1710/3710	HIgh Current/Speed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8 Pin DIL 5 Pin TO-220
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 15nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8-Pin DIL

POWER DRIVER, SWITCHES & INTERFACE CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC3724 UC3725 (PAIR)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600kHz Carrier Capability • Local Current Limiting Feature	8 Pin DIL (Pair)
UC5170C	Octal-Single Ended Line Driver	Suited for data transmission systems • Eight Driver in One Package • Meets EIA standards • Single External Resistor Controls Slew Rate • Tri-State Outputs • Low Power Consumption • TTL Compatible	28 Pin DIL 28 PLCC
UC5180C	Octal Line Receiver	Suited for digtital communication requirements. • Eight Receivers in One Package • Meets EIA Standards • Single 5V Supply • Differential Inputs Withstand ±25V • Low Noise Filter	28 Pin DIL 28 PLCC

INTEGRATED CIRCUITS

UNITROODE

Dual Switchmode Solenoid Driver

FEATURES

- High current capability (up to 2.5A per channel)
- High voltage operation (up to 46V for power stage)
- High efficiency switchmode operation
- Regulated output current (adjustable)
- Few external components
- Separate logic supply
- Thermal protection

DESCRIPTION

The L295 is a monolithic integrated circuit in a 15 lead MULTIWATT® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels and drive 2 independent solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and separate power supply inputs for bilevel operation such as interfacing with peripherals running at higher voltage levels.

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.

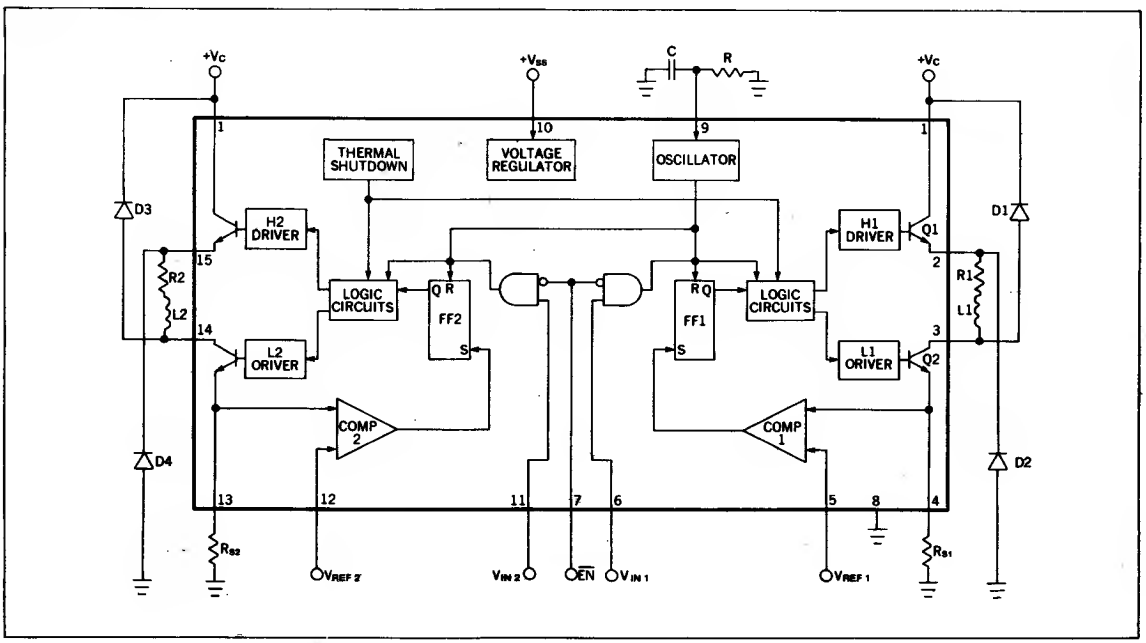
ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_C 50V
Logic Supply Voltage, V_{SS} 12V
Enable and Input Voltage, V_{EN}, V_I 7V
Reference Voltage, V_{REF} 7V
Peak Output Current (each channel)
Non-Repetitive, (t = 100μsec), I_O 3A
Repetitive (80% on −20% off; t_{ON} = 10ms) 2.5A
DC Operation 2A
Total Power Dissipation (at T_{case} = 75°C) 25W
Storage and Junction Temperature ..... −40 to +150°C

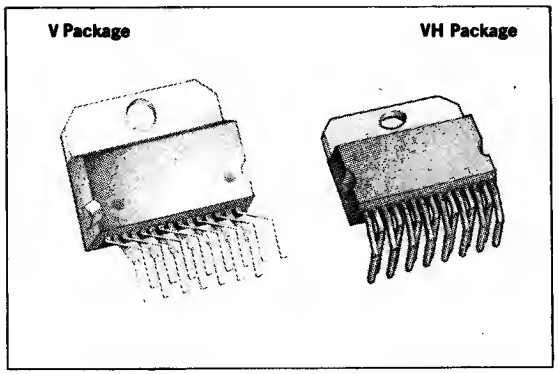
THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max
Thermal Resistance Junction-Ambient, θ_{JA} ..... 35°C/W max

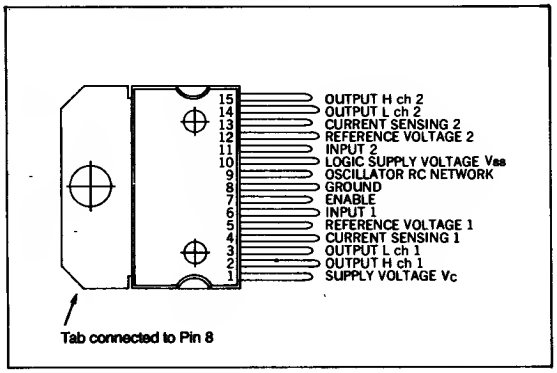
BLOCK DIAGRAM



MECHANICAL DATA



CONNECTION DIAGRAM (TOP VIEW)



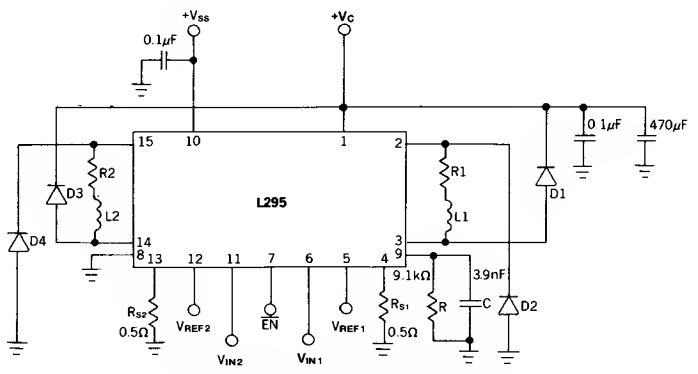
ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{SS} = 5V, V_C = 36V, T_j = 25°C; unless otherwise specified, L = Low; H = High) T_A=T_J

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_C		12		46	V
Logic Supply Voltage	V_{SS}		4.75		10	V
Quiescent Drain Current (from V_C)	I_C	V_C = 46V; V_{I1} = V_{I2} = V_{EN} = L			4	mA
Quiescent Drain Current (from V_{SS})	I_{SS}	V_{SS} = 10V			46	mA
Low Input Voltage	$V_{I1}L$, $V_{I2}L$		-0.3		0.8	V
High Input Voltage	$V_{I1}H$, $V_{I2}H$		2.2		7	V
Low Enable Input Voltage	$V_{EN}L$		-0.3		0.8	V
High Enable Input Voltage	$V_{EN}H$		2.2		7	V
Input Current	I_{I1}, I_{I2}	V_{I1} = V_{I2} = L			-100	μA
		V_{I1} = V_{I2} = H			10	
Enable Input Current	I_{EN}	V_{EN} = L			-100	μA
		V_{EN} = H			10	
Input Reference Voltage	V_{REF1}, V_{REF2}		0.2		2	V
Input Reference Current	I_{REF1}, I_{REF2}				-5	μA
Oscillation Frequency	f_{osc}	C = 3.9nF, R = 9.1KΩ		25		KHz
Transconductance (each channel)	$\frac{I_p}{V_{REF}}$	V_{REF} = 1V, R_s = 0.5Ω	1.9	2	2.1	A/V
Total Output Voltage Saturation (each channel)*	V_{sat}	I_o = 2A		2.8	3.6	V
External Sensing Resistors Voltage Drop	$V_{sens\ 1}$, $V_{sens\ 2}$				2	V

*V_{sat} = $V_{CEsatQ1}$ + $V_{CEsatQ2}$.

6

APPLICATION CIRCUIT



D1, D4 = 2A HIGH SPEED DIODES (SES5001, or equivalent)

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are;

$\overline{EN}$ chip enable (digital input, active low), enables both channels when in the low state.

V_{IN1}, V_{IN2} channel inputs (digital inputs, active high), enable each channel independently. A channel is activated when both $\overline{EN}$ and the appropriate channel input are active.

V_{REF1}, V_{REF2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{REF}.

Since the two channels are identical, only channel one will be described. The following description applies equally to channel two, replacing FF2 for FF1, V_{REF2} for V_{REF1} etc. When the channel is activated by a low level on the $\overline{EN}$ input and a high level on the channel input V_{IN1}, the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law:

$$I = \frac{V}{R1}\left(1 - e^{\frac{-R1t}{L1}}\right)$$

where: R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{REF1}. This peak current, I_{p1}, is given by:

$$I_{p1} = \frac{V_{REF1}}{R_{S1}}$$

At this point the comparator output, Comp 1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{P1}\right)e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where: $V_A = V_{CEsat\ Q2} + V_{sense\ 1} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in Figure 1.

At time t_2, channel 1 is disabled by taking the inputs V_{IN1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{T2}\right)e^{\frac{-R1t}{L1}} - \frac{V_B}{R1}$$

where: $V_B = V_C + V_{D1} + V_{D2}$
I_{T2} = current value at the time t_2.

Figure 2 shows the current waveform obtained with an RC network connected between pin 9 and ground. From t_0 to t_1 the current increases as in Figure 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{s1} is equal to V_{REF1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in Figure 4 and must be chosen in the range 10 to 30KHz.

It is possible with external hardware to change the reference voltage V_{REF} in order to obtain a high peak current I_p and a lower holding current I_h (see Figure 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{REF1}, V_{REF2}) can be left open or connected to V_{ss}; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_s:

$$I_p = \frac{2.5}{R_s}$$

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SIGNAL WAVEFORMS

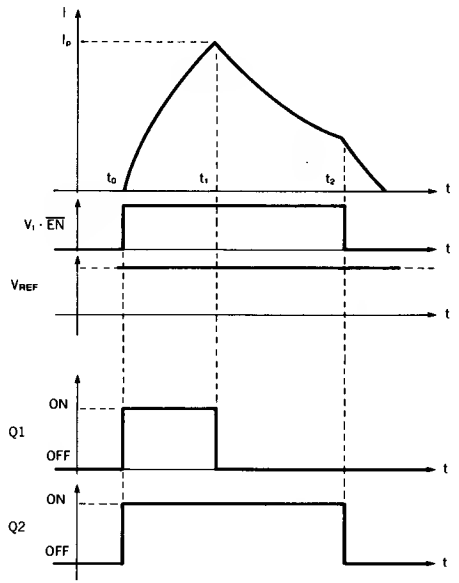


Figure 1. Load current waveform with pin 9 connected to GND

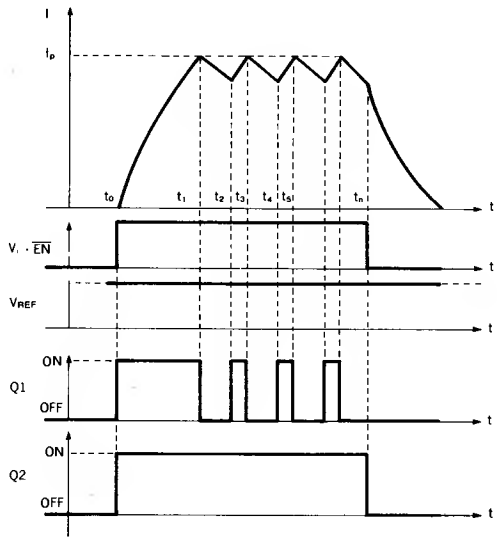


Figure 2. Load current waveform with external R-C network connected between pin 9 and ground

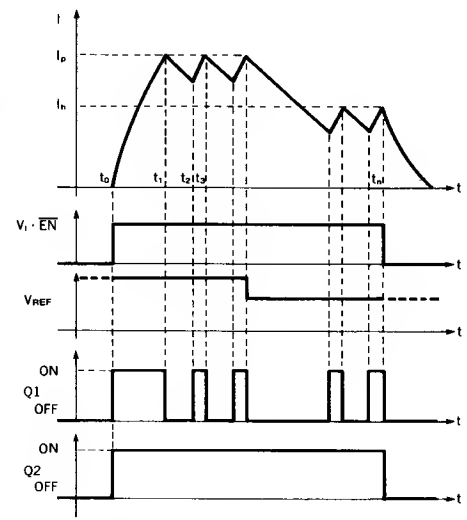


Figure 3. With V_{REF} changed by hardware

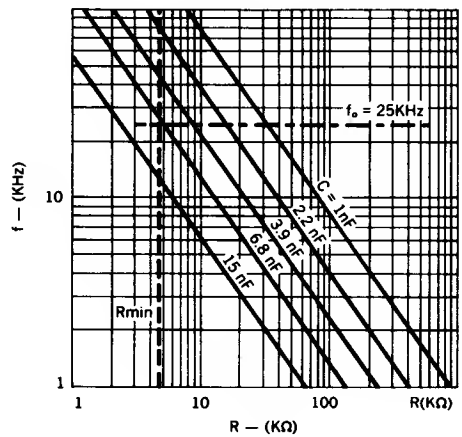


Figure 4. Switching frequency vs values of R and C

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

Smart Power Transistor

UC195
UC295
UC395

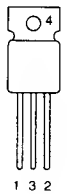
FEATURES
- Greater Than 1.0A Output
- 3.0μA Typical Base Current
- 500ns Switching Time
- 2.0V Saturation
- Directly Interfaces with CMOS or TTL
- Internal Thermal Limiting
- Available in TO-257 military package

DESCRIPTION

The UC195/UC395 family of devices are ultra reliable, fast, monolithic power transistors with complete overload protection. These devices act as high gain power transistors and have on chip, current limiting, power limiting, and thermal overload protection, making them virtually impossible to destroy. The UC195/UC395 offers a significant increase in reliability and simplifies power circuitry designs.

The UC195/UC395 are available in standard TO-3 power packages and solid Kovar TO-5. The UC195 is rated for operation from −55°C to +150°C, the UC295 is rated from −25°C to +125°C, and the UC395 is rated from 0°C to +125°C.

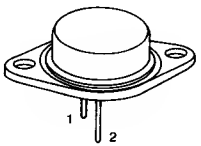
G, IG (TO-257)



Non-isolated
Pin 1. Adjust
2. Input
3. Output
4. Output

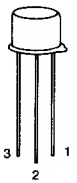
Isolated
Pin 1. Adjust
2. Input
3. Output
4. No Connection

TO-3 (K)



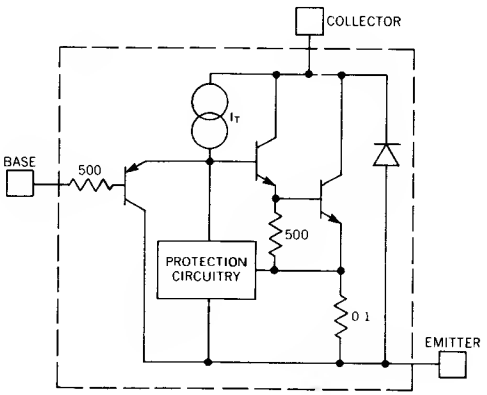
Pin 1. Input
2. Output
Case: Ground

TO-5 (H)



Pin 1. Emitter
2. Base
3. Collector
Case: Emitter

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Collector to Emitter Voltage
- UC195, UC295 ..... 42V
- UC395 ..... 36V

Collector to Base Voltage
- UC195, UC295 ..... 42V
- UC395 ..... 36V

Base to Emitter Voltage (Forward)
- UC195, UC295 ..... 42V
- UC395 ..... 36V

Base to Emitter Voltage (Reverse) 20V
Collector Current ..... Internally Limited
Power Dissipation ..... Internally Limited
Operation Temperature Range
- UC195 ..... −55°C to +150°C
- UC295 ..... −25°C to +125°C
- UC395 ..... 0°C to +125°C

Storage Temperature Range ..... −65°C to +150°C
Lead Soldering Temperature (10 seconds) ..... 300°C

THERMAL DATA

TO-3 ..... θ_{ja} = 35°C/W
TO-5 ..... θ_{ja} = 150°C/W
TO-257 ..... θ_{ja} = 42°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise specified these specifications apply for −55°C ≤ T_j ≤ +125°C for the UC195, −25°C ≤ T_j ≤ +125°C for the UC295, and 0°C ≤ T_j ≤ +125°C for the UC395.) T_A=T_J

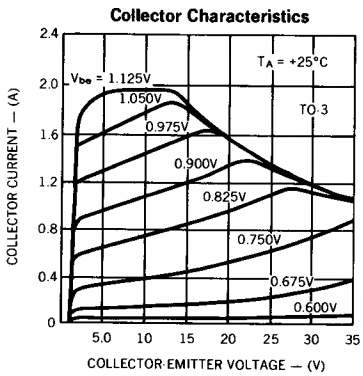
PARAMETERS	SYMBOL	CONDITIONS	UC195, UC295			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Operating Voltage	V_{ce}	$I_q \le I_c \le I_{c\,max}$			42	V
Base to Emitter Breakdown Voltage	BV_{be}	$0 \le V_{ce} \le V_{ce\,max}$	42			V
Collector Current TO-3, TO-5, TO-257	I_c	$V_{ce} \le 15V$ $V_{ce} \le 7.0V$	1.2 1.2	2.2 1.8		A A
Saturation Voltage	V_{sat}	$I_c \le 1.0A$, T_A = 25°C		1.8	2.0	V
Base Current	I_b	V_{be} = 0V, V_{ce} = 42V	−50			μA
		V_{be} = 42V, V_{ce} = 0V			5	μA
Quiescent Current	I_q	V_{be} = 0V $0 \le V_{ce} \le V_{ce\,max}$		2.0	5.0	mA
Base-Emitter Voltage	V_{be}	I_c = 1.0A, T_A = 25°C		0.9		V
Switching Time	t_s	V_{ce} = 36V, R_L = 36Ω T_A = 25°C		500		ns
Thermal Resistance Junction to Case	θ_{jc}	TO-3 Package TO-5 Package TO-257 Package Isolated TO-257 Package		2.3 12 2.5 3.0	3.0 15 3.5 4.2	°C/W °C/W °C/W °C/W

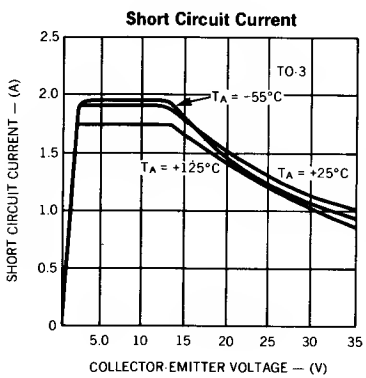
6

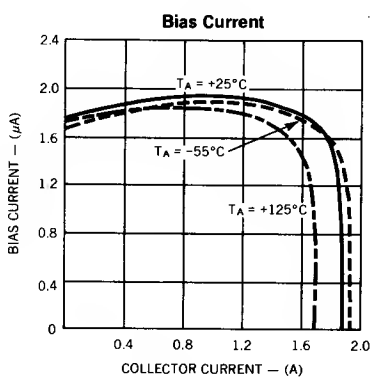
ELECTRICAL CHARACTERISTICS (Unless otherwise specified these specifications apply for $-55°C \leq T_j \leq +125°C$ for the UC195, $-25°C \leq T_j \leq +125°C$ for the UC295, and $0°C \leq T_j \leq +125°C$ for the UC395.) $T_A = T_J$

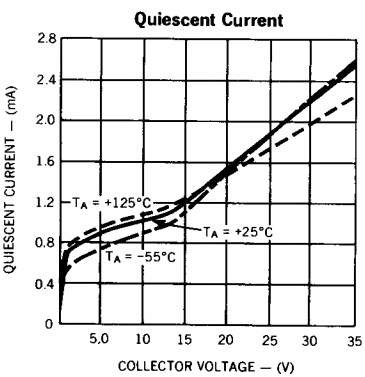
PARAMETERS	SYMBOL	CONDITIONS	UC395			UNITS
			MIN.	TYP.	MAX.	
Collector-Emitter Operating Voltage	V_{ce}	$I_q \leq I_c \leq I_{c\,max}$			36	V
Base to Emitter Breakdown Voltage	BV_{be}	$0 \leq V_{ce} \leq V_{ce\,max}$	36	60		V
Collector Current TO-3, TO-5, TO-257	I_c	$V_{ce} \leq 15V$ $V_{ce} \leq 7.0V$	1.0 1.0	2.2 1.8		A A
Saturation Voltage	V_{sat}	$I_c \leq 1.0A$, $T_A = 25°C$		1.8	2.2	V
Base Current	I_b	$V_{be} = 0V$, $V_{ce} = 36V$	-50			μA
		$V_{be} = 36V$, $V_{ce} = 0V$			10	μA
Quiescent Current	I_q	$V_{be} = 0V$ $0 \leq V_{ce} \leq V_{ce\,max}$		2.0	10.0	mA
Base-Emitter Voltage	V_{be}	$I_c = 1.0A$, $T_A = 25°C$		0.9		V
Switching Time	t_s	$V_{ce} = 36V$, $R_L = 36\Omega$ $T_A = 25°C$		500		ns
Thermal Resistance Junction to Case	θ_{jc}	TO-3 Package TO-5 Package TO-257 Package Isolated TO-257 Package		2.3 12 2.5 3.0	3.0 15 3.5 4.2	°C/W °C/W °C/W °C/W

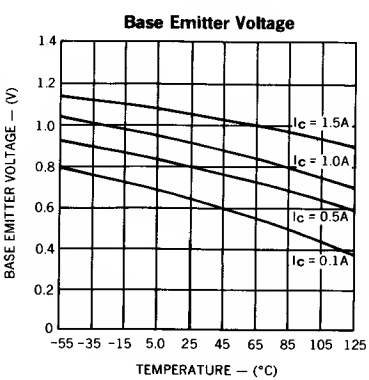
TYPICAL PERFORMANCE CHARACTERISTICS

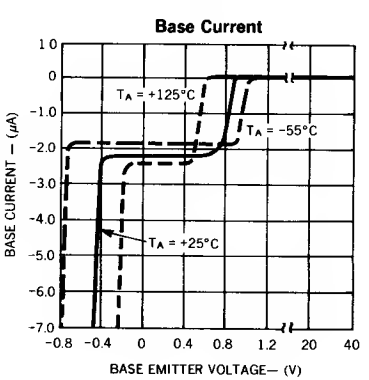




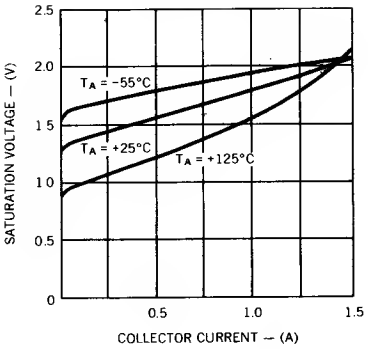




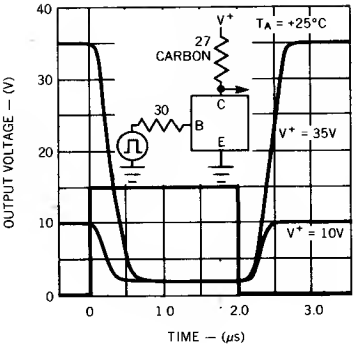




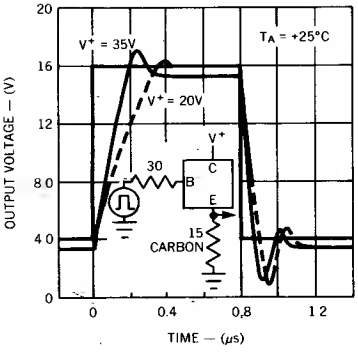
Saturation Voltage



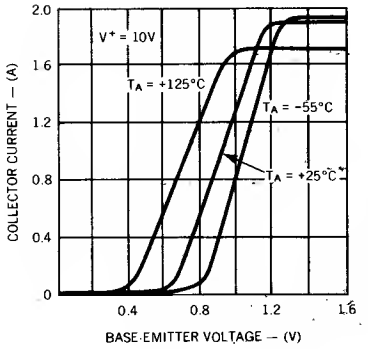
Response Time



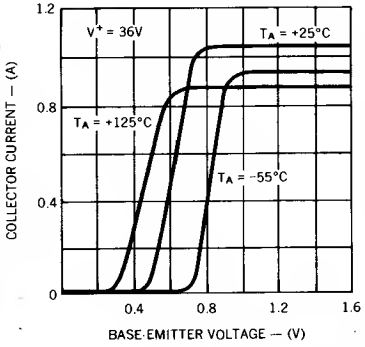
Response Time



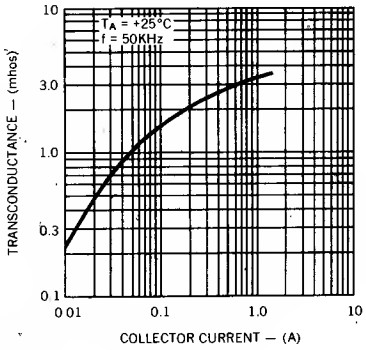
10V Transfer Function



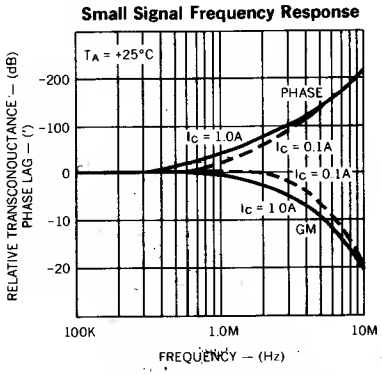
36V Transfer Function



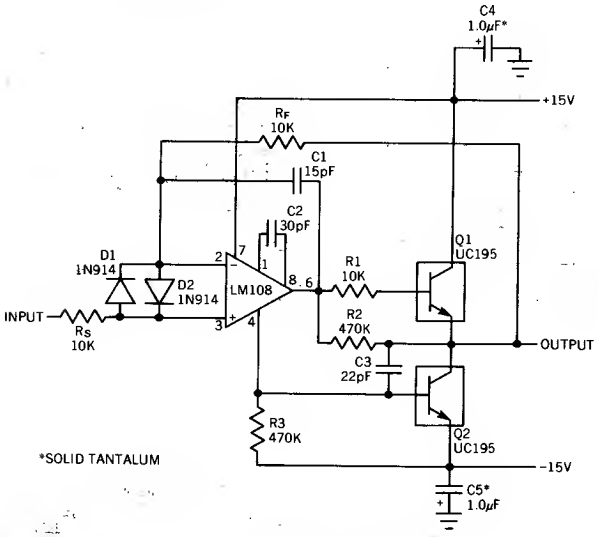
Transconductance



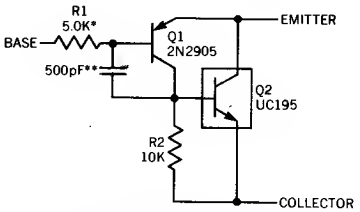
Small Signal Frequency Response



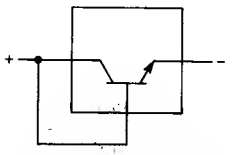
TYPICAL APPLICATIONS



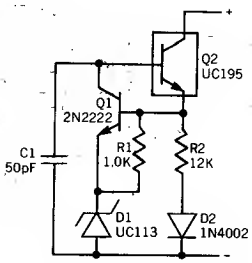
1.0A Voltage Follower



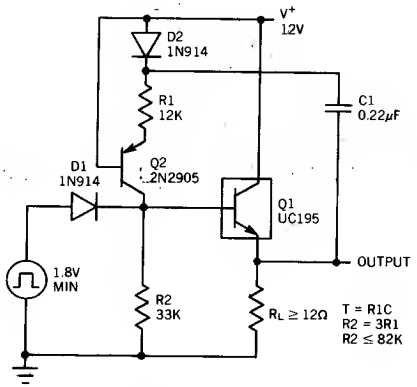
Power PNP



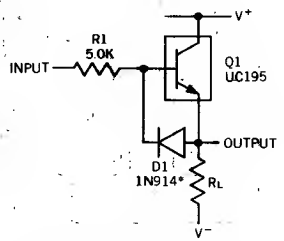
Two Terminal Current Limiter



Two Terminal 100mA Current Regulator



Power One-Shot



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INTEGRATED CIRCUITS
UNITRODE

High Speed Power Driver

UC1705
UC3705

FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices — particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both V_S and V_C can independently range from 5V to 40V. In the MINIDIP package, V_S can also be used to gate the output as when V_S is less than 4V, the output is held in the high impedence state and no current is drawn from V_C.

For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for −55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

TRUTH TABLE

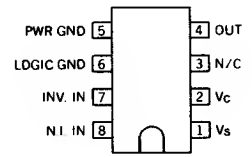
INV	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{INV}$ and N.I.

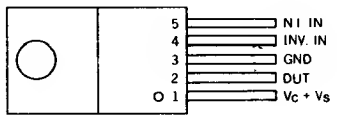
$\overline{OUT}$ = INV or $\overline{N.I.}$

CONNECTION DIAGRAMS

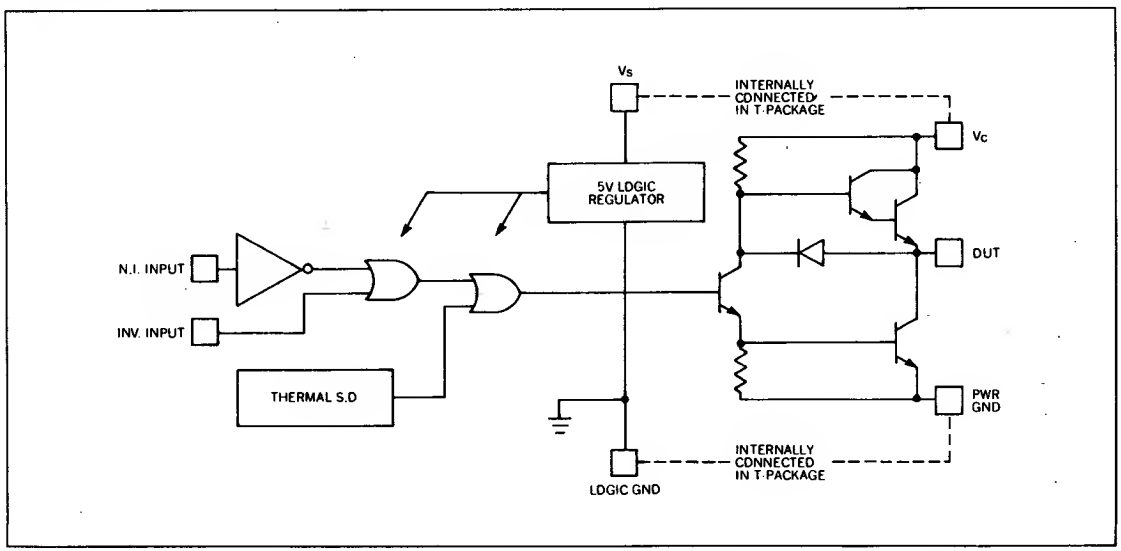
DIL-8 MINIDIP
N or J Package
Top View



5-Pin TO-220
T Package
Top View



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, V_C	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20μJ	15μJ	50μJ
Digital Inputs (see note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W	3W
Derate above 50°C	10mW/°C	10mW/°C	25mW/°C
Power Dissipation at T (Leads/Case) = 25°C	3W	2W	25W
Derate for Ground Lead Temperature above 25°C	25mW/°C	—	—
Derate for Case Temperature above 25°C	—	16mW/°C	200mW/°C
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Load Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

NOTE: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.

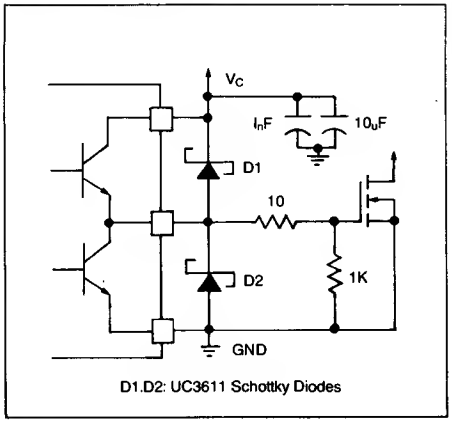
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1705 and 0°C to +70°C for the UC3705; V_S = V_C = 20V.) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_S Supply Current	V_S = 40V, (Outputs High; T Pkg.)		6	8	mA
V_S Supply Current	V_S = 40V (Outputs Low; T Pkg.)		8	12	mA
V_C Supply Current (N, J Only)	V_C = 40V, Outputs Low		2	4	mA
V_C Leakage Current (N, J Only)	V_S = 0, V_C = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		−0.6	−1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C−V_O	I_o = −50mA			2.0	V
Output High Sat., V_C−V_O	I_o = −500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS (V_S = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.)

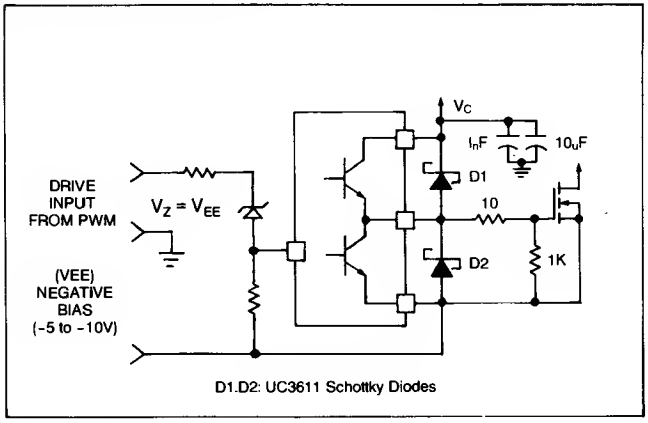
PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
		open	1.0	2.2	nF
From Inv. Input to Output:					
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns

Power MOSFET Drive Circuit



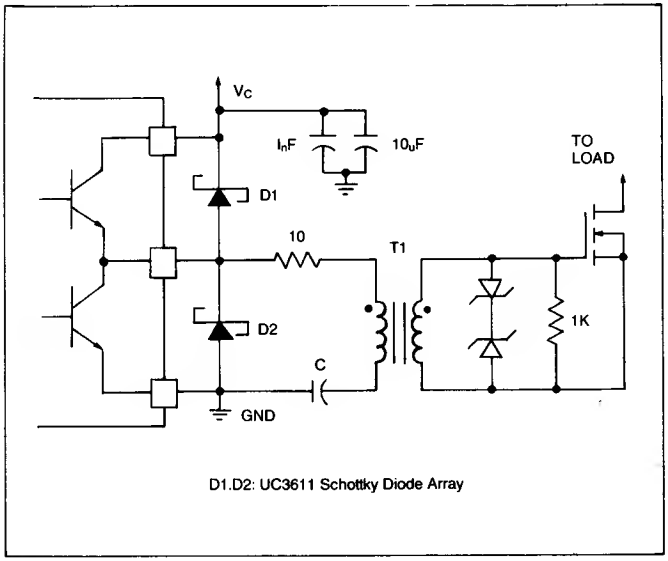
D1.D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS



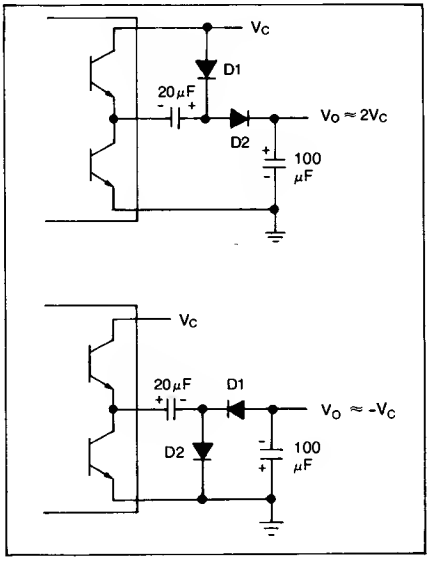
D1.D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Charge Pump Circuits



6

INTEGRATED CIRCUITS

UNITRODE

Dual Output Driver

UC1706
UC3706

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below:

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

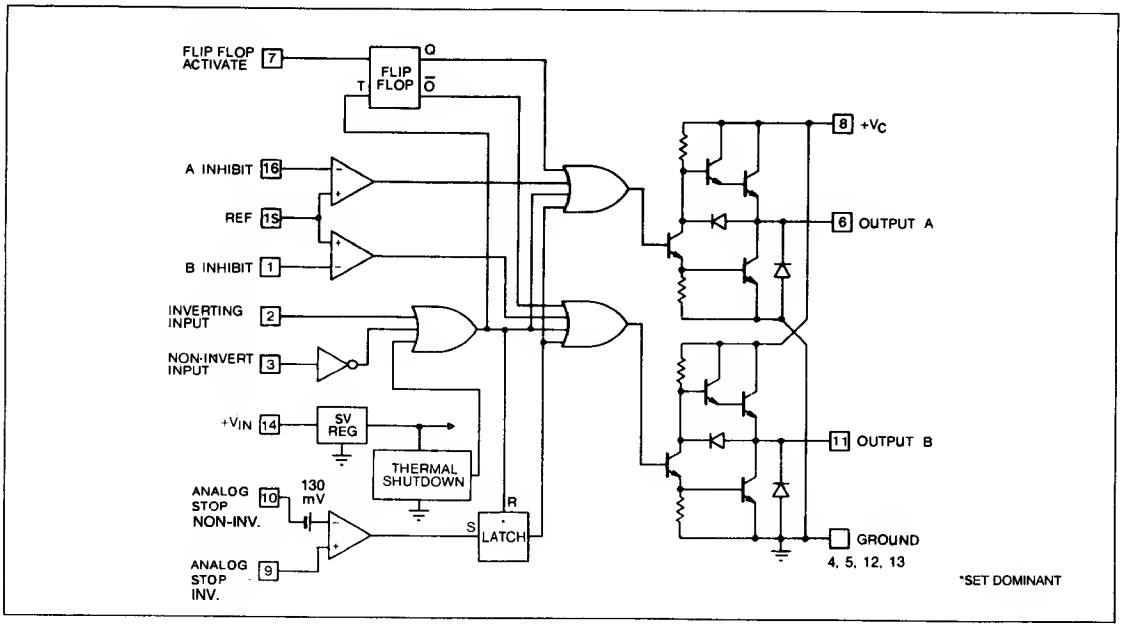
These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

TRUTH TABLE

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

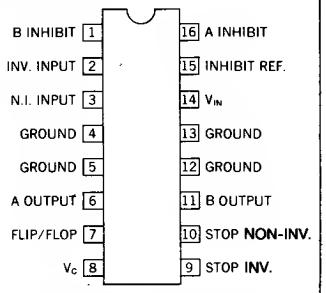
OUT = $\overline{\text{INV}}$ and N.I.
$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



Note: All four ground pins must be connected to a common ground.

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20μJ	15μJ
Digital Inputs	5.5V	5.5V
Inhibit Inputs	5.5V	5.5V
Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C	2W	1W
Derate above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (Leads/Case) = 25°C	5W	2W
Derate for Ground Lead Temperature above 25°C	40mW/°C	—
Derate for Case Temperature above 25°C	—	16mW/°C
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Load Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55° to +125°C for the UC1706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V.) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
V_C Supply Current	V_C = 40V, Outputs Low		4	5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_o = -50mA			2.0	V
Output High Sat., V_C-V_O	I_o = -500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
Inhibit Threshold	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		-10	-20	μA
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	μA
Thermal Shutdown			155		°C

6

TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured 50% in to 10% out.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L=			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V Stop Inv. = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION

Outputs
The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop
Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs
With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs — the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit
Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

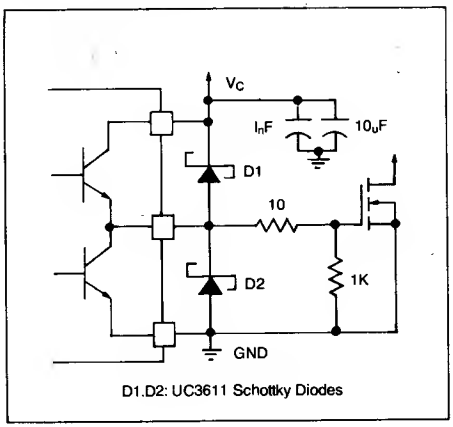
Analog Shutdown
This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} – 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

Supply Voltage
With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply V_{IN} to the UC1706. V_{IN} switching should be fast as if V_C is high, undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations
Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

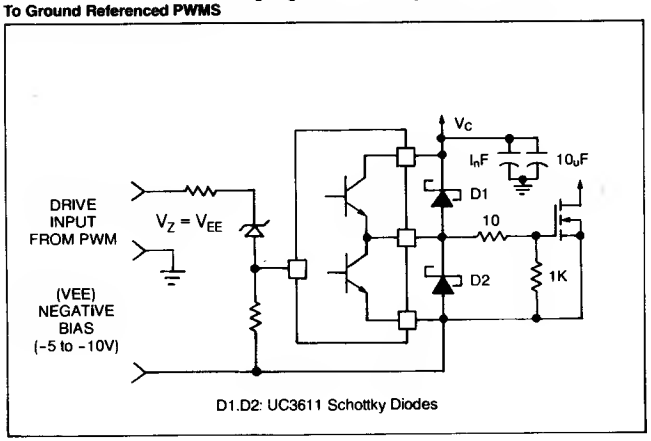
APPLICATIONS

Power MOSFET Drive Circuit



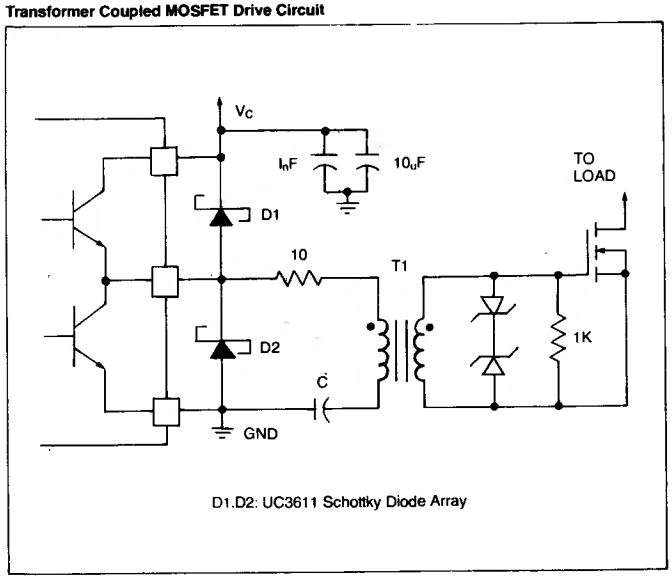
D1.D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voitage and Level Shifting To Ground Referenced PWMS



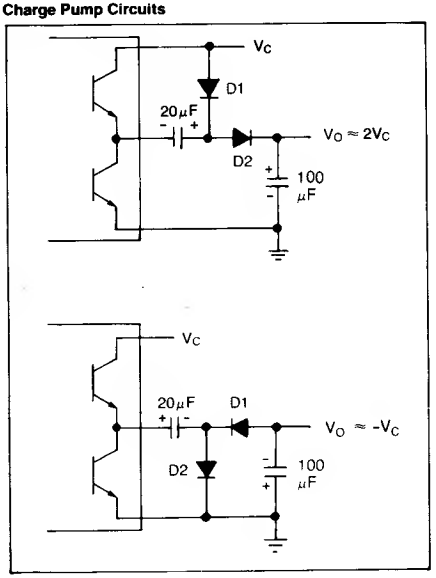
D1.D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Charge Pump Circuits



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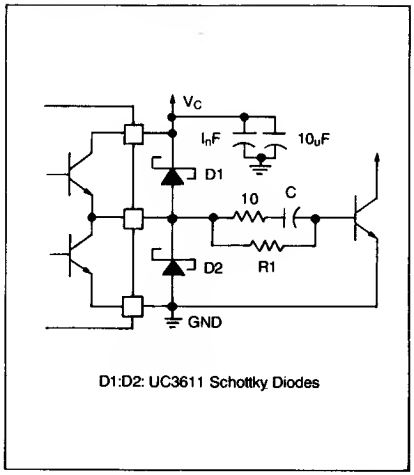
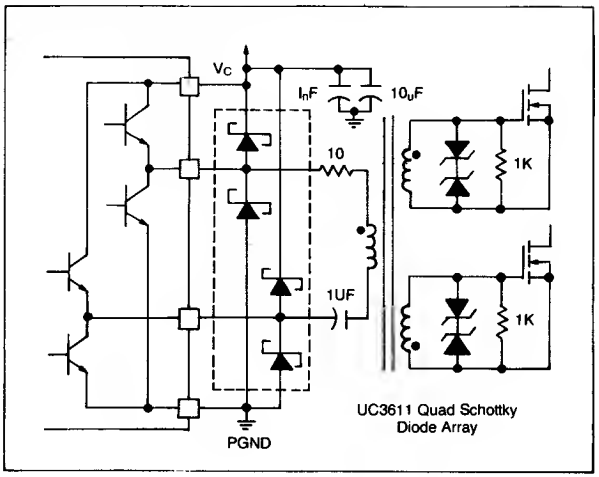
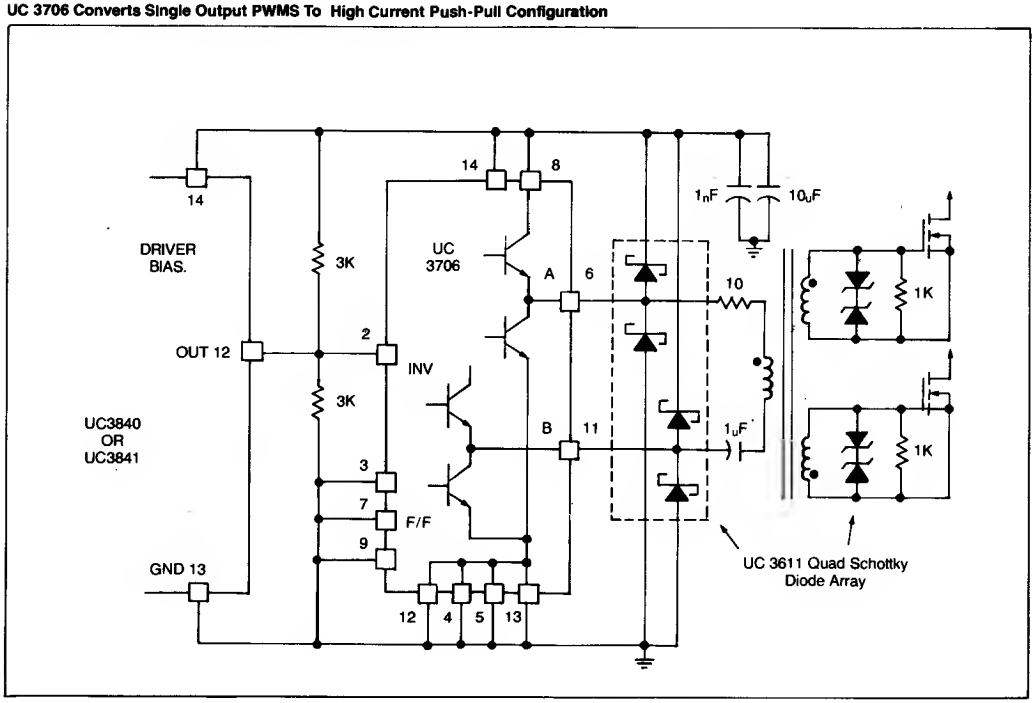
Power Bipolar Drive Circuit



Transformer Coupled Push-Pull MOSFET Drive Circuit



UC 3706 Converts Single Output PWMS To High Current Push-Pull Configuration



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INTEGRATED CIRCUITS

UNITRODE

Dual Channel Power Driver

UC1707
UC3707

FEATURES

- Two Independent Drivers
- 1.5A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40ns Rise and Fall into 1000pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown with Optional Latch
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

DESCRIPTION

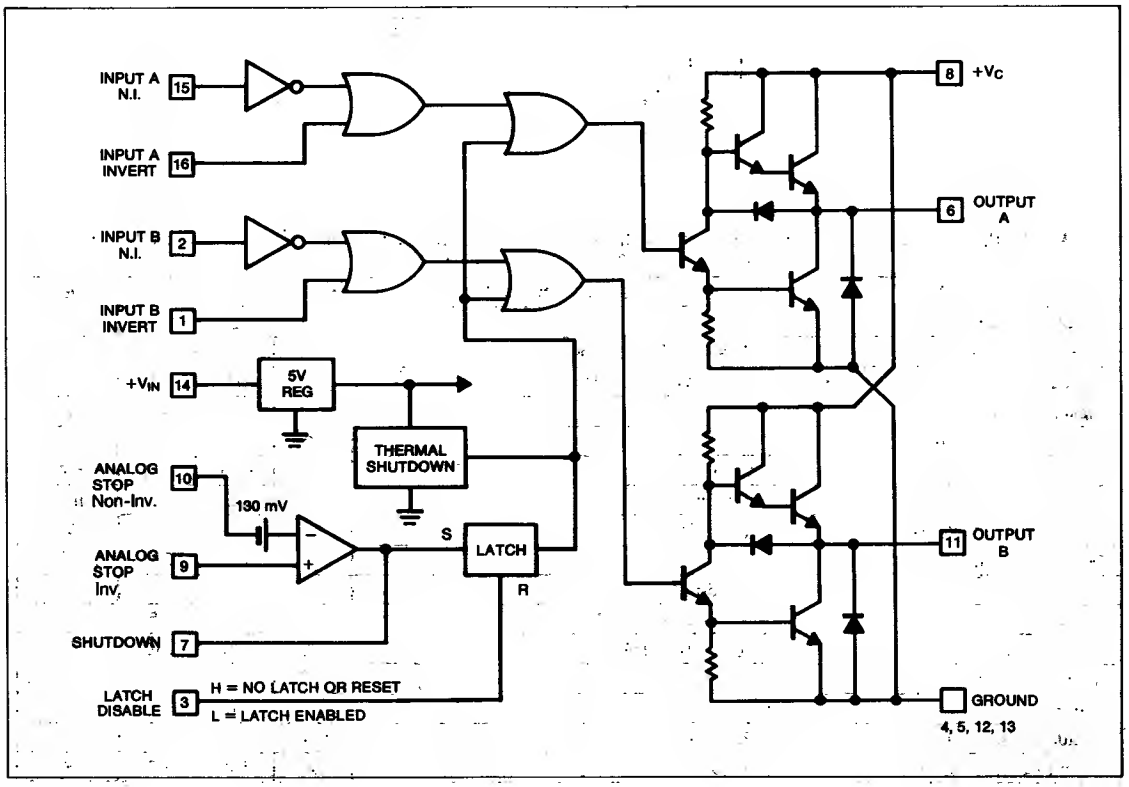
The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices — particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and V_C can independently range from 5V to 40V. V_{IN} can also be used to gate the outputs as when V_{IN} is less than 4V, both outputs are held in the high impedance state and no current is drawn from V_C.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q, L packages.

BLOCK DIAGRAM



6

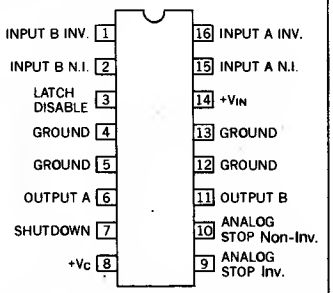
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20μJ	15μJ
Digital Inputs (see note)	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C	2W	1W
Derate above 50°C	20mW/°C	10mW/°C
Power Dissipation at T (Leads/Case) = 25°C	5W	2W
Derate for Ground Lead Temperature above 25°C	40mW/°C	—
Derate for Case Temperature above 25°C	—	16mW/°C
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Load Temperature (Soldering, 10 seconds)	300°C	

NOTE: All voltages are with respect to the four ground pins which must be conected together. All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J OR N PACKAGE



NOTE: All four ground pins must be connected to a common ground.

TRUTH TABLE (Each Channel)

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV.}}$ and N.I.

$\overline{\text{OUT}}$ = INV. or $\overline{\text{N.I.}}$

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V.) T_A=T_J

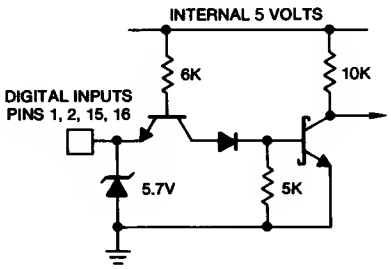
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{IN} Supply Current	V_{IN} = 40V		12	15	mA
V_C Supply Current	V_C = 40V, Outputs Low		5.2	7.5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_o = -50mA			2.0	V
Output High Sat., V_C-V_O	I_o = -500mA			2.5	V
Output Low Sat., V_O	I_o = 50mA			0.4	V
Output Low Sat., V_O	I_o = 500mA			2.5	V
Analog Threshold	V_{CM} = 0V to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	μA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		40	50	60	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		30	40	50	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output:					
Rise Time Delay		30	40	50	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		45	55	65	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V Stop Inv. = 0 to 0.5V	180			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

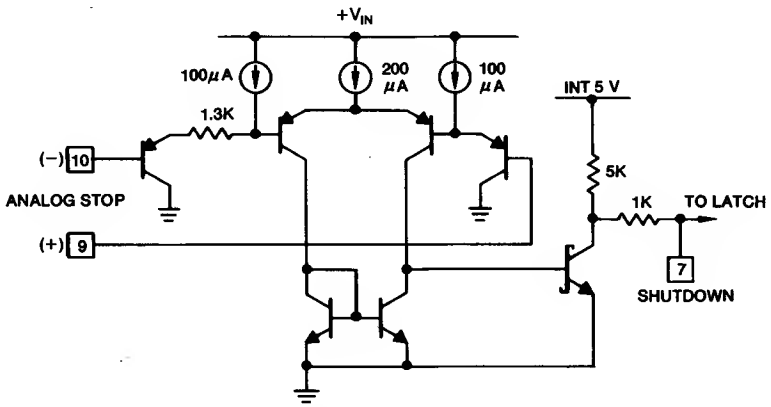
SIMPLIFIED INTERNAL CIRCUITRY

Typical Digital Input Gate



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

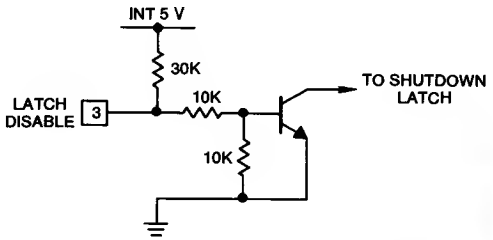
Analog Shutdown Comparator Circuit



The input common-mode voltage range is from ground to (V_{IN}−3V). When not used both inputs should be grounded. Activate time is a function of overdrive with a minimum value of 160ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

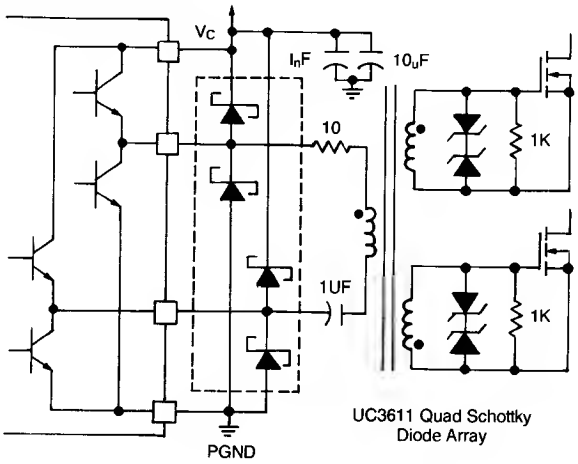
SIMPLIFIED INTERNAL CIRCUITRY (continued)

Latch Disable

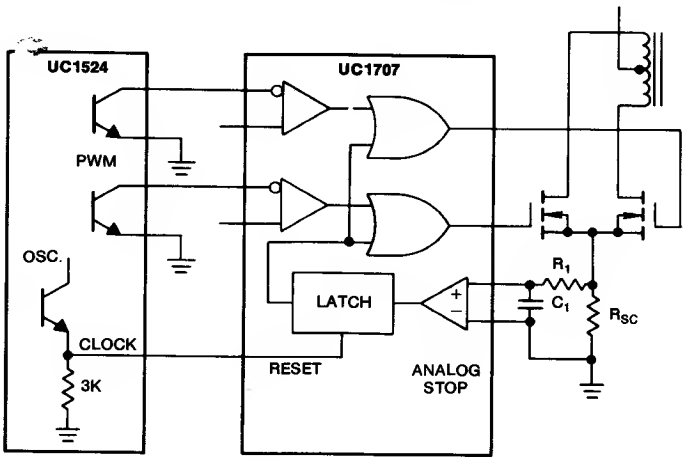


The Shutdown latch is disabled when pin 3 is open. An impedance of 4KΩ or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the V_{IN} supply or by momentarily (>200ns) raising pin 3 high.

Transformer Coupled Push-Pull MOSFET Drive Circuit



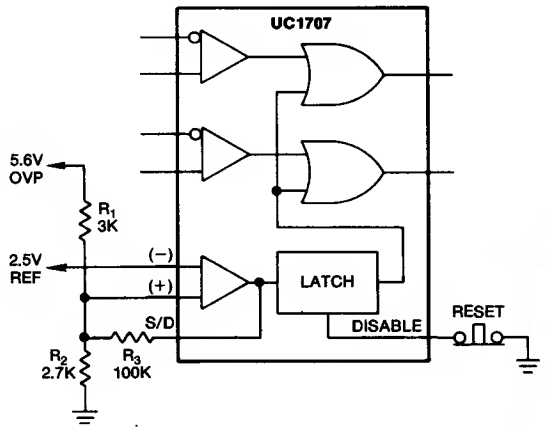
Current Limiting



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R_1C_1 is used to filter leading edge spikes.

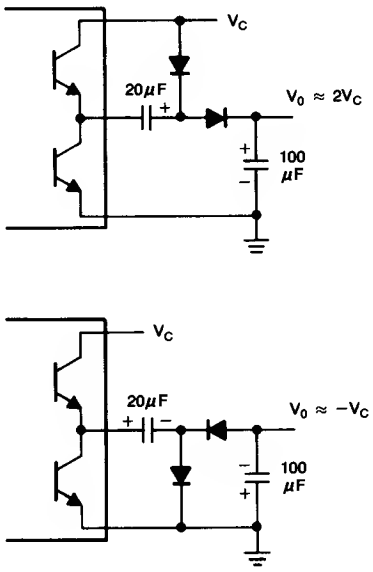
APPLICATIONS (continued)

Over-Voltage Protection



With an external reference, the shutdown comparator can be used for over-voltage protection. R_1 and R_2 set the shutdown level while R_3 adds positive feedback for hysteresis.

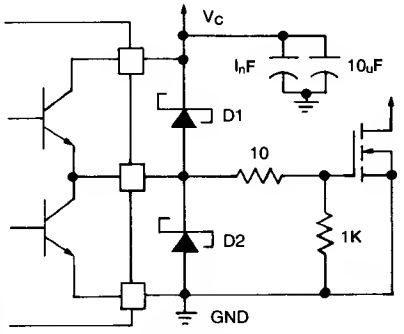
Charge Pump Circuits



When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

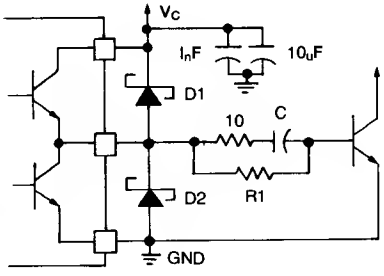
OUTPUT STAGE COUPLING

Power MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diodes

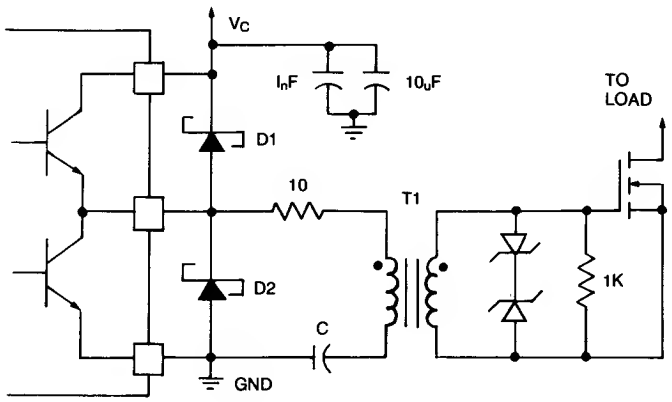
Power Bipolar Drive Circuit



D1:D2: UC3611 Schottky Diodes

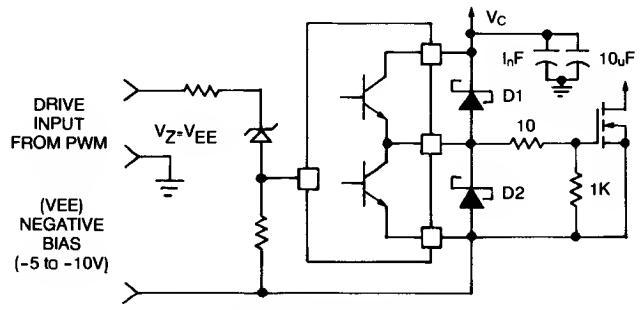
TRANSFORMER COUPLING

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS



D1.D2: UC3611 Schottky Diodes

UC1708
UC3708

Dual Non-Inverting Power Driver

PRELIMINARY

FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25nSec Rise and Fall Times
- 25nSec Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 to 35 volt supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as VIN. Each output can source or sink up to 3A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

These devices are available in plastic 8-pin MINIDIP and 16-pin "bat-wing" DIP packages for operation over a 0°C to +70°C temperature range. For operation over a -55°C to +125°C temperature range, the device is available in hermetically sealed 8-pin MINIDIP and 16 pin DIP packages.

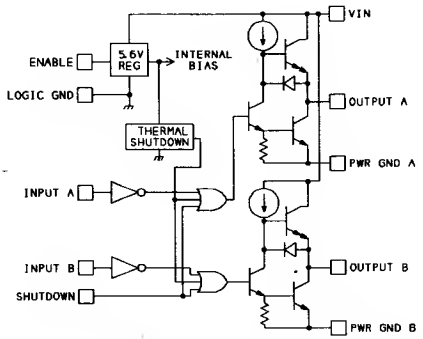
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{IN} 35V
Output Current (Each Output, Source or Sink)
Steady-State 0.5A
Peak Transient 3A
Ouput Voltage . . . . . -0.3 to (V_{IN} + 0.3)V
Enable and Shutdown Inputs . . . . . -0.3 to 6.2V
A and B Inputs . . . . . -0.3 to (V_{IN} + 0.3)V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

NOTE 1: All voltages are with respect to LOGIC GND pin.
All currents are positive into, negative out of, device terminals.

NOTE 2: Consult Unitrode Integrated Circuits databoook for information regarding thermal specifications and limitations of packages.

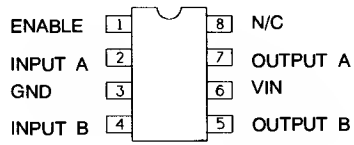
BLOCK DIAGRAM



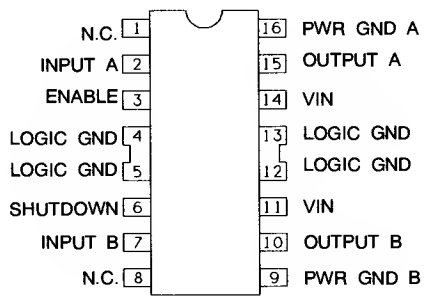
NOTE: Shutdown feature available only in JE or NE packages.

CONNECTION DIAGRAMS

DIL–8 (TOP VIEW)
J or N Package



DIL–16 (TOP VIEW)
JE or NE Package



NOTE: In JE package, Pin 4 is logic ground. Pins 5, 12, and 13 are N/C.

6

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{IN}=10V to 35V, and these specifications apply for: $-55^{\circ}C<T_A<125^{\circ}C$ for the UC1708 and $0^{\circ}C<T_A<70^{\circ}C$ for the UC3724. $T_A=T_j$

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
VIN Supply Current	Outputs Low		18	24	mA
	Outputs High		14	20	mA
	Enable=0V		1	5	mA
A, B and Shutdown Inputs Low Level				0.8	V
A, B and Shutdown Inputs High Level		2.0			V
A, B Input Current Low	$V_{A,B}$=0.4V	–1	–0.6		mA
A, B Input Current High	$V_{A,B}$=2.4V	–200		50	µA
A, B Input Leakage Current High	$V_{A,B}$=35.3V			200	µA
Shutdown Input Current Low	$V_{SHUTDOWN}$=0.4V		20	50	µA
Shutdown Input Current High	$V_{SHUTDOWN}$=2.4V		170	300	µA
	$V_{SHUTDOWN}$=6.2V		0.6	1	mA
Enable Input Current Low	V_{ENABLE}=0V	–600	–460	200	µA
Enable Input Current High	V_{ENABLE}=6.2V				µA
Output High Sat., V_{IN}–V_{OUT}	I_{OUT}=–50mA			2.0	V
	I_{OUT}=–500mA			2.5	V
Output Low Sat., V_{OUT}	I_{OUT}=50mA			0.4	V
	I_{OUT}=500mA			2.5	V
Thermal Shutdown			155		°C

SWITCHING CHARACTERISTICS (Figure 1)

(VIN=20V, delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
From A,B Input to Output:					
Rise Time Delay (TPLH)	CL = 0pF		25	40	nS
	CL = 1000pF (Note 3)		25	40	nS
	CL = 2200pF		30	40	nS
10% to 90% Rise (TTLH)	CL = 0pF		55	75	nS
	CL = 1000pF (Note 3)		25	50	nS
	CL = 2200pF		40	50	nS
Fall Time Delay (TPHL)	CL = 0pF		25	40	nS
	CL = 1000pF (Note 3)		25	45	nS
	CL = 2200pF		35	50	nS
90% to 10% Fall (TTHL)	CL = 0pF		25	60	nS
	CL = 1000pF (Note 3)		25	50	nS
	CL = 2200pF		40	50	nS

NOTE 3: These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.

SWITCHING CHARACTERISTICS (continued)

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
From Shutdown Input to Output:					
Rise Time Delay (TPLH)	CL = 0pF		25	60	nS
	CL = 1000pF (Note 3)		30	65	nS
	CL = 2200pF		35	70	nS
10% to 90% Rise (TTLH)	CL = 0pF		50	75	nS
	CL = 1000pF (Note 3)		25	50	nS
	CL = 2200pF		40	55	nS
Fall Time Delay (TPHL)	CL = 0pF		25	45	nS
	CL = 1000pF (Note 3)		30	50	nS
	CL = 2200pF		35	55	nS
90% to 10% Fall (TTHL)	CL = 0pF		25	60	nS
	CL = 1000pF (Note 3)		25	50	nS
	CL = 2200pF		40	50	nS
VIN Cross-Conduction Current Spike Duration	Output Rise		50		nS
	Output Fall		50		nS

NOTE 3: These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.

Figure 1: AC Test Circuit and Switching Time Waveforms

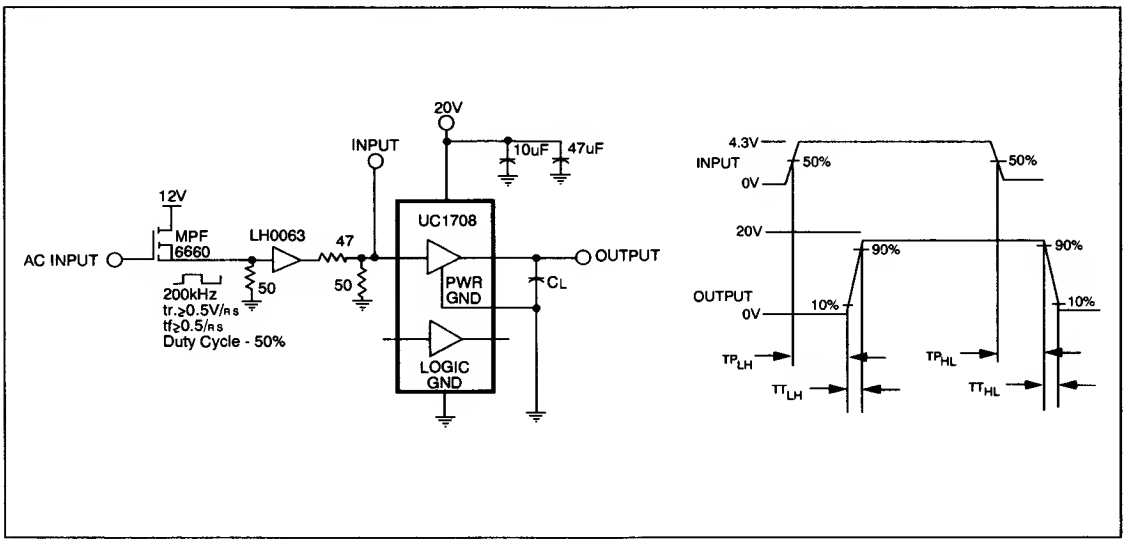
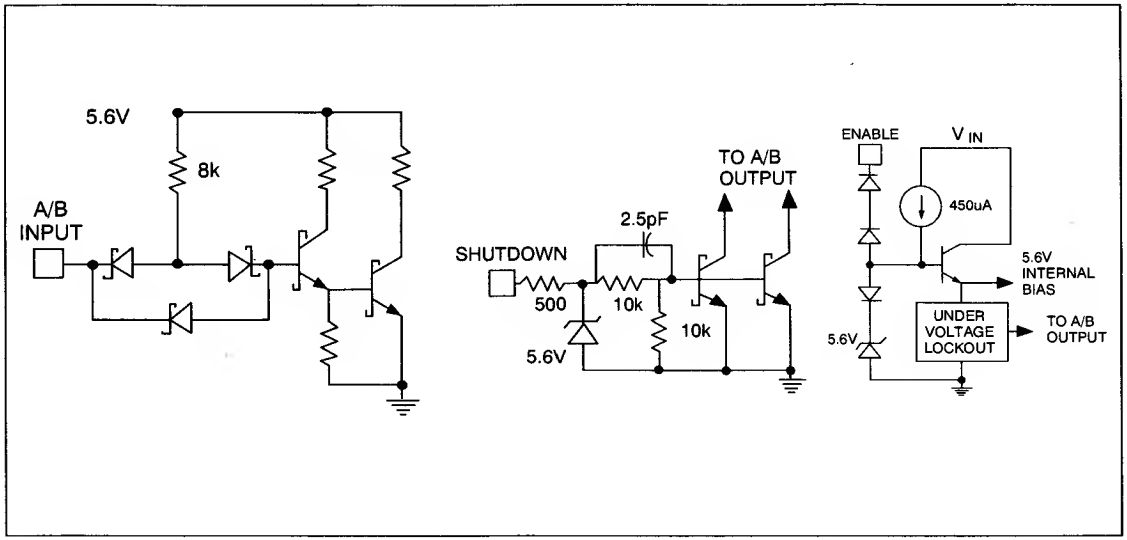


Figure 2: Equivalent Input Circuits



Unitrode Integrated Circuits Corporation
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Telephone 603-424-2410 • FAX 603-424-3460

INTEGRATED CIRCUITS

UNITRODE

UC1709
UC3709

Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection
- 8-Pin Minidip Package

DESCRIPTION

The UC1709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 amps of either source or sink current from e totem-pole output stage configured for minimal cross-conduction current spike.

Packaged in an 8-Pin ceramic or plastic minidip, the 1709 (3709) is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30V. This design also includes thermal shutdown protection end an under-voltage lockout circuit which prevents any undefined states at turn-on or turn-off by disabling the output stage.

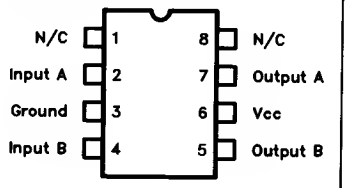
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40V	40V
Output Current (Source or Sink)		
Steady-State	±500 mA	±500 mA
Peek Transient	±1.5A	±1.0A
Capecitive Discharge Energy	20 μJ	15 μJ
Digital Inputs (See Note)	5.5V	5.5V
Power Dissipetion at T_A = 25°C	1W	1W
Derate above 50°C	10 mW/°C	10 mW/°C
Power Dissipetion et T_C = 25°C	3W	2W
Derete for Case Temperature above 25°C	25 mW/°C	16 mW/°C
Opereting Tempereture Renge	−55°C to +125°C	−55°C to +125 °C
Storege Tempereture Renge	−65°C to +150°C	−65°C to +150°C
Load Temperature (Soldering, 10 Seconds)	300°C	300°C

Note: All currents are positive into, negative out of the specified terminals. Digital Drive can exceed 5.5V if input current is limited to 10 mA.

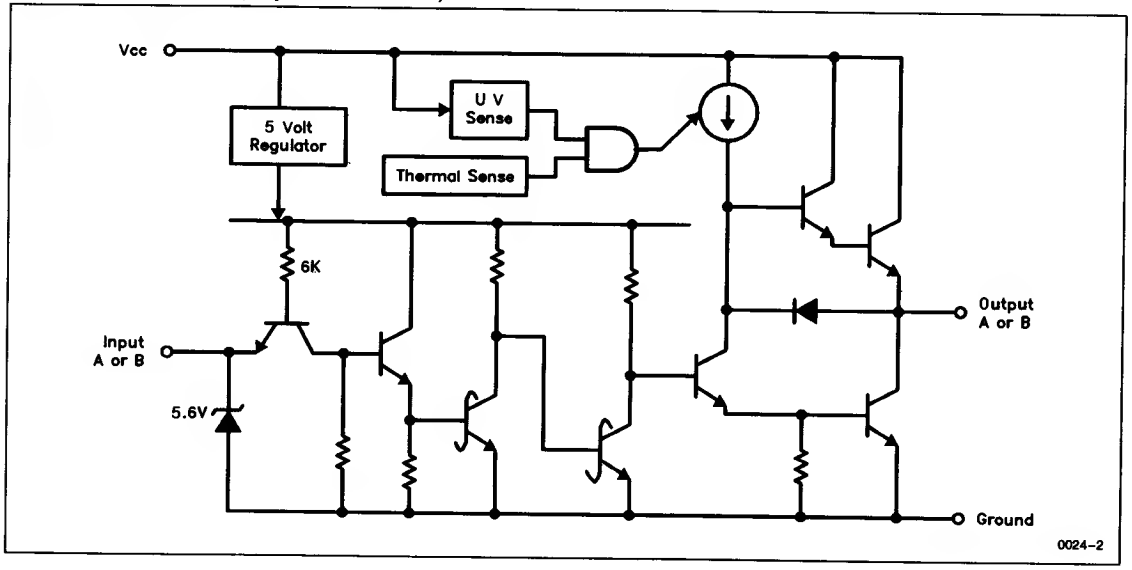
CONNECTION DIAGRAM

TOP VIEW
8-PIN N or J PACKAGE



0024-1

SIMPLIFIED SCHEMATIC (Only One Driver Shown)



0024-2

6

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, these specifications apply for $T_A = -55°C$ to $+125°C$ for the UC1709, and $0°C$ to $+70°C$ for the UC3709; $V_{CC} = 20V$) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Both Outputs High		10	12	mA
Supply Current	Both Outputs Low		7	10	mA
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	$V_I = 0V$		−0.6	−1.0	mA
Input Leakage	$V_I = 5V$		0.05	0.1	mA
Output High Sat., $V_{CC}-V_O$	$I_O = -50$ mA		1.5	2.0	V
Output High Sat., $V_{CC}-V_O$	$I_O = -500$ mA		2.0	2.5	V
Output Low Sat., V_O	$I_O = 50$ mA		0.1	0.4	V
Output Low Sat., V_O	$I_O = 500$ mA		2.0	2.5	V
Thermal Shutdown			155		°C

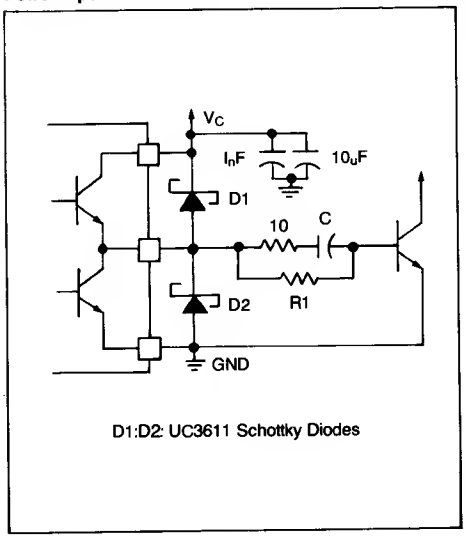
TYPICAL SWITCHING CHARACTERISTICS ($V_{CC} = 20V$, $T_A = 25°C$. Delays measured to 10% output change)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =		UNITS
		0 nF	2.2 nF	
Rise Time Delay		80	80	ns
10% to 90% Rise		20	40	ns
Fall Time Delay		60	80	ns
90% to 10% Fall		20	40	ns
V_{CC} Cross Conduction Current Spike	Output Rise	25		ns
	Output Fall	0		ns

NOTE: Refer to UC1705 specification for further information.

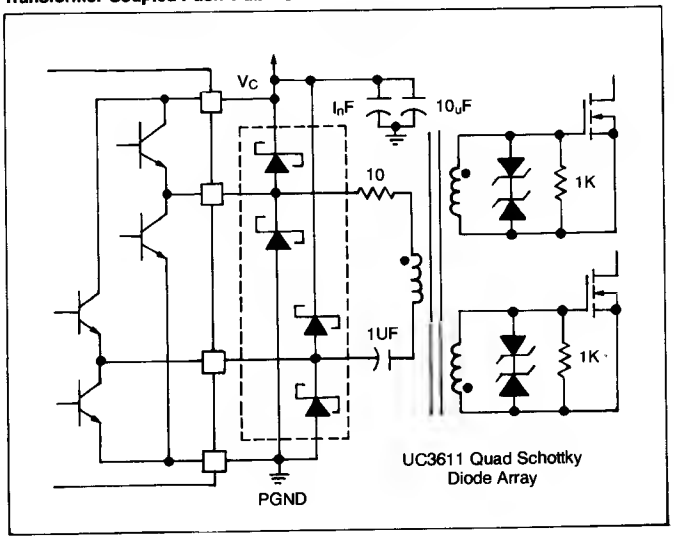
APPLICATIONS

Power Bipolar Drive Circuit



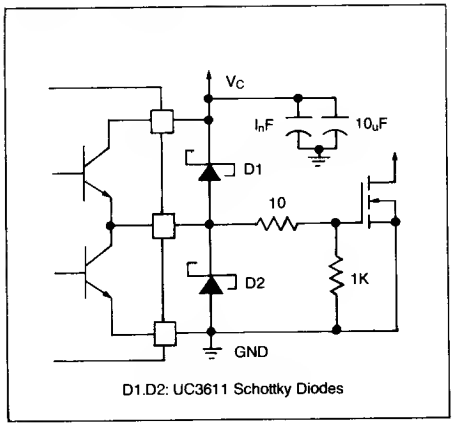
D1:D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



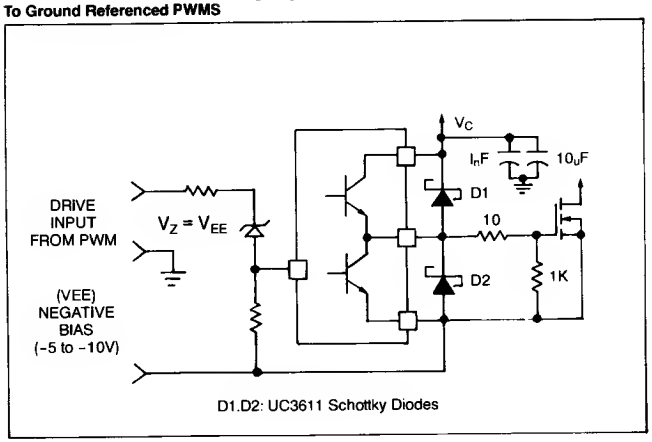
UC3611 Quad Schottky Diode Array

Power MOSFET Driva Circuit



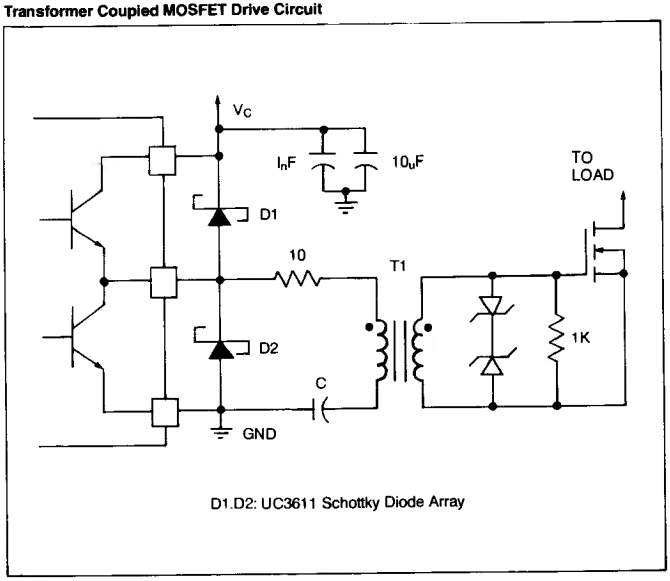
D1.D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS



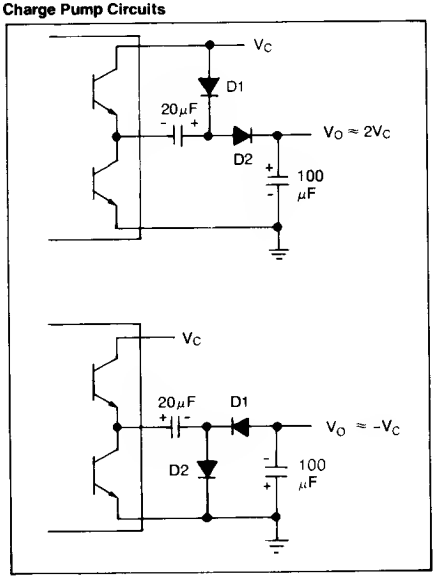
D1.D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Charge Pump Circuits



6

INTEGRATED CIRCUITS

UNITRODE

High Current FET Driver

UC1710
UC3710

PRELIMINARY

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 35 nsec Delay
- 25 nsec Rise and Fall Time into 2.2nF
- 85 nsec Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both Vin and Vc can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to +125°C operation. The UC3710 is specified for a temperature range of 0°C to +70°C and is available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package.

TRUTH TABLE

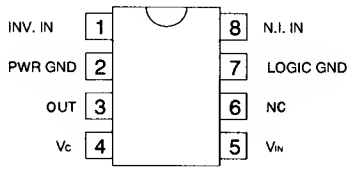
INV	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{INV}$ and N.I.

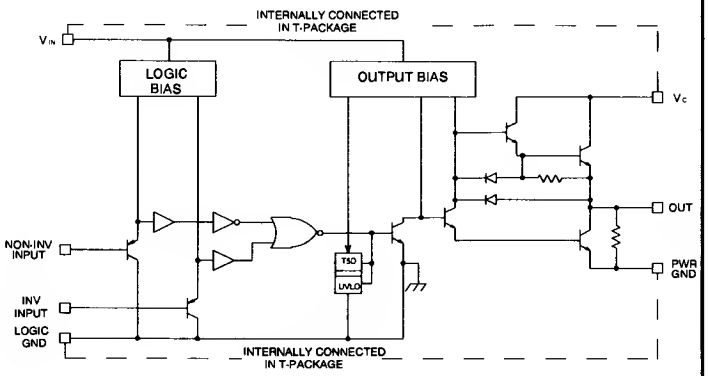
$\overline{OUT}$ = INV or $\overline{N.I.}$

CONNECTION DIAGRAMS

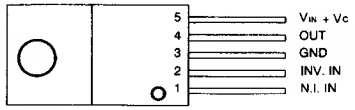
DIL-8 MINIDIP
N or J Package
Top View



BLOCK DIAGRAM



5-Pin TO-220
T Package
Top View



ABSOLUTE MAXIMUM RATINGS	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, V_C	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1A
Digital Inputs	-.3V-Vin	-.3V-Vin	-.3V-Vin
Power Dissipation at Ta=25°C	1W	1W	3W
Derate above 50°C	10mW/°C	10mW/°C	25mW/°C
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Derate for Case Temperature above 25°C	16mW/°C	16mW/°C	200mW/°C
Operating Junction Temperature	-55°C-+150°C	-55°C-+150°C	-55°C-+150°C
Storage Temperature	-65°C-+150°C	-65°C-+150°C	-65°C-+150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

NOTE: All currents are positive into, negative out of the specified terminal

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for the UC1710 and T_A=0 °C to +70°C for the UC3710; Vin=Vc=15V, No load.) $T_A=T_J$

PARAMETERS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Vin Supply Current	Vin=18V, Vc=18V					
		Output Low		26	35	mA
		Output High		21	30	mA
Vc Supply Current	Vin=18V, Vc=18V					
		Output Low		1.5	5.0	mA
		Output High		5.0	8	mA
UVLO Threshold	Vin High to Low		3.8	4.1	4.4	V
UVLO Threshold	Vin Low to High		4.1	4.4	4.7	V
UVLO Threshold Hysteresis			0.2	0.3	0.5	V
Digital Input Low Level					0.8	V
Digital Input High Level			2.0			V
Digital Input Current	Digital Input=0.0V		-30	-4.0		uA
Output High Sat., Vc-Vo	Io=-100mA			1.35	2.2	V
Output High Sat., Vc-Vo	Io=-6A			3.2	4.5	V
Output Low Sat., Vo	Io=100mA			0.25	0.6	V
Output Low Sat., Vo	Io=6A			3.4	4.5	V
Thermal Shutdown				165		°C
From Inv. Input to Output (Note 1,2):						
Rise Time Delay	CL =0			35	70	ns
	CL = 2.2nF			35	70	ns
	CL = 30nF			35	70	ns
10% to 90% Rise	CL = 0			20	40	ns
	CL = 2.2nF			25	40	ns
	CL = 30nF			85	150	ns

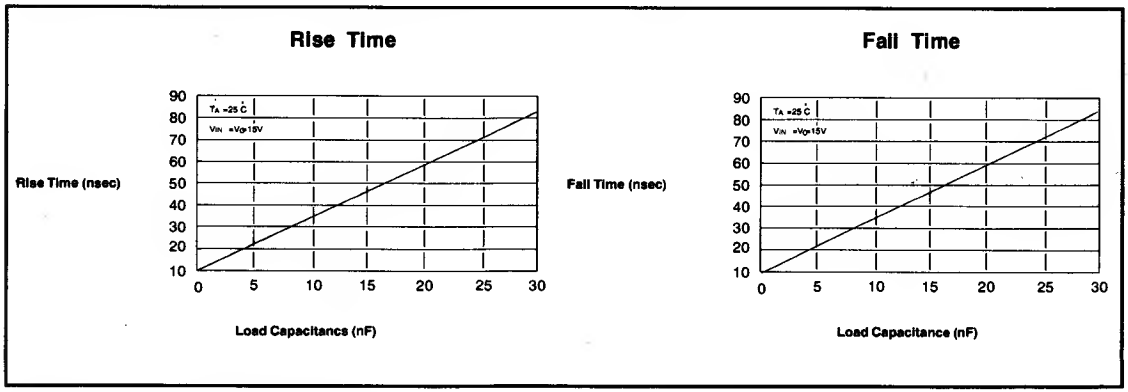
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 1,2):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns
Total Supply Current	T_A = 25°C				
at 200kHz Input	(Note 3)				
Switching Frequency	CL = 0		30	40	mA

Note: 1. Delay measured from 50% input change to 10% output change.

Note: 2. Those parameters, with CL = 30nF, are not tested in production.

Note: 3. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = OV.

TYPICAL PERFORMANCE CHARACTERISTICS



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UC1711 Dual Ultra High-Speed FET Driver

PRELIMINARY

FEATURES

- 25nS Rise and Fall into 1000pF
- 15nS Propagation Delay
- 1.5Amp Source or Sink Output Drive
- Operation with 5V to 35V Supply
- High-Speed Schottky NPN Process
- 8-PIN Mini-DIP Package

DESCRIPTION

The UC1711 family of FET drivers are made with an all-NPN Schottky process in order to optimize switching speed, temperature stability, and radiation resistance. The cost for these benefits is a quiescent supply current which varies with both output state and supply voltage. For lower power requirements, refer to the the UC1709 family which is both pin compatible with, and functionally equivalent to the UC1711.

These devices implement inverting logic with TTL compatible inputs, and output stages which will either source, or sink in excess of 1.5A of load current with minimal cross-conduction charge. Due to their monolithic construction, the channels are well matched and can be paralleled for doubled output current capability.

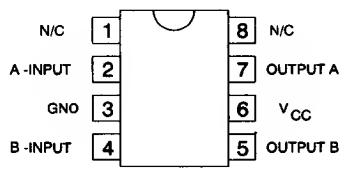
ABSOLUTE MAXIMUM RATINGS (note 1)

Input Supply Voltage, Vcc 40V
Output Current (Source or Sink)
Steady State . . . . . +/-500mA
Peak Transient . . . . . +/-1.5A
Inputs
maximum forced voltage . . . . . .-0.3V to 7V
maximum forced current . . . . . .+/- 10mA
Power Dissipation at T_a = 25°C 1W
Derate N, or J for T_a > 50°C . . . . . .10mW/°C
Power Dissipating at T_a = 25°C 1W
Derate N for T_c > 25°C . . . . . .25mW/°C
Derate J for T_c > 25°C . . . . . .16mW/°C
Operating Junction Temperature . . . . . -55°C to =150°C
Storage Temperature . . . . . -65°C to +150°C

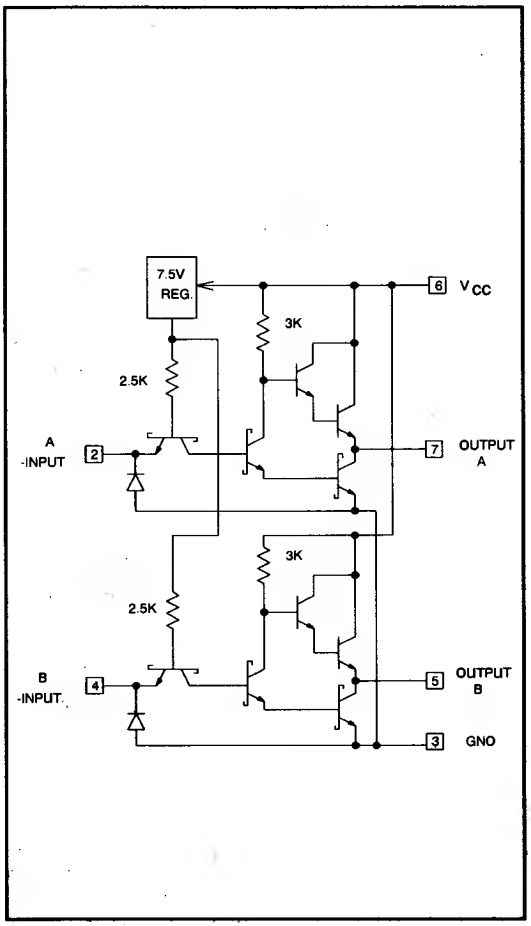
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8 TOP VIEW
J OR N PACKAGE



EQUIVALENT SCHEMATIC



Electrical Characteristics: Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, Vcc = 15V. T_A=T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (Note 2)	Both inputs=OV Vcc=15V		11	15	mA
	Both inputs=5V, Vcc=15V		20	27	mA
	Both inputs=OV, Vcc=35V		15	20	mA
	Both inputs=5V, Vcc=35V		41	56	mA
Logic Inputs					
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	Vin = 0V	-5.0	-2.7		mA
	Vin = 5V		0.5	2.0	mA
Output Stages					
Output High Level	Isource = 20mA, below Vcc		1.5	2.0	V
	Isource = 200mA, below Vcc		2.0	3.0	V
Output Low Level	Isink = 20mA		.25	0.4	V
	Isink = 200mA		0.4	1.0	V
Switching Characteristics (Note 3)					
Rise Time Delay, TPLH	Cload = 0		10	40	nS
	Cload = 1000pF, Note 4		15	50	nS
	Cload = 2200pF		20	55	nS
Fall Time Delay, TPHL	Cload = 0		3	20	ns
	Cload = 1000pf, Note 4		5	20	nS
	Cload = 2200pF		5	20	nS
Rise Time, TLH	Cload = 0, Note 4		12	25	nS
	Cload = 1000pF, Note 4		25	40	nS
	Cload = 2200pF		40	55	nS
Fall Time, THL	Cload = 0, Note 4		7	15	nS
	Cload = 1000pF, Note 4		25	40	nS
	Cload = 2200pF		40	55	nS
Total Supply Current	Freq=200KHz, 50% Duty-cycle				
	Both Channels Switching				
	Cload = 0		17	23	mA
	Cload = 2200pF		29	35	mA

Note 2: Supply currents at other input supply votages can be calculated by extrapolating the 15V and 35V supply currents. The impedance of the chip at the Vcc pin is linear for supply voltages from 8V to 35V, the approximate value of this impedance is 4.3K for both inputs low, 0.94K for both inputs high, and 1.54K for one input high and one low.

Note 3: Switching test conditions are, Vcc=15V, Input voltage waveform levels are OV and 5V, with transition times of < 3nS. The timing terms are defined as : TPHL Propagation delay 50% Vin to 90% Vout; TPLH Propogation delay 50% Vin to 10% Vout; THL 90% Vout to 10% Vout TLH 10% Vout to 90% Vout

Note 4: This specification not tested in production.

Smart Switch

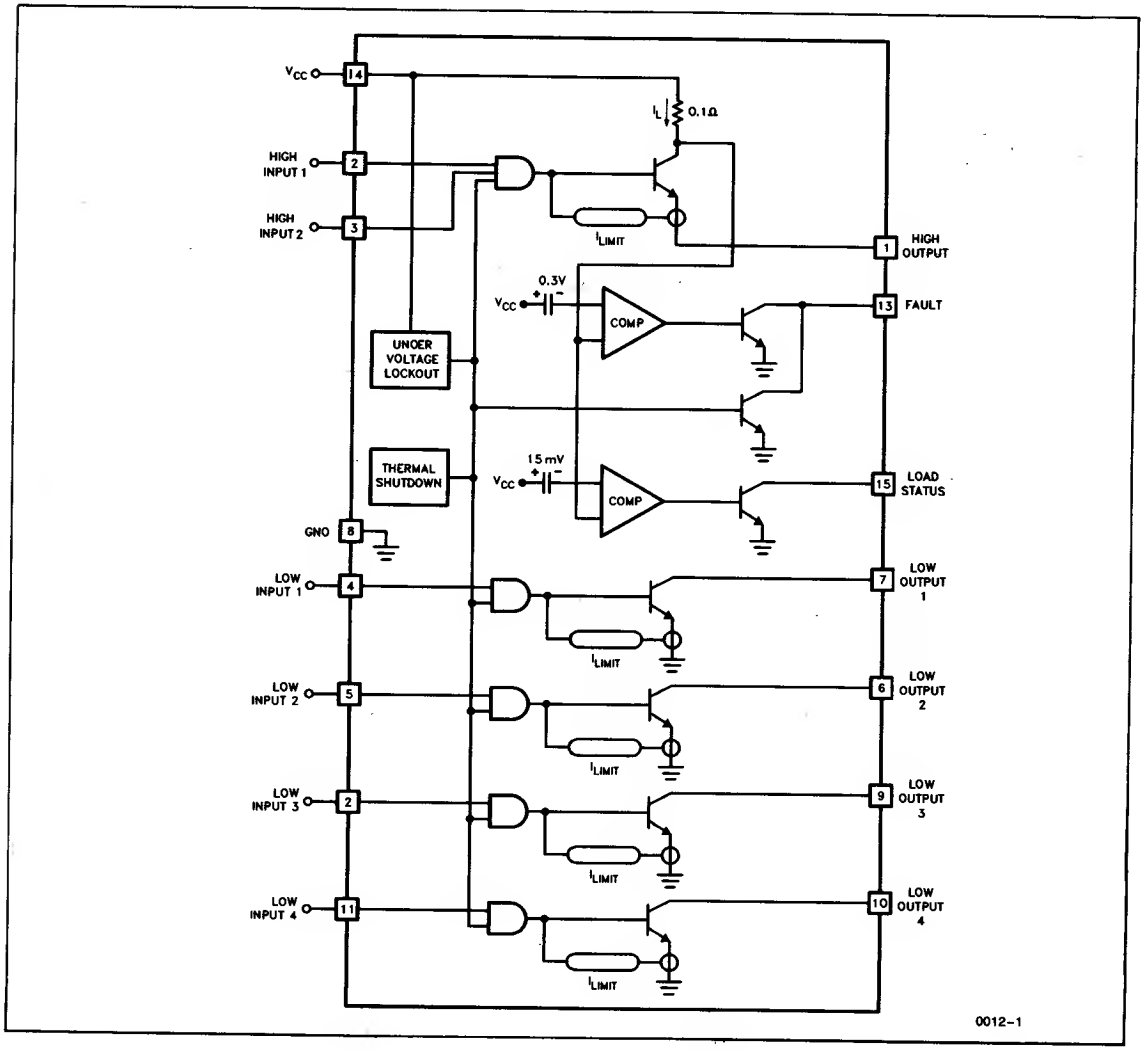
FEATURES

- 60V Operation
- 4 Independent Low Side Switches with 1A Capability
- 4.5A High Side Switch Capability
- Over and Under Current Fault Indication
- Short Circuit and Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt Package
- 24 Lead, 25W Power Ceramic Package

DESCRIPTION

The UC3720 Smart Switch contains a fully protected 4.5A high side switch along with four 1A low side switches. This device allows for the control of up to four separate loads while monitoring for both shorted or open conditions at the point of load. A full range of protection circuitry including instantaneous current limit, under-voltage lockout, hiccup mode current limit, and thermal shutdown allow for safe reliable operation. The UC1720 is characterized for operation over full military temperature range of —55°C to +125°C, while the UC3720 is characterized for 0°C to +70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{CC} 60V

Output Current, High Side Switch (pin 1)
- Non-Repetitive ($t \leq 50\ \mu s$) ..... −8A
- DC Operation ..... −4.5A

Output Current, Low Side Switches (pins 6, 7, 9, 10)
- Non-Reptitive ($t = 50\ \mu s$) 1.5A
- DC Operation 1A

Logic Inputs ..... −0.3 to 7V

Total Power Dissipation (at $T_{CASE} = 75°C$) 25W

Storage and Junction Temperature ..... −65°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, θ_{jc} ..... 3°C/W Max

Thermal Resistance Junction-Ambient, θ_{ja} ..... 35°C/W Max

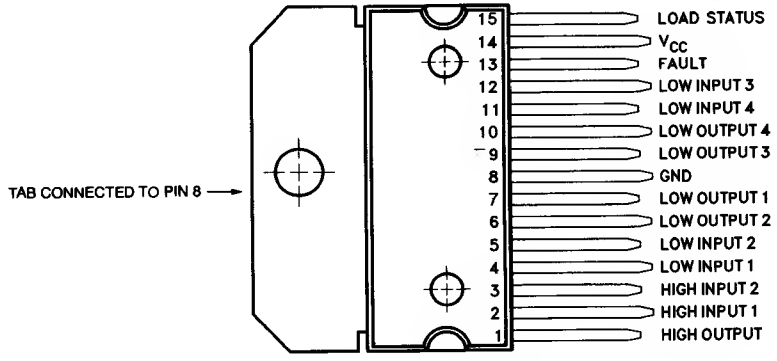
Note: 1. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = −55°C to +125°C for the UC1720 and 0°C to +70°C for the UC3720; V_{IN} = 28VDC. $T_A = T_J$

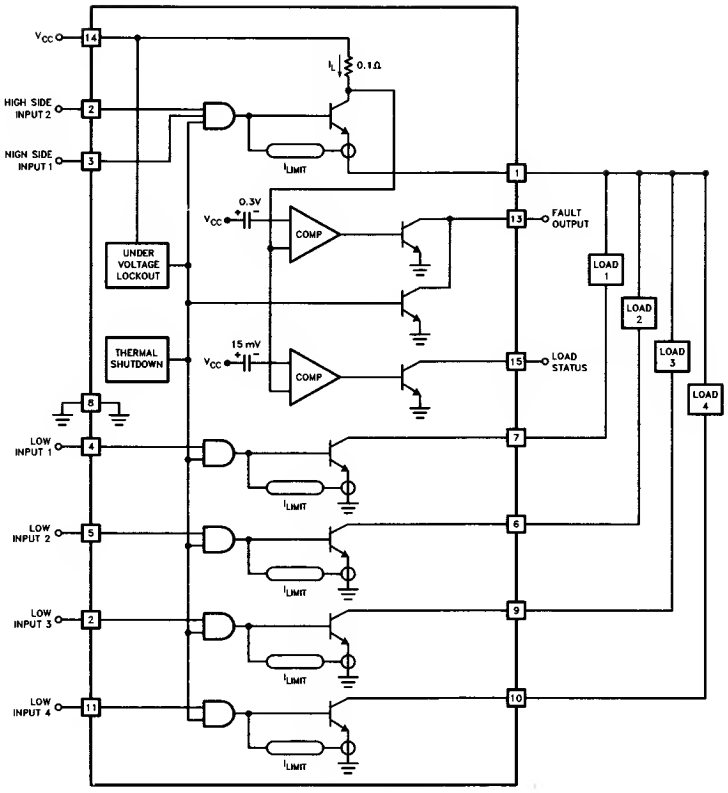
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage		8		40	V
Supply Current	$V_{PIN1} = V_{PIN2} = 0V$			20	mA
LOGIC INPUTS					
High-Level Input Voltage		3.0			V
Low-Level Input Voltage				0.8	V
High-Level Input Current	$V_{IN} = 5.5V$			250	μA
Low-Level Input Current	$V_{IN} = 0.4V$	−160			μA
LOAD STATUS					
Output Sink Current	$V_{OUT} = 0.4V$	0.5			mA
Current Detect Threshold			150		mA
FAULT					
Output Sink Current	$V_{OUT} = 0.4V$	0.5			mA
Overcurrent Threshold			3.0		A
U.V. Lockout Threshold		6.0		8.0	V
Thermal Shutdown			160		°C
HIGH SIDE SWITCH					
V_{SAT} ($V_{PIN14} - V_{PIN1}$)	$I_{LOAD} = 3A$			2	V
Output Leakage Current				100	μA
Output Current Limit			8.0		
LOW SIDE SWITCHES					
V_{SAT} ($V_{PIN6,7,9,10}$)	$I_{LOAD} = 0.75A$			1.4	V
Output Leakage Current	$V_O = 28V$			50	μA
Output Current Limit			1.5		A

CONNECTION DIAGRAM

(TOP VIEW)



TYPICAL APPLICATIONS



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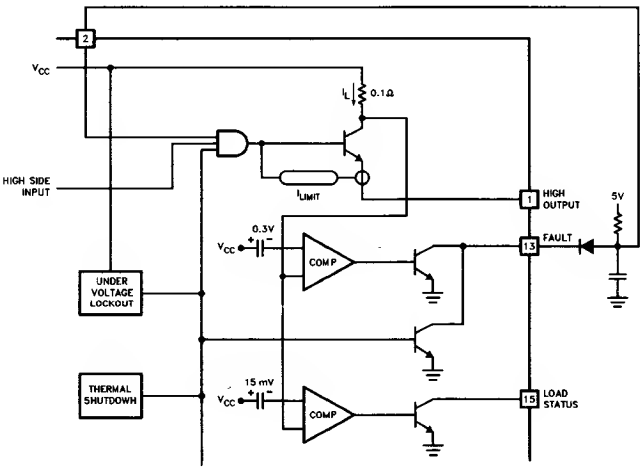
TYPICAL LOAD CONFIGURATION

Hiccup-Mode Current Limit



0012-5

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INTEGRATED CIRCUITS

UNITRODE

Isolated Drive Transmitter

UC1724
UC2724
UC3724

PRELIMINARY

FEATURE

- 500mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Logic Signal Instantly
- Programmable Operating Frequency
- Under-Voltage Lockout
- Able To Pass DC Information Across Transformer
- Up To 600kHz Operation

DESCRIPTION

The UC1724 family of Isolated Drive Transmitters, along with the UC1725 Isolated Drivers, provide a unique solution to driving isolated power MOSFET gates. They are particularly suited to drive the high-side devices on a high-voltage H-bridge. The UC1724 devices transmit drive logic, and drive power, to the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty-cycle modulation technique that gives instantaneous response to the drive control transistions, and reliably passes steady-state, or DC, conditions. High frequency operation, up to 600kHz, allows the cost and size of the coupling transformer to be minimized.

These devices will operate over an 8 to 35 Volt supply range. The dual high current totem pole outputs are disabled by an uder-voltage lockout circuit to prevent spurious responses during startup or low voltage conditions.

These devices are available in 8-pin plastic or ceramic dual-inline packages.

ABSOLUTE MAXIMUM RATINGS (Note 1)

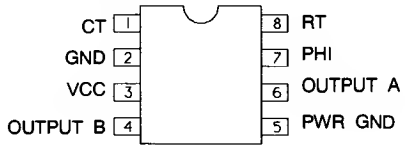
Supply Voltage V_{IN} 40V
Source/Sink Current (Pulsed) 1A
Source/Sink Current (Continuous) 0.5A
Ouput Voltage (pins 4, 6) . . . . . -0.3 to (VIN +0.3)V
PHI, Rt, and Ct inputs (pins 1, 7, and 8) . . . . . -0.3 to 6V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

NOTES 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.

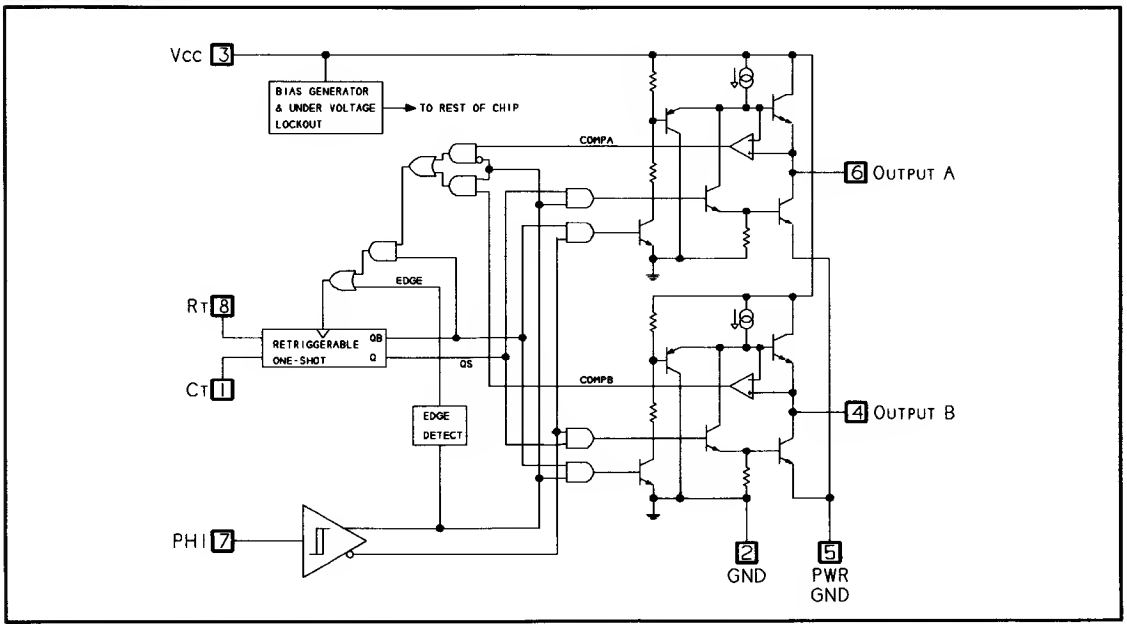
2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
J or N Package



BLOCK DIAGRAM



RECOMMENDED OPERATION CONDITIONS (Note 3)

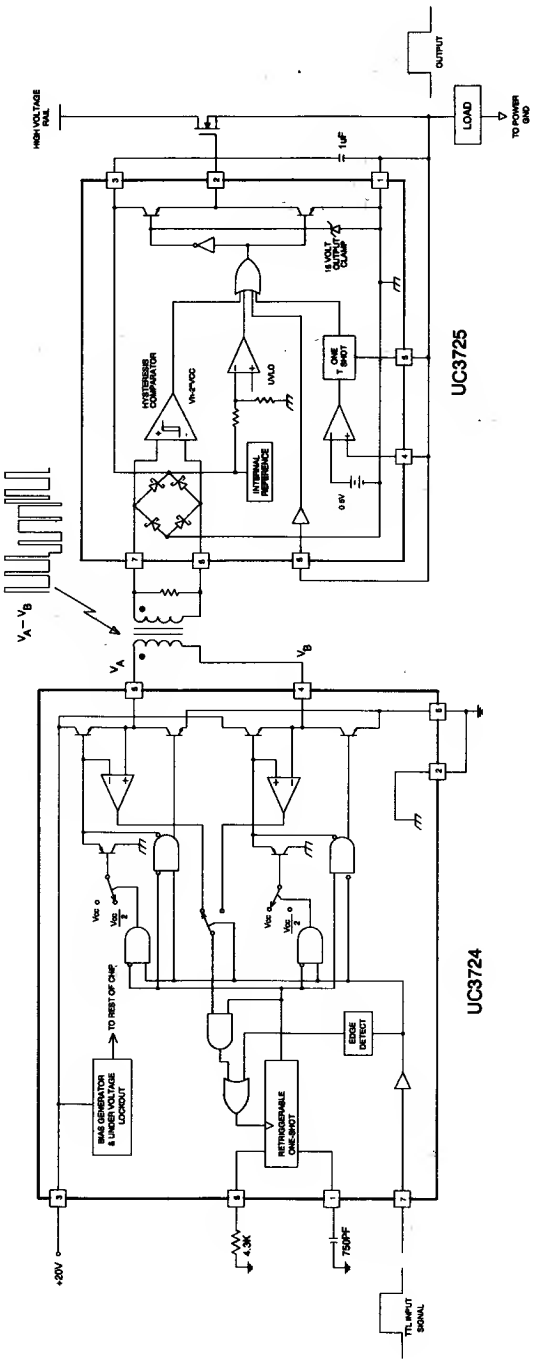
Input Voltage . . . . . +9V to +35V
Sink/Source Load Current (each output) . . . . . .0 to 500mA
Timing Resistor . . . . . 2kOhm to 100kOhm
Timing Capacitor . . . . . .300pF to 3nF
Operating Temperature Range (UC1724) . . . . . -55°C to +125°C
Operating Temperature Range (UC3724) . . . . . .0°C to +70°C

NOTE 3: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, V_{CC}=20V, R_T=4.3kOhm, C_T=1000pF, no load on any output, and -55°C<T_A<125°C for the UC1724, -25°C<T_A<85°C for the UC2724, and 0°C<T_A<70°C for the UC3724. $T_A = T_j$

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
UNDER-VOLTAGE LOCKOUT					
Start-Up Threshold	V_{IN} Rising		9.0	9.5	V
Threshold Hysteresis			1.0		V
RETRIGGERABLE ONE-SHOT					
Initial Accuracy	T_J=25°C	1.854	1.667	1,75	µSec
Temperature Stability	Over Operating T_J	1.069		2.049	µSec
Voltage Stability	V_{IN} = 10 to 35V		0.2		%/V
Operating Frequency	L_{LOAD} = 1.4mH		145		kHz
Minimum Pulse Width	RT = 2k C_T = 300pF			300	nSec
Operating Frequency	RT = 2k C_T = 300pF L_{LOAD} = 1.4mH		560		kHz
PHI INPUT (CONTROL INPUT)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current	V_{IH} = +2.4V	-220	-130		µA
LOW Input Current	V_{IL} = +0.4V	-600	-300		µA
Delay to One-Shot				250	nSec
Delay to Output				250	nSec
OUTPUT DRIVERS					
Output Low Level	I_{SINK} = 500mA		0.3	0.4	V
	I_{SINK} = 250mA		0.5	2.1	V
Output High Level (volts below V_{CC})	I_{SOURCE} = 250 mA		1.5	2.1	V
	I_{SOURCE} = 250 mA		1.7	2.1	V
Rise/Fall Time	No load		30	90	nSec
TOTAL SUPPLY CURRENT					
Supply Current	C_T = 1.4V		15	30	mA

"TYPICAL APPLICATION"



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INTEGRATED CIRCUITS

UNITRODE

Isolated High Side FET Driver

UC1725
UC2725
UC3735

PRELIMINARY

FEATURES

- Receives both power and signal across the isolation boundary
- 9 to 15 volt high level gate drive guaranteed
- Under-voltage lockout
- Programmable over-current shutdown and restart
- Output enable function

DESCRIPTION

The UC1725 and its companion chip, the UC1724, provide all the necessary features to drive an isolated MOSFET transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signals across an isolation boundary with a minimum of external components.

Protection circuitry, including under-voltage lockout, over-current shutdown, and gate voltage clamping provide fault protection for the MOSFET. High level gate drive is guaranteed to be greater than 9 volts and less than 15 volts under all conditions.

Uses include isolated off-line full bridge and half bridge drives for driving motors, switches, and any other load requiring full electrical isolation.

The UC1725 is characterized for operation over the full military temperature range of -55°C to +125°C while the UC2725 and UC3725 are characterized for -25°C to +85°C and 0°C to +70°C respectively.

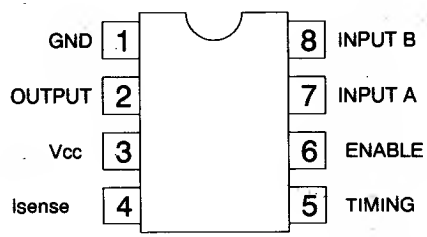
ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage (pin 3) 30V
Power inputs (pins 7 & 8) 40V
Output current, source or sink (pin 2)
DC 0.5A
Pulse (0.5 us) 2.0A
Enable and Current limit inputs (pins 4 & 6) . . . . . -0.3 to 6V
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mw/ C for $T_A > 25°C$
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Derate 5.8mw/ C for $T_A > 25°C$
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

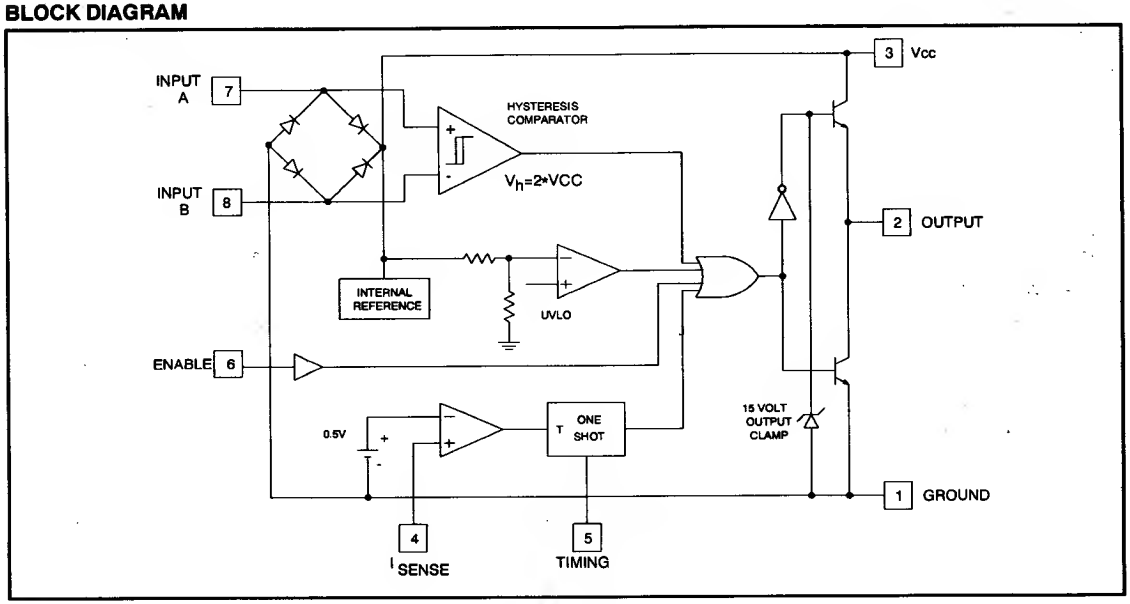
Note 1. All voltages are with respect to ground, pin 1. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-8 (TOP VIEW)
N or J PACKAGE



BLOCK DIAGRAM



6

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for Ta=0 to 70°C; Vcc (pin 3) = 15v, Rt=50k, Ct=.01uf) $T_A = T_j$

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX	UNIT
POWER INPUT SECTION (PINS 7 & 8)					
Forward diode drop, schotkey rectifier	I_F = 50ma		.6	.7	v
	I_F = 500ma		1.1	1.5	v
CURRENT LIMIT SECTION (PIN 4)					
Input bias current	V_{pin4} = OV		1	10	ua
Threshold voltage		0.4	0.5	0.6	v
Delay to outputs	V_{pin4} =0 to 1v		150		ns
TIMING SECTION (PIN 5)					
Output Off Time	C_t = 2.2nf, R_t = 10k		60		us
Upper Mono Threshold			7.0		v
Lower Mono Threshold			2.0		v
HYSTERESIS AMPLIFIER (PINS 7 & 8)					
Input open circuit voltage	inputs (pins 7 & 8) open circuited ta=25°C	7.0	Vcc/2	8.0	v
Input impedance	ta=25°C	23	28	33	kohm
Hysteresis			2*Vcc		v
Delay to outputs	V_{pin7}–V_{pin8}=Vcc+1v		200		ns
ENABLE SECTION (PIN 6)					
High Level input voltage		2.1	1.4		v
Low Level input voltage			1.4	.8	v
Input bias current			–200	–500	ua
OUTPUT SECTION					
Output Low Level	I_{out} = 20ma		.5	0.4	v
	I_{out} = 200ma		1.2	2.2	v
Output High Level	I_{out} = –20ma	13	13.5		v
	I_{out} = –200ma	12	13.4		v
	V_{cc} = 30v, I_{out} = –20ma		14	15	v
Rise/Fall Time	Ct = 1nf		30	60	ns
UNDER VOLTAGE LOCKOUT					
UVLO Low Saturation	20ma, Vcc=8V		0.8	1.5	v
Start-up threshold		11.2	12	12.6	v
Threshold hysteresis		.75	1.0	1.12	v
TOTAL STANDBY CURRENT					
Supply current			12	16	ma

NOTES: 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

APPLICATION INFORMATION

INPUTS

Figure 1 shows the rectification and detection scheme used in the UC1725 to derive both power and signal information from the input waveform. Vcc is generated by peak detecting the input signal via the internal bridge rectifier and storing on a small external capacitor, C1. Note that this capacitor is also used to bypass high pulse currents in the output stage, and therefore should be placed direclty between pins 1 and 3 using minimal lead lengths.

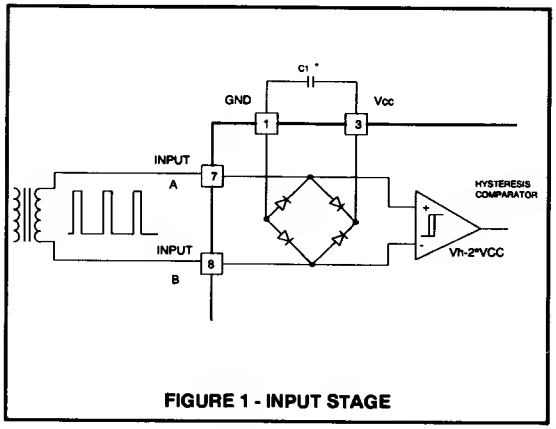


FIGURE 1 - INPUT STAGE

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in figure 2. This is accomplished by setting (resetting) the comparator only if the input signal exceeds Vcc (-Vcc). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis amplifier as shown in figure 3.

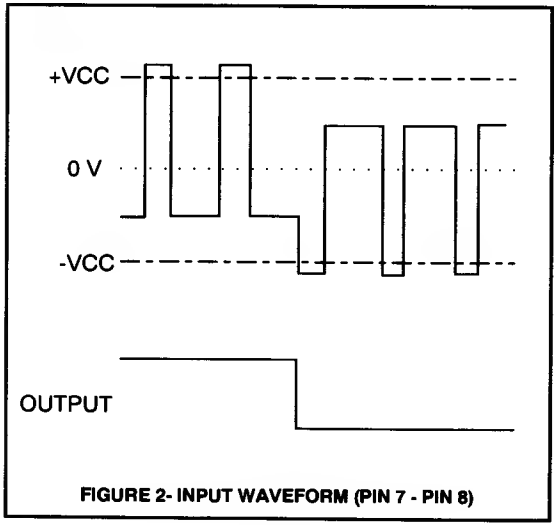
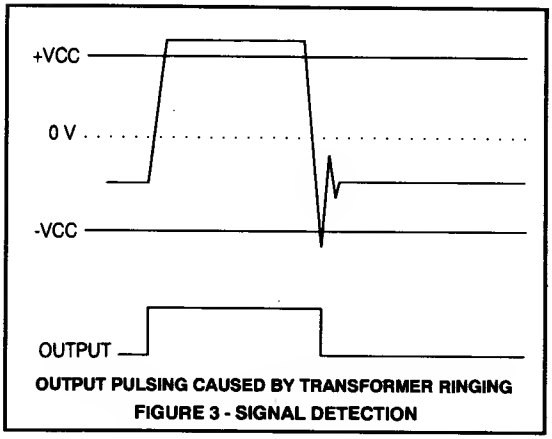


FIGURE 2- INPUT WAVEFORM (PIN 7 - PIN 8)



OUTPUT PULSING CAUSED BY TRANSFORMER RINGING

FIGURE 3 - SIGNAL DETECTION

CURRENT LIMIT AND TIMING

Current sensing and shutdown can be implemented directly at the output using the scheme shown in figure 4. Alternatively, a current transformer can be used in place of Rsense. A small RC filter in series with the input (pin 4) is generally needed to eliminate the leading edge current spike caused by parasitic circuit capacitances being charged during turn on. Due to the speed of the current sense circuit, it is very important to ground C_F directly to ground (pin 1) as shown to eliminate false triggering of the one shot caused by ground drops.

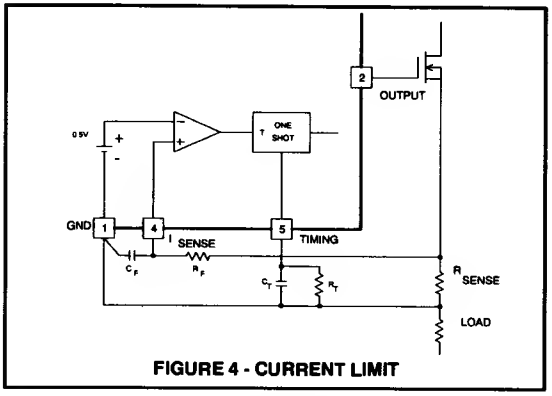


FIGURE 4 - CURRENT LIMIT

One shot timing is easily programmed using an external capacitor and resistor as shown in figure 4. This, in turn, controls the output off time according to the formula:

$$t_{off} = 1.28\ RC$$

OUTPUT

Gate drive to the power FET is provided by a totem pole output stage capable of sourcing and sinking up to 1 amp peak currents. In addition, the undervoltage lockout circuit and output voltage clamp guarantee that the output high level will never be less than 9 volts nor greater than 15 volts under all operating conditions. During

undervoltage lockout, the output stage will actively sink current to eliminate the need for an external gate to source resistor.

ENABLE

An enable pin is provided as a fast, digital input that can be used in a number of applications to directly switch the output. Figure 6 shows a simple means of providing a fast, high voltage translation by using a small signal, high voltage transistor in a cascode configuration. Note that the UC1725 is still used to provide power, drive and protection circuitry for the power FET.

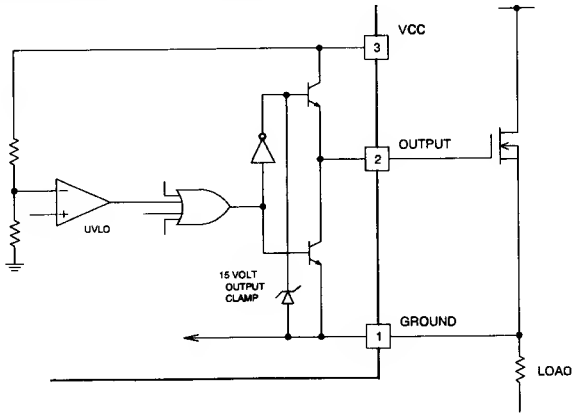


FIGURE 5 - OUTPUT CIRCUIT

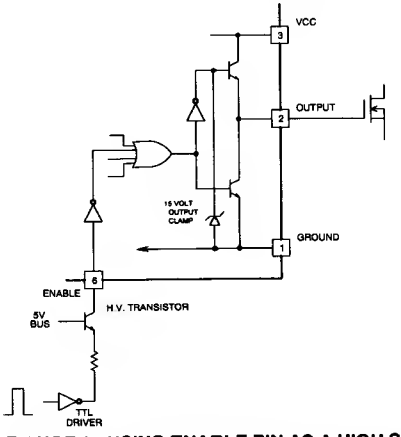


FIGURE 6 - USING ENABLE PIN AS A HIGH SPEED INPUT PATH

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Dual Smart Switch

FEATURES

- Independent Floating Switches
- PWM Current Control
- Supply Voltages to 46V
- Load Currents to 1A
- Transparent Input Latches
- Programmable Current Level
- Three-State Status Outputs
- Over-Current Latch
- Under-Voltage Lockout
- Thermal Shutdown

ABSOLUTE MAXIMUM RATINGS

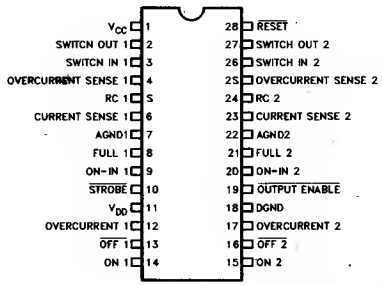
V_{DD} Voltage	7V
V_{CC} Voltage	50V
Switch Input Voltage	V_{CC} +0.3V
Logic Input Voltage	V_{DD} +0.3V
Switch Current, Per Channel	1.5A
Operating Temperature,	
UC1728	-55°C to +125°C
UC3728	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation at T_C = 70°C	1W

DESCRIPTION

This IC performs load control and status monitoring for two inductive loads up to 1 amp each. Loads can be ground referenced, positive supply referenced, or floating, depending on the control and monitoring desired. Load current regulation is provided by fixed off-time pulse-width modulation, so that efficient use of low-voltage inductive loads from higher supplies is practical. Digital status outputs indicate load off, load on, and overload conditions. Latching over-current detection circuitry protects the system from shorts to ground and shorted loads. These parts are available in ceramic or plastic dual-inline packages and heremetic surface-mount chip carriers.

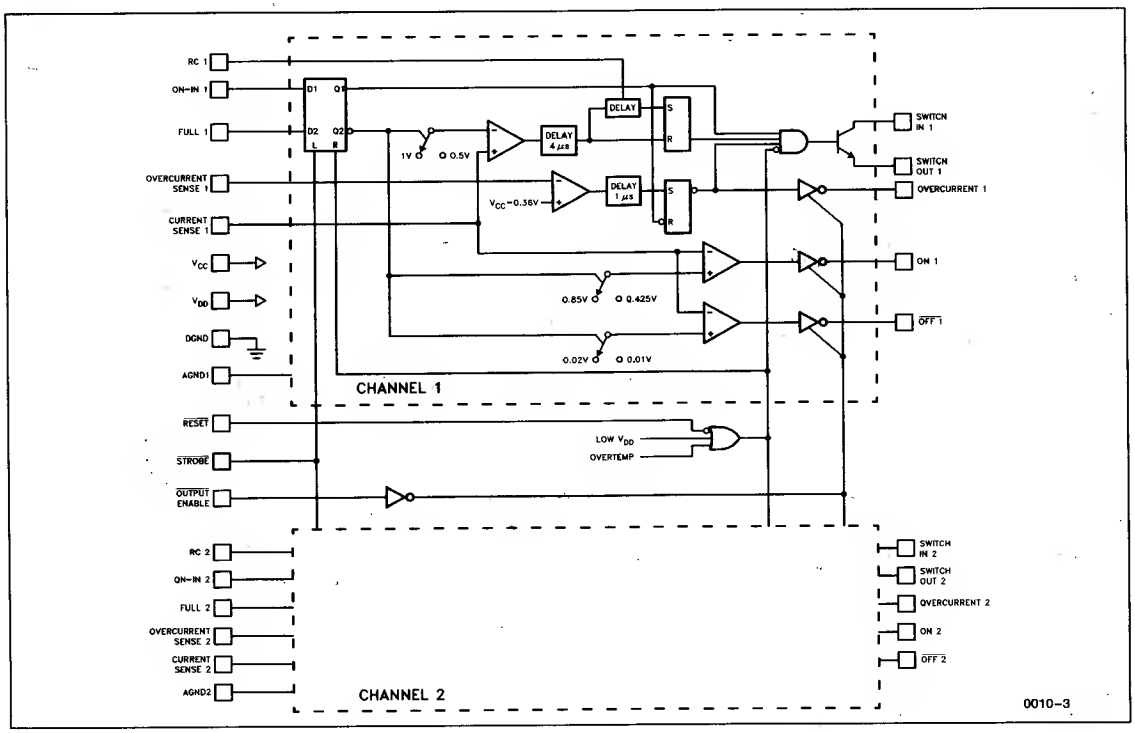
CONNECTION DIAGRAMS

28 PIN-DIL (TOP VIEW)
N or J PACKAGE



0010-1

BLOCK DIAGRAM



0010-3

6

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply over $-55°C < T_A < +125°C$ for the UC1728 and $0°C < T_A < +70°C$ for the UC3728. Unless otherwise stated, $V_{DD} = +5V$, $V_{CC} = +32V$.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
V_{DD} Enable Threshold		3.5	4	4.5	V
V_{DD} Opereting Renge		4.5		5.5	V
V_{DD} Current	$V_{DD} = 5.5V$		12	30	mA
V_{CC} Current	$V_{CC} = 46V$		1.5	6	mA
Logic Input Current	$V_{IN} = 0V$	−50	−5		µA
Current Sense Input Current	$V_{CS} = 0V$	−15	−3		µA
Overcurrent Sense Input Current	$V_{OCS} = V_{CC}$	−10	−1		µA
Logic Input Threshold	$4.5 < V_{DD} < 5.5$	0.8	1.4	2	V
Fault Threshold Overcurrent Sense Input	$13 < V_{CC} < 46$ Meesured to V_{CC}	−0.4	−0.36	−0.32	V
PWM Threshold Current Sense Input	FULL = 1	0.92	1	1.08	V
	FULL = 0	0.45	0.5	0.55	V
ON Threshold Current Sense Input	FULL = 1	780	850	890	mV
	FULL = 0	390	425	450	mV
OFF Threshold Current Sense Input	FULL = 1	10	20	30	mV
	FULL = 0	5	10	15	mV
Switch Drop	I = 200 mA		0.95	1.4	V
	I = 1A		1.05	1.8	V
Switch Leakege	$S_I = 32V$, $S_O = 0V$			200	µA
Logic Output Low	$I_{LOGIC} = 4$ mA		0.2	0.45	V
Logic Output High	$I_{LOGIC} = -4$ mA	2.4	3.3		V
Logic Output Leakage	$0 < V_{LOGIC} < 5V$	−10		10	µA
OFF Time	$R_T = 36k$, $C_T = 1$ nF	15	25	35	µs
Current Sense Delay			4		µs
Overcurrent Sense Deley			1		µs

APPLICATION INFORMATION

In the adjoining figure, one half of the UC1728 is shown in a typical application driving a solenoid. The solenoid current is set by current sense resistor R_S, and programmed by the FULL input as per the following:

FULL = 1 $\quad I_{PEAK} = 1V/R_S$

FULL = 0 $\quad I_{PEAK} = 0.5V/R_S$

The solenoid current will charge up to the programmed peak current at a rate approximately equal to:

$dI/dt = V_{CC}/L$, where L is the load inductance

and coast down at a slower rate for a fixed off-time of about:

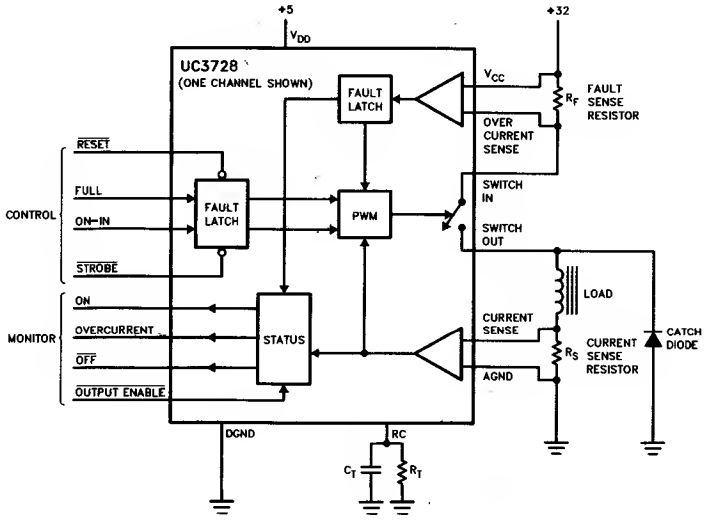
$T_{OFF} = 0.69\ R_T\ C_T$

The slower rate is determined by the series voltage drop in the current sense resistor, the drop in the load resistance, and the Catch Diode voltage working with the load inductance. Typical designs target the PWM frequency over 20 kHz to avoid audible noise. If the duty cycle is less than 50%, the PWM frequency will be controlled by the off time, and an appropriate off time will be around 20 µs.

The overcurrent threshold is set by the fault resistor, R_F. The fault latch will trip when the current in that resistor reaches:

$$I_{FAULT} = 0.36V/R_F$$

The catch diode should be returned to ground rather than R_S so that load current always flows through R_S, making the status information continuously valid through the PWM cycle. Returning the catch diode to ground also produces a more smooth voltage waveform on R_S, which lessens the potential of false triggering the PWM.



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INTEGRATED CIRCUITS

UNITRODE

Thermal Monitor

UC1730
UC2730
UC3730

FEATURES

- On-Chip Temperature Transducer
- Temperature Comparator Gives Threshold Temperature Alarm
- Power Reference Permits Airflow Diagnostics
- Precision 2.5V Power Reference Permits Airflow Diagnostics
- Transducer Output is Easily Scaled for Increased Sensitivity
- Low 2.5 mA Quiescent Current

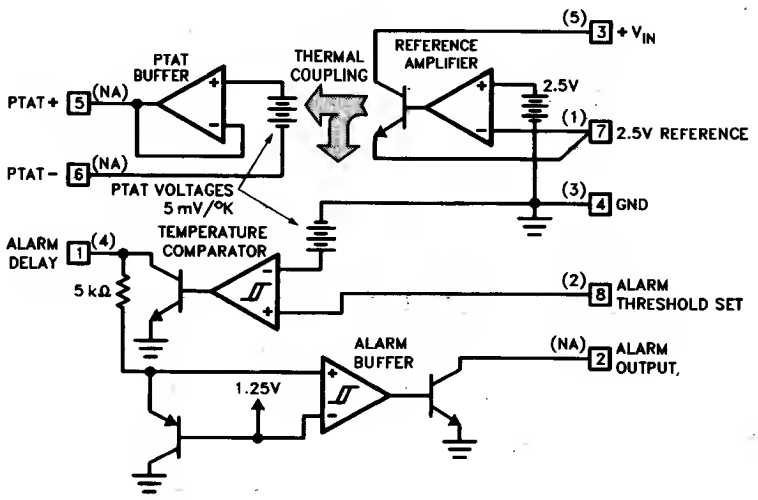
DESCRIPTION

The UC1730 family of integrated circuit devices are designed to be used in a number of thermal monitoring applications. Each IC combines a temperature transducer, precision reference, and temperature comparator allowing the device to respond with a logic output if temperatures exceed a user programmed level. The reference on these devices is capable of supplying in excess of 250 mA of output current—by setting a level of power dissipation the rise in die temperature will vary with airflow past the package, allowing the IC to respond to airflow conditions.

These devices come in an 8-Pin DIP, plastic or ceramic, or a 5-Pin TO-220 version. In the 8-pin version, a PTAT (proportional to absolute temperature) output reports die temperature directly. This output is configured such that its output level can be easily scaled up with two external gain resistors. A second PTAT source is internally referenced to the temperature comparator. The other input to this comparator can then be externally programmed to set a temperature threshold. When this temperature threshold is exceeded an alarm delay output is activated. Following the activation of the delay output, a separate open collector output is turned on. The delay pin can be programmed with an external RC to provide a time separation between the activation of the delay pin and the alarm pin, permitting shutdown diagnostics in applications where the open collector outputs of multiple parts are wire OR'ed together.

The 5-pin version in the TO-220 package is well suited for monitoring heatsink temperatures. Enhanced airflow sensitivities can be obtained with this package by mounting the device to a small heatsink in the airstream. This version of the device does not include the PTAT output or the open collector alarm output.

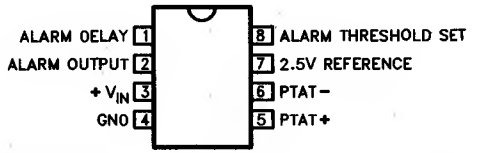
BLOCK DIAGRAM



Pin numbers shown for 8-Pin DIP, ( ) number for 5-Pin TO-220.

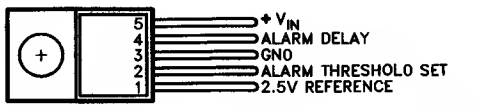
CONNECTION DIAGRAMS

DIL-8 (TOP VIEW)
N or J PACKAGE



0008-1

5-PIN TO-220 (TOP VIEW)
T PACKAGE



0008-2

TAB IS CONNECTED TO GND

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, ($+V_{IN}$) 40V
Alarm Output Voltage (8-Pin Version Only) 40V
Alarm Delay Voltage 10V
Alarm Threshold Set Voltage 10V
2.5V Reference Output Current ..... −400 mA
Alarm Output Current (8-Pin Version Only) ..... 20 mA
Power Dissipation at T_A = 25°C ..... 1000 mW
Derate at 10 mW/°C Above 25°C
Power Dissipation at T_C = 25°C ..... 2000 mW
Derate at 16 mW/°C Above 25°C

Thermal Resistance Junction to Ambient
N, 8-Pin Plastic DIP ..... 110°C/W
J, 8-Pin Ceramic DIP ..... 110°C/W
T, 5-Pin Plastic DIP TO-220 ..... 65°C/W
Thermal Resistance Junction to Case
N, 8-Pin Plastic DIP ..... 60°C/W
J, 8-Pin Ceramic DIP ..... 40°C/W
T, 5-Pin Plastic TO-220 ..... 5°C/W
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note: 1. Voltages are referenced to ground. Currents are positive into, negative out of, the specified terminals.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_j = 0°C to +100°C for the UC3730, −25°C to +100°C for the UC2730 and −55°C to +125°C for the UC1730, $+V_{IN}$ = +5V, and PTAT− = 0V.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	$+V_{IN}$ = 35V		2.8	4.0	mA
	$+V_{IN}$ = 5V		2.3	3.5	mA
REFERENCE					
Output Voltage	T_J = 25°C	2.475	2.5	2.525	V
	Over Temperature	2.46		2.54	V
Load Reguletion	I_{OUT} = 0 to 250 mA		8.0	25	mV
Line Reguletion	$+V_{IN}$ = 5 to 25V		1.0	5.0	mV
TEMPERATURE COMPARATOR					
Tempereture Comparetor Threshold	at 300°K (26.85°C), Nominally 5 mV/°K, V_{INPUT} High to Low	1.475	1.50	1.525	V
Tempereture Error		−10		10	°C
Threshold Line Reguletion	$+V_{IN}$ = 5 to 25V		0.005	0.02	%/V
Tempereture Linearity	Note 2		2.0	5.0	°C
Threshold Hysteresis		3.0	8.0	15	mV
Input Bias Current	V_{INPUT} et 1.5V	−0.5	−0.1		µA
Max Output Current	V_{OUT} = 1V	1.2	3.0		mA
Output Sat Voltage	I_{OUT} = 100 µA		0.05	0.25	V
Output Leakage Current	V_{OUT} = 1V		0.01	1.0	µA

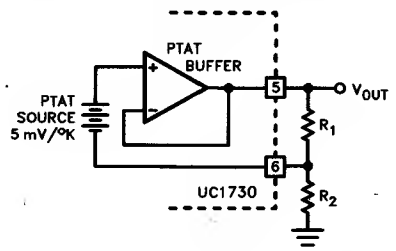
ELECTRICAL CHARACTERISTICS (Continued) (Unless otherwise stated, specifications hold for T_j = 0°C to +100°C for the UC3730, −25°C to +100°C for the UC2730 and −55°C to +125°C for the UC1730, $+V_{IN}$ = +5V, and PTAT− = 0V.) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PTAT BUFFER (8-Pin N, or J Version Only)					
Output Voltage	at 300°K (26.85°C), Nominally 5 mV/°K	1.460	1.50	1.54	V
	In 10X Config. $+V_{IN}$ = 25V	14.6	15	15.4	V
Temperature Error		−12		12	°C
Temperature Linearity (Note 2)			2.0	5.0	°C
Line Regulation	$+V_{IN}$ = 5 to 25V		0.02	0.04	%/V
Load Regulation	I_{OUT} = 0 to 2 mA		1.0	3.0	mV
Dropout Voltage	PTAT+ TO $+V_{IN}$		1.9	2.5	V
Input Bias Current at PTAT− Input		−3.0	−1.0		µA
ALARM BUFFER COMPARATOR (8-Pin N, or J, Version Only)					
Threshold Voltage (V_{th})	Alarm Delay Input Low to High	1.1	1.2	1.3	V
Threshold Hysteresis Voltage	Alarm Delay Voltage > V_{th}		100	250	mV
Input Bias Current	Alarm Delay Voltage < V_{th}		0.1	0.5	µA
Max Output Current	V_{OUT} = 1V	7.0	15		mA
Output Sat Voltage	I_{OUT} = 3 mA		0.25	0.45	V
Output Leakage	V_{OUT} = 35V		0.1	2.0	µA

Note: 2. This parameter is guaranteed by design and is not tested in production.

APPLICATION AND OPERATION INFORMATION

Scaling the PTAT Output (8-Pin Version Only)

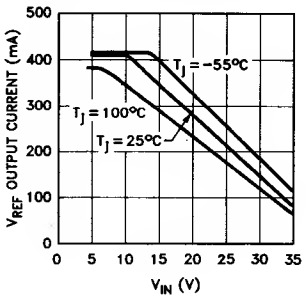


$$V_{OUT} = 5 \times \left(1 + \frac{R_2}{R_1}\right) \text{mV/°K}$$

(Recommended Range for R_1 is 2K to 4K)

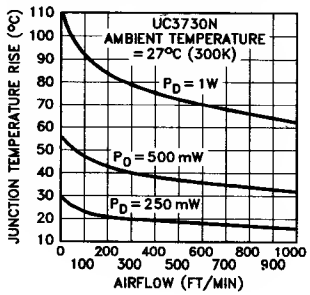
0008-3

V_{REF} Maximum Output Current vs Input Supply



0008-4

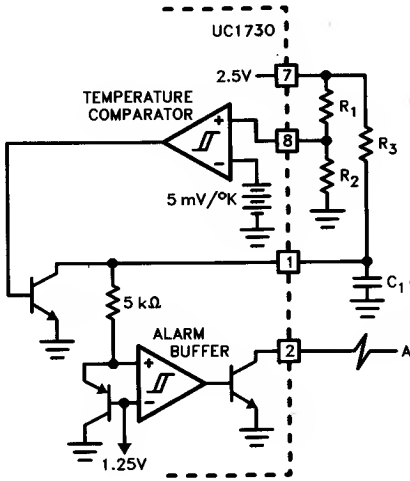
Junction Temperature Rise vs Airflow UC3730N (8-Pin Plastic Dip)



0008-5

APPLICATION AND OPERATION INFORMATION (Continued)

Setting a Temperature Threshold

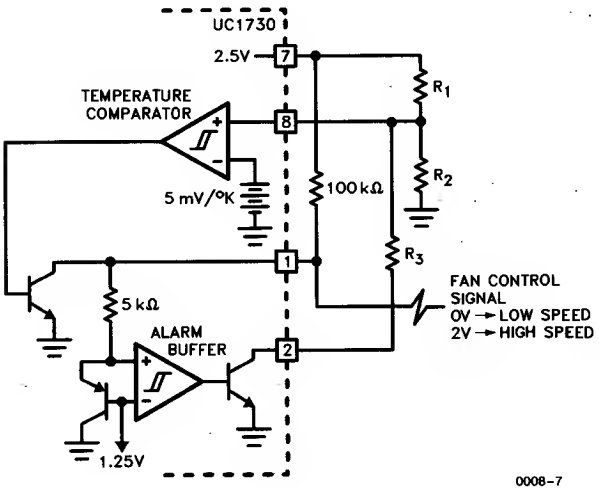


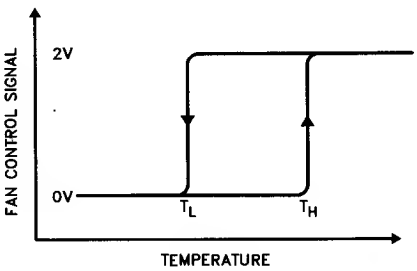
$$\text{Temperature Threshold (°C)} = \left(\frac{2.5V}{0.005}\right) \times \frac{R_2}{R_1 + R_2} - 273.15$$

Note: For airflow monitoring a power dissipation level can be set with a resistive load, R_L, on the reference output. $P_D = (+V_{IN} - 2.5V)^2/R_L$.

0008-6

Dual Speed Fan Control





0008-8

0008-7

$$T_H\,(°C) = \frac{2.5V}{0.005} \times \frac{R_2}{R_1 + R_2} - 273.15$$

$$T_L\,(°C) = \frac{2.5V}{0.005} \times \frac{R_X}{R_1 + R_X} - 273.15$$

$$\text{Where: } R_X = \frac{R_2 R_3}{R_2 + R_3}$$

INTEGRATED CIRCUITS

UNITRODE

UC2950

Half-Bridge Bipolar Switch

FEATURES

- Source or Sink 4.0A
- Supply Voltage to 35V
- High-Current Output Diodes
- Tri-State Operation
- TTL and CMOS Input Compatibility
- Thermal Shutdown Protection
- 300kHz Operation
- Low-Cost TO-220 Package

DESCRIPTION

This device is a monolithic integrated circuit designed to provide high-current switching with low saturation voltages when activated by low-level logic signals. Source and sink switches may be independently activated without regard to timing as a built-in interlock will keep the sink off if the source is on.

This driver has the high-current capability to drive large capacitive loads with fast rise and fall times; but with high-speed internal flyback diodes, it is also ideal for inductive loads. Two UC2950s can be used together to form a full bridge, bipolar motor driver compatible with high frequency chopper current control.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_C ..... 8V to 35V
Output Voltage Range, V_O ..... -3.0V to V_C+3V
Input Voltage Range, V_{IN} ..... -0.3V to +7.0V
Peak Output Current (100ms, 10% DC) ..... ±4.0A
Continuous Output Current ..... ±2.0A
Power Dissipation with Heat Sink 15W
Derate for tab T_C > 75°C ..... 0.2W/°C
Power Dissipation in Free Air 2W
Derate for T_A > 75°C ..... 30mW/°C
Operating Temperature Range, T_A ..... -20°C to +100°C
Storage Temperature Range, T_S ..... -55°C to +125°C

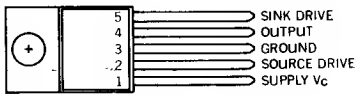
TRUTH TABLE

Source Drive Pin 2	Sink Drive Pin 5	Output Pin 4
Low	Low	Low
Low	High	OFF
High	Low	High
High	High	High

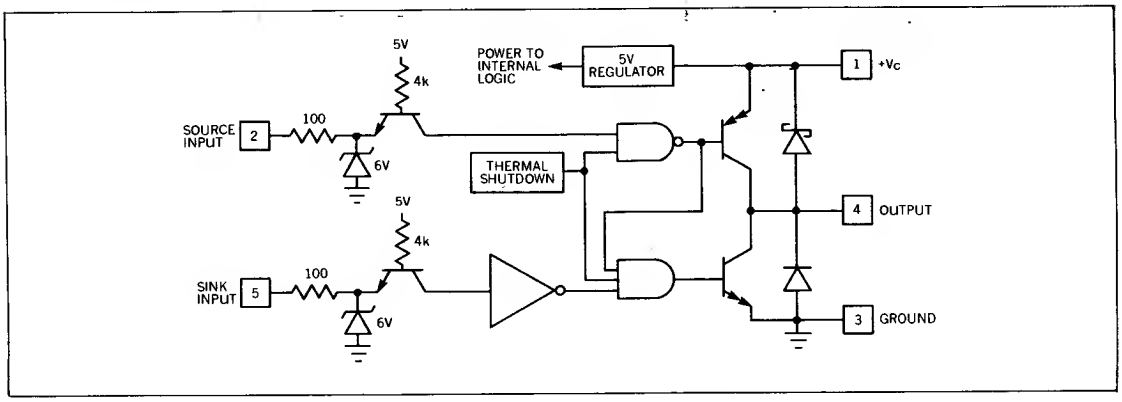
Note: With no load, output voltage will be HIGH in the OFF state.

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T PACKAGE



SIMPLIFIED SCHEMATIC



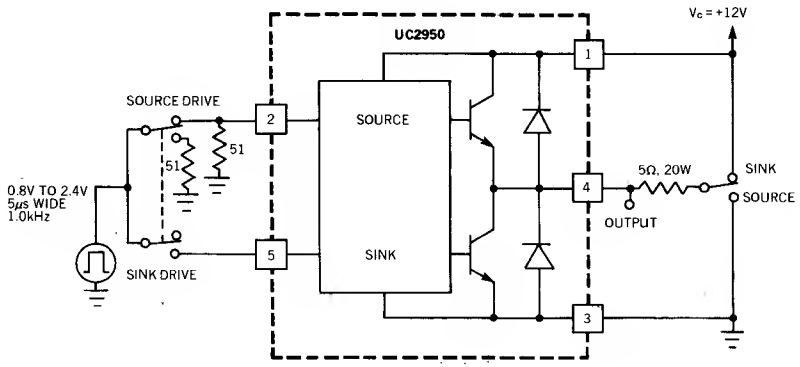
ELECTRICAL CHARACTERISTICS (Unless otherwise stated, V_C = 35V, T_A = −20°C to +100°C, V_{IL} = 0.8V, V_{IH} = 2.4V for either input.) T_A=T_J

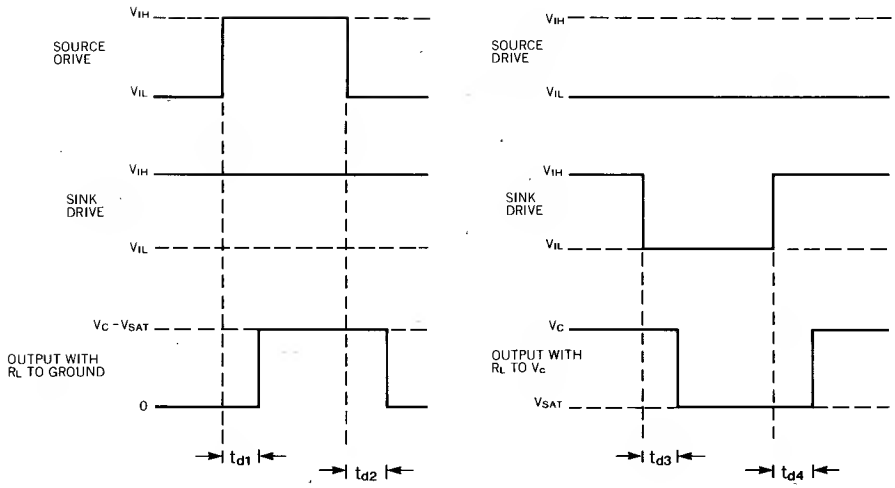
PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Leakage to V_C	Output Off		20	500	μA
Output Leakage to Ground	Output Off		−200	−500	μA
Output Sink Saturation	V_{OL}, I_L = 2.0A		1.2	2.0	V
Output Source Saturation	(V_C−V_{OL}), I_L = −2.0A		1.2	2.0	V
Sink Diode Forward Voltage	I_D = −2.0A		1.4	2.0	V
Source Diode Forward Voltage	I_D = 2.0A		1.4	2.0	V
Input Current	Either Input, V_I = 5V		20	100	μA
Input Current	Either Input, V_I = 0V		−1.0	−1.6	mA
Supply Current	Output High		20	30	mA
Supply Current	Output Low		10	20	mA

SWITCHING CHARACTERISTICS (See Test Circuit. V_C = 12V, R_L = 5Ω, T_A = 25°C. Guaranteed by design, not 100% tested in production.)

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Source Turn-On Delay, t_{d1}		300	500	ns
Source Turn-Off Delay, t_{d2}		1.0	2.0	μs
Sink Turn-On Delay, t_{d3}		200	400	ns
Sink Turn-Off Delay, t_{d4}		100	300	ns
Cross-Conduction Current Spike When Source and Sink are Activated Together		0.6	1.0	μs

SWITCHING TEST CIRCUIT




SOURCE DRIVE
SINK DRIVE
OUTPUT WITH RL TO GROUND
VIH
VIL
VC - VSAT
0
td1
td2
SOURCE DRIVE
SINK DRIVE
OUTPUT WITH RL TO VC
VIH
VIL
VC
VSAT
td3
td4

INTEGRATED CIRCUITS

UNITRODE

UC3657

Triple Tri-State Power Driver

FEATURES

- Operating Supply Voltage to 32V
- Load Current Capability to 3A
- Built-In Thermal Protection
- Clamp Diodes Included for Driving Inductive Loads
- 25W Multiwatt® Power-Tab Package
- Individual Logic Inputs for Each Driver
- Master Inhibit Input for Power-Down and Coast
- TTL/CMOS Compatible inputs

DESCRIPTION

The UC3657 triple power driver integrated circuit is well suited to driving three-phase motors, stepper motors, brush motors, inductors, incandescent lamps, resistive loads and long lines with controlled voltage slew rates. The UC3657 features minimum saturation voltage with light loads as well as low saturation voltage for loads in excess of 2A.

Each output contains two clamp diodes to conduct transient currents from inductive loads. The diode to V_{CC} is a fast, low voltage-drop Schottky type, while the diode to ground is a slower P-N junction device.

The UC3657 is completely safe from destruction due to incorrect combinations of logic inputs. For best performance, however, it is recommended that the inputs are driven with logic signals that have transition times faster than 100nS.

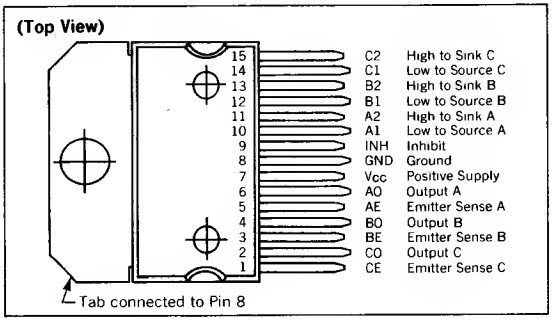
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage 35V
Logic Input Voltage ..... -0.3 to +35V
Peak Output Current (each channel)
  Non-Repetitive 100μS 3A
  Repetitive, 8mS on, 2mS off 2.5A
  Continuous 2A
Total Power Dissipation, T_{TAB} = 75°C 25W
Derate for T_{TAB} > 75°C ..... 0.3W/°C
Storage and Junction Temperature ..... -40°C to +150°C

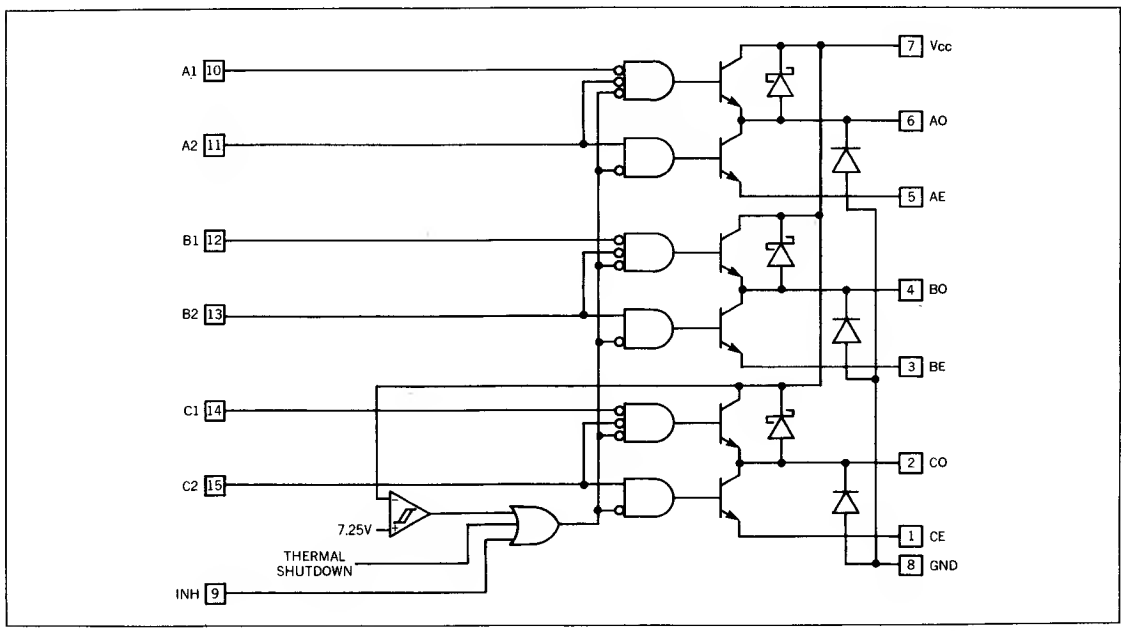
THERMAL DATA

Thermal Resistance, Junction to Case ..... 3°C/W
Thermal Resistance, Junction to Ambient ..... 35°C/W

CONNECTION DIAGRAM



BLOCK DIAGRAM

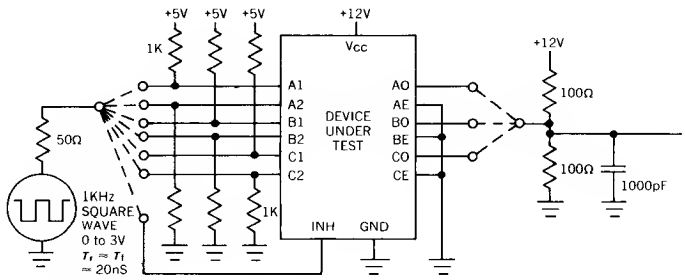


ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C, V_{CC} = 12V unless otherwise noted.) T_A=T_J

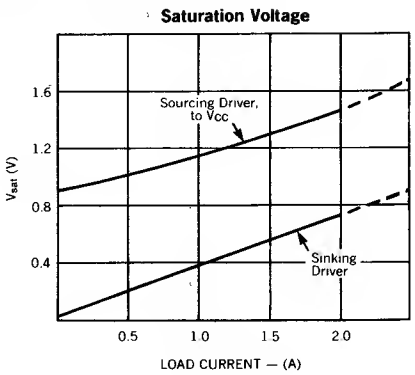
PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Icc, Outputs Off	A1, B1, C1 = H A2, B2, C2 = L INH = L			10	25	mA
Icc, Outputs High	A1, B1, C1 = L A2, B2, C2 = L INH = L			10	28	mA
Icc, Outputs Low	A1, B1, C1 = L A2, B2, C2 = H INH = L			40	70	mA
Icc, Chip Inhibited	INH = H			0.5	5	mA
Icc, One Output Low 2A	A2, B2, C2 = H INH = L			100		mA
V_{CC} Range, Operating			8		32	V
Turn-On Threshold				7.5	8	V
Turn-Off Threshold				7.0		V
Thermal Shutdown Temperature				170		°C
Thermal Recovery Temperature				160		°C
Logic Input Threshold			0.8		2.0	V
Input Low Current; A1, A2, B1, B2, C1, C2	at 0.0V			4	20	μA
Inhibit Low Current; INH	at 0.0V				20	μA
Input High Current; A1, A2, B1, B2, C1, C2	at 3.0V				10	μA
Inhibit High Current; INH	at 3.0V			0.2	1	mA
Output Low Voltage	A2, B2, C2 = H INH = L	100mA		.07	.12	V
	AE, BE, CE Grounded	1A		.37	.75	V
		2A		.7	1.25	V
Output High Voltage, to V_{CC}	A1, B1, C1 = L INH = L	100mA		-.9	-1.3	V
	A2, B2, C2 = L	1A		-1.2	-1.5	V
		2A		-1.5	-1.9	V
Propagation Delay, Off-High	Test Circuit, Drive A1, B1, or C1			.1		μS
Propagation Delay, Off-Low	Test Circuit, Drive A2, B2, or C2			3.2		μS
Propagation Delay, High-Low	Test Circuit, Drive A1+A2, B1+B2, or C1+C2			.25		μS
Propagation Delay, Low-High	Test Circuit, Drive A1+A2, B1+B2, or C1+C2			.51		μS
Propagation Delay, High-Off	Test Circuit, Drive A1, B1, or C1			.4		μS
Propagation Delay, Low-Off	Test Circuit, Drive A2, B2, or C2			.35		μS
Propagation Delay, Low-Inhibit	Test Circuit, Drive INH			1.5		μS
Propagation Delay, Inhibit-Low	Test Circuit, Drive INH			.6		μS
Propagation Delay, High-Inhibit	Test Circuit, Drive INH			2.5		μS
Propagation Delay, Inhibit-High	Test Circuit, Drive INH			.5		μS
Output Slew Rate, Output Rising	100Ω Load to GND; Drive A1+A2, B1+B2, or C1+C2			50		V/μS
Output Slew Rate, Output Falling	100Ω Load to V_{CC}; Drive A1+A2, B1+B2, or C1+C2			50		V/μS
Output Leakage Current	INH = H, V_{CC} = 32V, OV < V_{OUT} < 32V		-250		250	μA
High-Side Diode 2A Drop	INH = H			1.3	2	V
Low-Side Diode 2A Drop	INH = H			1.6	3	V

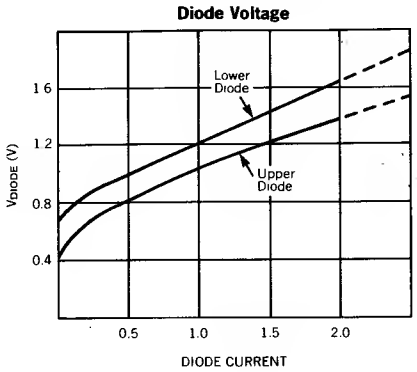
PROPAGATION DELAY TEST CIRCUIT

Connect only one channel at a time.



TYPICAL CHARACTERISTICS, 25°C, 12V



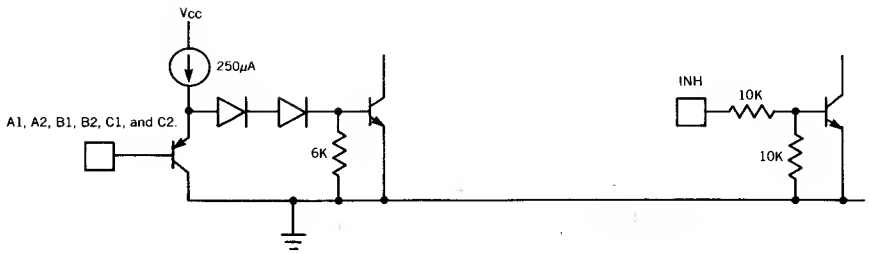


LOGIC TRUTH TABLE

Input 1	Input 2	INH	Output
X	X	H	Off
H	L	X	Off
L	L	L	High
X	H	L	Low

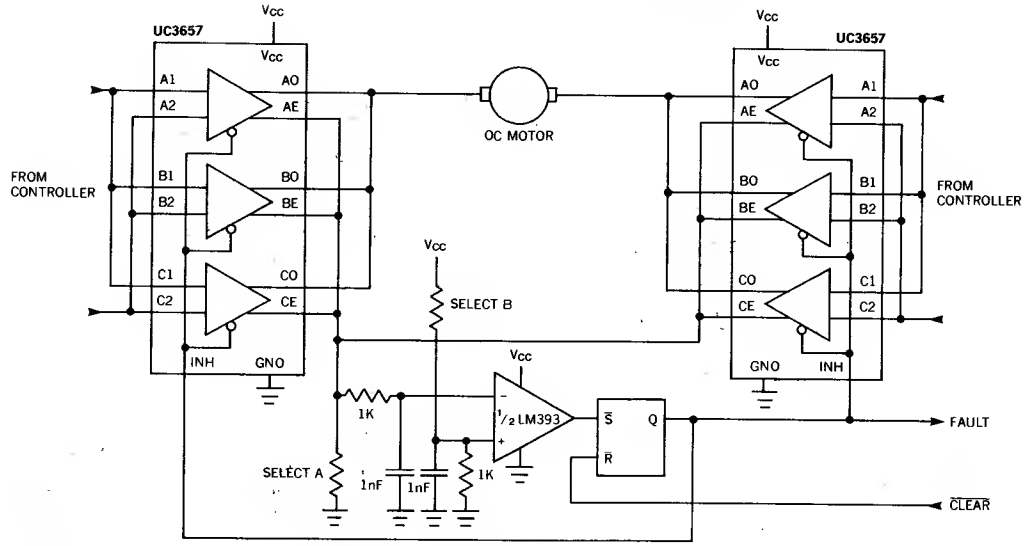
L means input voltage < 0.8V.
H means input voltage > 2.0V.
Off means output is high impedance.
Low means output is low impedance to "E."
High means output is low impedance to "V_{CC}."
X means input voltage will not affect the output (don't care).

EQUIVALENT INPUT CIRCUIT



TYPICAL APPLICATIONS

DC BRUSH MOTOR DRIVER WITH FAULT LATCH



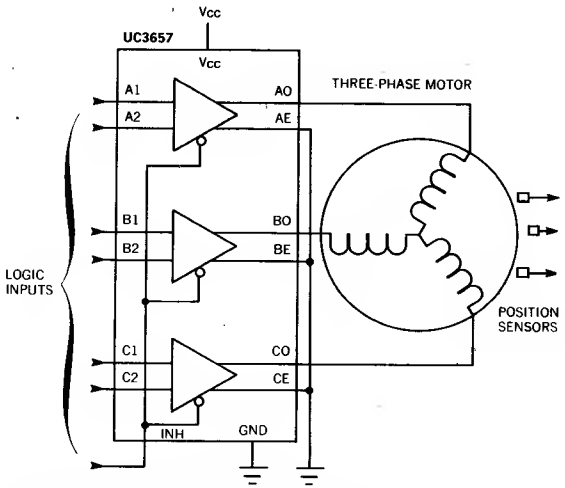
DC Brush Motor Driver with Fault Latch

This application features a fault latch to detect a shorted wire, stuck rotor, or other problem that can cause current to exceed some threshold. A single sense resistor is used with a voltage comparator to detect this fault. Emitter resistor "A" is used to sense total low-side current, and inhibit all devices in the event that current exceeds a threshold. Resistor "B" sets the comparator threshold, and a set-reset flip-flop latches the error signal to prevent oscillation. Matched RC filters on the comparator inputs allow operation close to threshold with good supply-noise rejection.

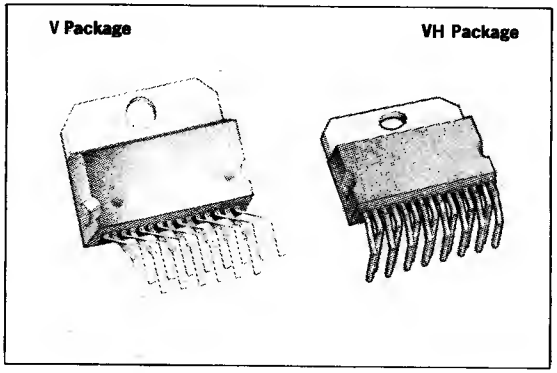
To achieve high currents, UC3657 outputs have been paralleled. This is practical within the device current and power ratings, according to the derating specification for the package.

6

BRUSHLESS MOTOR DRIVER



MECHANICAL DATA



Unitrode Integrated Circuits Corporation
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Telephone 603-424-2410 • FAX 603-424-3460

UC3704

Bridge Transducer Switch

UC3704 COMPATIBLE SENSORS

SENSOR TYPE	ACTIVATION SOURCE						
	Temperature	Pressure	Force	Position	Displacement	Velocity	Shock
Thermistor	X					X	
Sensistor	X					X	
Thermocouple	X						
Semiconductor	X	X	X				
Photo Voltaic				X	X	X	
Photo Resistive				X	X	X	
Strain Gage		X	X	X	X	X	X
Piezoelectric		X	X		X	X	X
Magneto Resistive				X	X		
Inductive				X	X	X	X
Hall Effect				X	X		
Capacitive							X

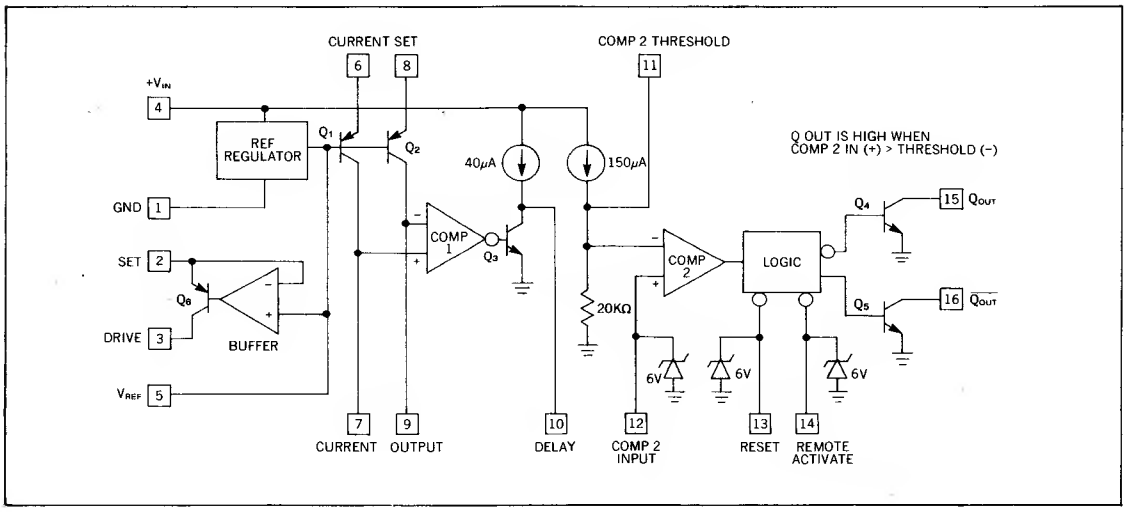
FEATURES

- Dual matched current sources
- High-gain differential sensing circuit
- Wide common-mode input capability
- Complimentary digital open-collector outputs
- Externally programmable time delay
- Optional output latch with reset
- Built-in diagnostic activation
- Wide supply voltage range
- High current heater power source driver

DESCRIPTION

This integrated circuit contains a complete signal conditioning system to interface low-level variable impedance transducers to a digital system. A pair of matched, temperature-compensated current sources are provided for balanced transducer excitation followed by a precision, high-gain comparator. The output of this comparator can be delayed by a user-selectable duration, after which a second comparator will switch complimentary outputs compatible with all forms of logic. This output section can be separately activated for diagnostic operation and has an optional latch with external reset capability. An added feature is a high current power source useful as a heater driver in differential temperature sensing applications. The UC3704 is designed for 0°C to +70°C environments.

BLOCK DIAGRAM



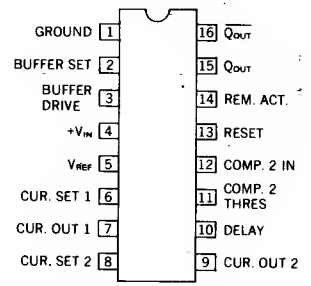
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($+V_{IN}$) 40V
Output Current (each output) 50mA
Buffer Power Source Current 200mA
Comparator 1 Inputs ..... −0.5V to V_{REF}
Comparator 2 Inputs ..... 0 to 5.5V
Remote Activation and Reset Inputs ..... 0 to 5.5V
Power Dissipation at T_A = 25°C 1000mW
Derate at 10mW/°C for T_A > 50°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

NOTE: Unless otherwise specified, all voltages are with respect to ground (Pin 1). Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N PACKAGE



ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704; V_{IN} = 15V) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Inputs					
Supply Voltage Range		4.2		36	V
Supply Current	V_{IN} = 36V		5	10	mA
Reference Section (with respect to V_{IN})					
V_{REF} Value $\lvert V_{IN} - V_{REF} \rvert$	T_J = 25°C	2.1	2.2	2.3	V
V_{REF} Temperature Coefficient	Note 1	−1	−2	−3	mV/°C
Line Regulation	ΔV_{IN} = 4.2 to 25V		2	10	mV
Load Regulation	ΔI_O = 0 to 4mA		2	10	mV
Short Circuit Current	V_{IN} = 36V V_{REF} = V_{IN} or Ground			±25	mA
Current Sources (Q_1 and Q_2)					
Output Current (Note 2)	Current Set = 10μA	−9	−9.5	−10	μA
	Current Set = 200μA	−180	−195	−200	μA
Output Offset Current	R_{E6} = R_{E8} = 20KΩ		0	±1	μA
Comparator One					
Input Offset Voltage			±1	±4	mV
Input Bias Current			−100	−300	nA
Input Offset Current				±60	nA
CMRR	V_{CM} = 0 to 12V	60	70		dB
Voltage Gain	R_L > 150KΩ	70	85		dB
Delay Current Source		34	40	52	μA
Output Rise Time	Overdrive = 10mV, C_D = 15pF, T_J = 25°C		2		V/μs

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704; V_{IN} = 15V) $T_A = T_J$

PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Comparator Two (Q_{OUT} and $\overline{Q_{OUT}}$)						
Threshold Voltage			2.2	3.0	3.8	V
Threshold Resistance	To Ground		14	20	24	KΩ
Input Bias Current	V_{IN} (Pin 12) = 5V			1	3	μA
Remote Activate Current	Pin 14 = 0V			0.2	0.5	mA
Reset Current	Pin 13 = 0V			0.2	0.5	mA
Remote Activate Threshold	T_A = 25°C		0.8	1.2		V
Reset Threshold	T_A = 25°C		0.8	1.2		V
Output Saturation	I_{OUT} = 16mA			0.2	0.5	V
	I_{OUT} = 50mA			0.7	2.0	V
Output Leakage	V_{OUT} = 40V			0.2	10	μA
Output Response	Comp. Overdrive = 1V, R_L = 5K to V_{IN}	Turn-on		0.4		μs
		Turn-off		1.0		
Buffer						
Set Voltage (V_{IN} − V_S)	T_J = 25°C, I_S = 100mA		1.9	2.1	2.3	V
Drive Current	T_J = 25°C, R_S = 200Ω, V_D = 0V		90	100	120	mA

Note: 1. Parameter guaranteed by design, not tested in production.

2. Collector output current = $\frac{V_{IN} - V_{REF} - V_{BE}}{R_E} \approx \frac{1.5V}{R_E}$

APPLICATIONS INFORMATION

Sensor Section

The input portion of the UC3704 provides both excitation and sensing for a low-level, variable impedance transducer. This circuitry consists of a pair of highly matched PNP transistors biased for operation as constant current sources followed by a high gain precision comparator.

The reference voltage at the bases of the PNP transistors has a TC to offset the base-emitter voltage variation of these transistors resulting in a constant voltage across the external emitter resistors and correspondingly constant collector currents. With the emitter resistors external, the user has the option of tailoring the collector currents for balancing, offsetting, or to provide a unique temperature characteristic.

With the PNP transistors' optimum current ranging from 10 to 200μA, and the common-mode input voltage of the comparator usable from ground to (V_{IN} − 3V), a wide range of transducer impedance levels is possible.

The sensor comparator has a current source pull-up at the output so that an external capacitor from this point to ground can be used to provide a programmable delay before reaching the second comparator's threshold. The low-impedance on-state of Comp 1's output provides quick reset of this capacitor. This programmable delay function is useful for providing transient protection by requiring that Comp 1 remain activated for a finite period of time before Comp 2 triggers. Another application is in counting repetitive pulses where a missing pulse will allow Comp 1's output to rise to Comp 2's threshold. This time delay function is:

$$\text{Delay} = \frac{\text{Comp 2 Threshold}}{\text{Delay Current}} \times C_D \approx 175\ \text{ms}/\mu\text{F}$$

If hysteresis is desired for Comparator 1, it may be accommodated by applying positive feedback from the delay terminal to the non-inverting input on Pin 7. This will aid in providing oscillation-free transitions for very slowly changing inputs.

Output Section

The output portion of the UC3704 is basically a second comparator with complimentary, open-collector outputs. This comparator has a built-in, ground-referenced threshold implemented with a high-impedance current source and resistor so that it may be easily overridden with an external voltage source if desired. Comp 2's input transistors are NPN types which require at least 1V of common-mode voltage for accurate operation and should not see a differential input voltage greater than 6V.

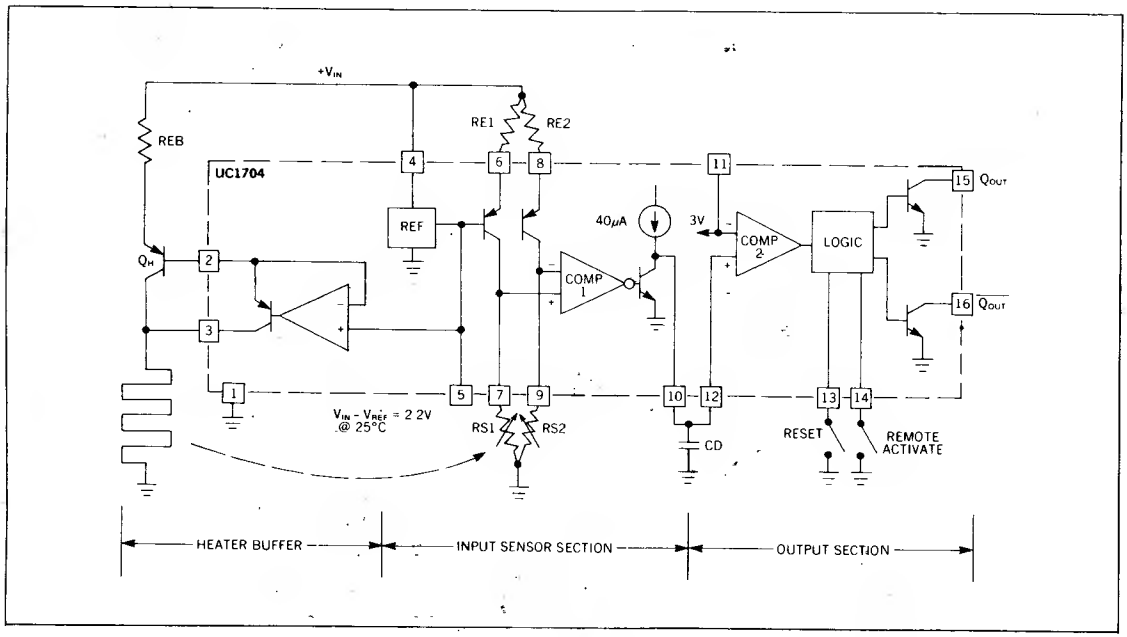
For diagnostic or latching purposes, the output logic is equipped with a Remote Activate and Reset function. These pins have internal pull-ups and are only active when pulled low below a threshold of approximately 1V. A low signal at the Remote Activate Pin causes the outputs to change state in exactly the same manner as if Comp 2's input is raised above the threshold on Pin 11. If Pin 16 is connected to Pin 14, positive feedback results and the outputs will latch once triggered by Comp 2's input. Pulling the Reset terminal low overrides the Remote Activate Pin releasing the latch.

Reference Buffer

This circuit is designed to provide up to 100mA to drive a high-current external PNP transistor useful for powering a heater for differential temperature measurements. Care must be taken that power dissipation in Q_6 does not cause excessive thermal gradients which will degrade the accuracy of the sensing circuitry.

Using a heating element attached to a temperature sensitive resistor, RS1, in one leg of the input bridge implements a flow sensor for either gasses or liquids. As long as there is flow, heat from the element is carried away and the sensor voltage remains below threshold. Using an identical sensor, RS2, without a heater to establish this threshold compensates for the ambient temperature of the flow.

Typical Application For Monitoring Liquid or Gas Flow



6

Five-Channel Programmable Current Switch

FEATURES

- Five Current-Sinking Switches
- Peak Current Programmable from 0.5 to 2.5A
- Internal Current Sensing
- Low-Saturation Outputs Can Block 40V
- TTL Compatible Inputs
- Diagnostic Signal Detects Open Load or Inoperative Switch
- Thermal Sensor Detects Excessive Chip Temperature
- High Power Multiwatt® or Standard DIP Packages

DESCRIPTION

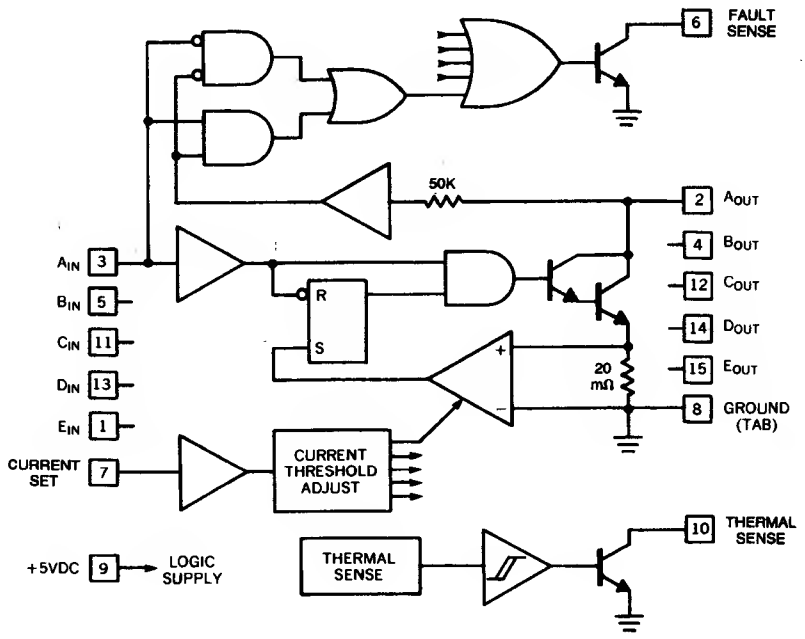
This high-power monolithic circuit consists of five identical, low-side, high-current switches plus a common programmable circuit which sets the peak current limit for all five channels. This current limit threshold—which immediately latches off the power switch when reached—can be programmed over a range of 0.5 to 2.5A. Each switch channel also contains a diagnostic circuit which compares the output response to the input command and provides, on a single fault-sense pin, an indication of a malfunction in either state of any switch. Finally, there is a temperature sensing circuit which switches on when the chip temperature exceeds a value of approximately 160°C. This circuit does not cause shutdown, but provides an indication to the user of an over-temperature condition.

Each current switch is a high-gain grounded-emitter NPN Darlington power device with internal current sensing. This switch is off with the input low and switches on with an input voltage above a two volt threshold. If the current through the switch increases to a value greater than that programmed by the current adjust pin, the switch will be immediately latched off regardless of the input command. Lowering the input signal below threshold will reset the latch allowing the switch to turn on again with the next positive excursion of the input.

The UC3722 is ideal for driving multiple inductive loads such as printer hammers or stepper motor phases to control peak current while providing maximum voltage across the coil. In the Multiwatt package, this device is able to handle up to 25W of internal power dissipation while the DIP package, with only one watt capability, should be considered only for low current and/or low duty cycle applications.

BLOCK DIAGRAM

UC3722
FIVE CHANNEL CURRENT SWITCH



Note: Pin numbers shown for Multiwatt Package

Multiwatt® is a registered trademark of SGS Corporation.

ABSOLUTE MAXIMUM RATINGS

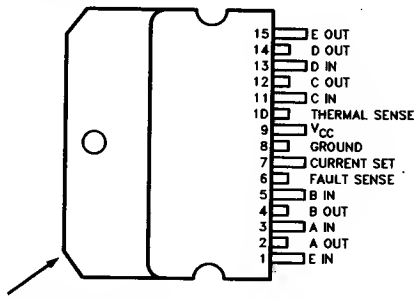
Collector Supply Voltage, V_C ..... +40V
Peak Collector Current, I_O ..... +3.0A
Logic Supply Voltage, V_{CC} ..... +7V
Fault and Thermal Sense Voltage ..... +40V
Fault and Thermal Sense Current ..... +20 mA
Input Signal Voltage, V_{IN} ..... −0.3 to +7.0V
Current Set Voltage ..... 0 to V_{CC}
Multiwatt Power Dissipation (T_{TAB} = +75°C) ..... +25W
Derate for Tab Temperature > +75°C ..... +0.3 W/°C
Dual-In-Line Power Dissipation (T_A = +25°C) ..... +1.0W
Derate for T_A > +25°C ..... +10 mW/°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

THERMAL DATA

Multiwatt Thermal Resistance,
Junction to Case, θ_{JC} ..... +3°C/W
Multiwatt Thermal Resistance,
Junction to Ambient, θ_{JA} ..... +35°C/W
Plastic DIL Thermal Resistance,
Junction to Case, θ_{JC} ..... +50°C/W
Plastic DIL Thermal Resistance,
Junction to Ambient, θ_{JA} ..... +100°C/W

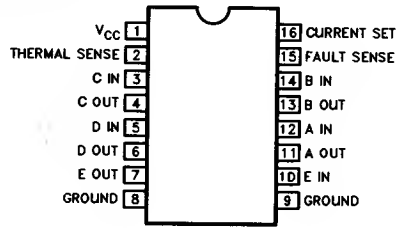
CONNECTION DIAGRAMS

MULTIWATT (TOP VIEW)
VH PACKAGE



Teb connected to Pin 8
Note: Available also in V Package.

DIL (TOP VIEW)
N PACKAGE



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = +5V, V_C = +35V, V_{CS} = V_{CC} = +5V) T_A=T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	V_{CC} = 5V		20	25	mA
Thermel Sense Leakage	V_{TS} = 40V		0.01	10	μA
Thermel Sense Saturetion*	I_{TS} = 5 mA		0.1	0.4	V
Fault Sense Leakage	V_{FS} = 40V		0.01	10	μA
Feult Sense Saturation	I_{FS} = 5 mA		0.1	0.4	V
Current Set Input Bies	V_{CS} = 5V		2	10	μA
Thermal Sanse Activation*			160		°C
Note: The following specifications apply to each channel tested separetely					
Input Bies Current	V_{IN} = 0.4V		−0.2	−0.5	mA
Input Bias Current	V_{IN} = 4.0V		0.2	0.5	mA
Min. Input Turn-On Voltage			2.3	3.2	V
Max. Input Reset Voltage		0.8	1.7		V
Output Saturetion	I_O = 1.0A		1.2	2.0	V
Output Saturation	I_O = 2.5A		1.8	2.5	V
Peak Output Current	V_{CS} = V_{CC}		2.7		A
Peak Output Current	V_{CS} = V_{CC} − 0.5V		1.5		A
Peak Output Current	V_{CS} = V_{CC} − 1.5V		0.5		A
Output Leakage	V_O = 40V		0.2	1.0	mA
Turn-On Deley*	See Test Circuit		100		ns
Turn-Off Delay*			500		ns
Current Shutdown Delay*			200		ns

*This paremeter not 100% tested in production

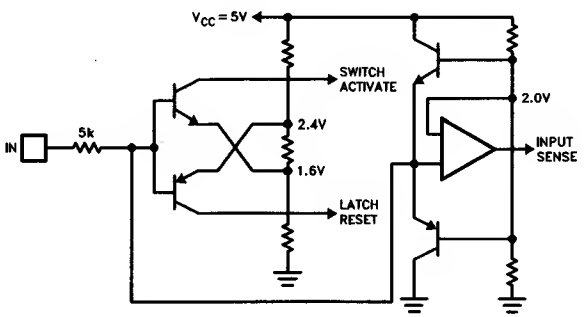
APPLICATION NOTES

1. All threshold levels are developed from, and are therefore proportional to, V_{CC}.
2. Ground is common to all switches and the package heat sink. Switch overlap is allowable but only if the heat sink is electrically connected to a high-conduction ground. In other words, ground current above 3 amps should go through the heat sink rather than pin 8. In the DIL package, maximum peak ground current should be limited to 6 amps.
3. For efficient switching, input signals should have fast transitions (100 ns, or less).
4. The Current Set input is referenced to V_{CC} and is intended for operation with a Set voltage ranging from V_{CC} down to (V_{CC} − 1.5) volts at which point the switch current is clamped to its minimum value. Reducing V_{CS} below (V_{CC} − 1.5) volts will saturate the Current Set internal amplifier and cause the switch current clamp to increase back to its peak value.
5. The Fault Sense logic will indicate a fault by pulling low on its open-collector output. Multiple units can be wire-ORed together merely by connecting together to a common pull-up. The truth table logic is the following:

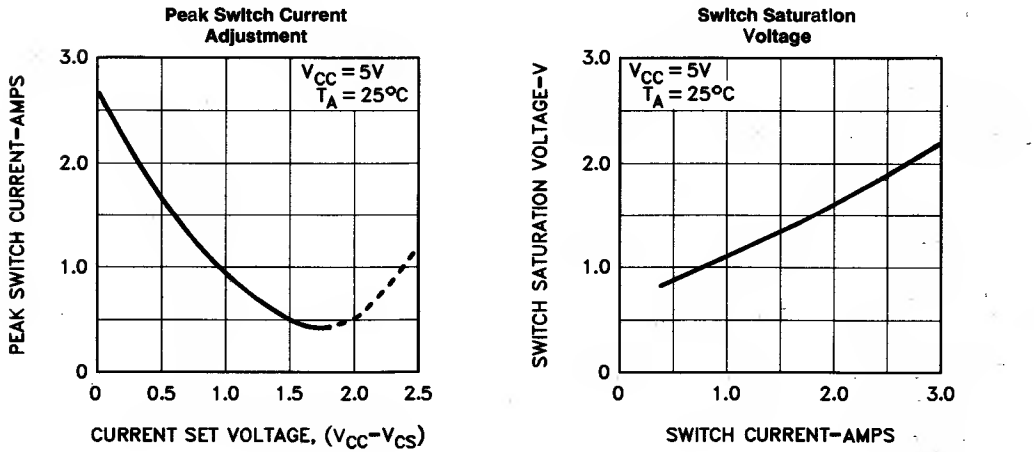
	V_C < 4V	V_C > 4V
V_{IN} > 2.7V	High (Good)	Low (Fault)
V_{IN} < 1.3V	Low (Fault)	High (Good)

   The Fault Signal may need to be externally strobed since, due to switching delays, there will be a short fault condition with every signal transition. In addition, if the current sensing circuit latches the output off while the input remains high, this will show as a fault state.
6. The Thermal Sense output is also open-collector so it can be wire-ORed with other circuitry. The sense circuit has approximately 15° of hysteresis (switch on at approximately 160°C; off at approximately 145°C).

SIMPLIFIED INPUT CIRCUITRY (Each Channel)

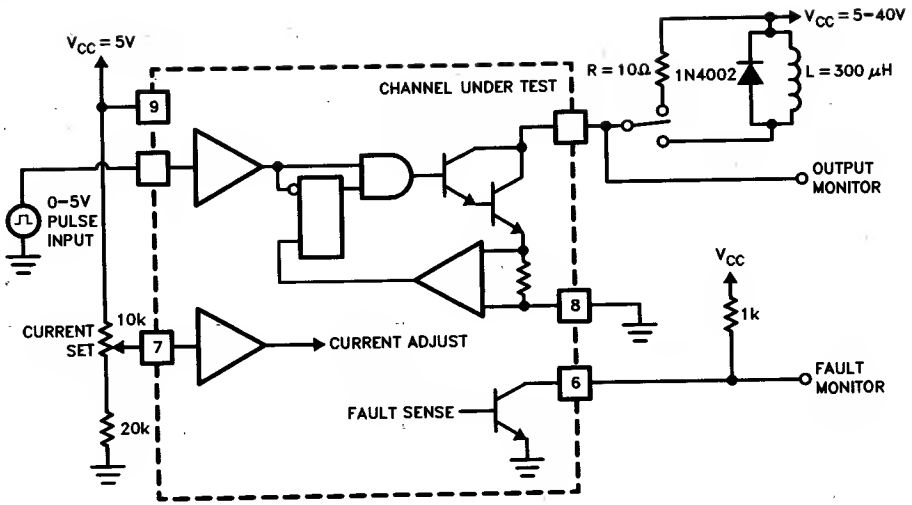


0003-4



0003-5

TEST CIRCUIT



0003-2

6

INTEGRATED CIRCUITS

UNITRODE

Octal Line Driver

UC5170C

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards RS-232D and RS-423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption

DESCRIPTION

The UC5170C is a octal single ended line driver suited for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between SRA (slew rate adjust) and ground. The slew rate and output levels (RS-423A mode) are independent of power supply variations.

RS-423A and RS-232C selection is easily accomplished by taking the mode select pins (M_S+ and M_S-) to ground (RS-423A) or to their respected supplies (RS-232C).

Inputs are compatible with TTL and MOS logic families and are diode-protected against negative transients.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V^+ (Pin 20) 15V
V^- (Pin 11) ..... −15V
PLCC Power Dissipation, T_A = 25°C ..... 1000 mW
  Derate at 10 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 100°C/W
DIP Power Dissipation, T_A = 25°C ..... 1250 mW
  Derate at 12.5 mW/°C for T_A above 50°C
  Thermal Resistance, Junction to Ambient ..... 80°C/W
Input Voltage ..... −1.5V to +7V
Output Voltage ..... −12V to +12V
Slew Rate Resistor ..... 2k to 10 kΩ
Storage Temperature ..... −65°C to +150°C

Note: 1. All voltages are with respect to ground, pin 18.

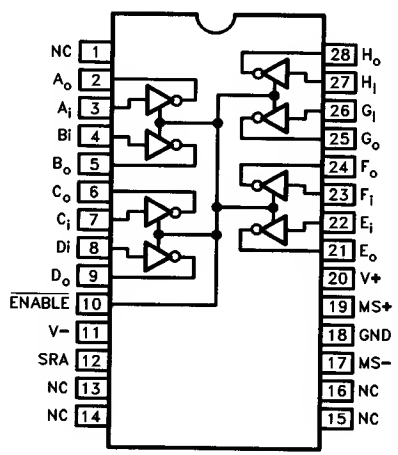
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
$\overline{EN}$	DATA	RS-232C(2)	RS423A
0	0	$(V^+)-3V$	5V to 6V
0	1	$(V^-)-3V$	−5V to −6V
1	X	High Z	High Z

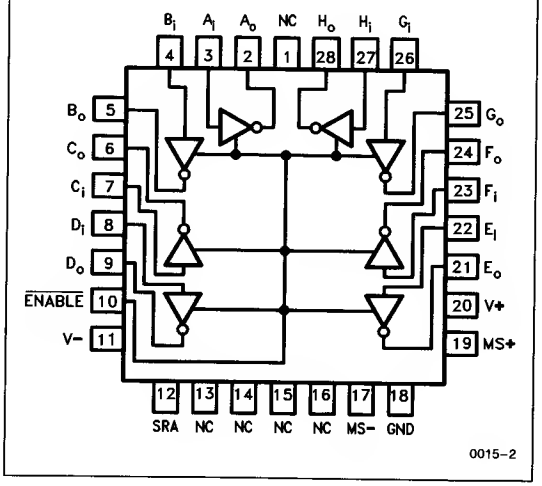
Note: 2. Minimum output swings.

CONNECTION DIAGRAMS

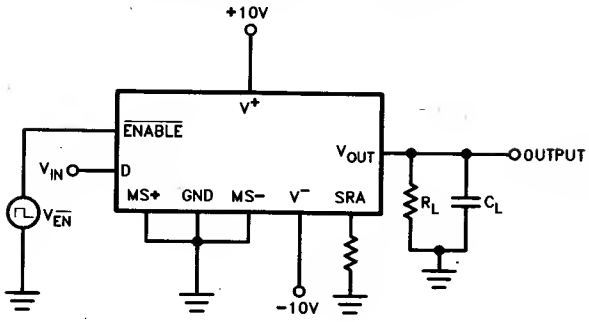
N PACKAGE (TOP VIEW)



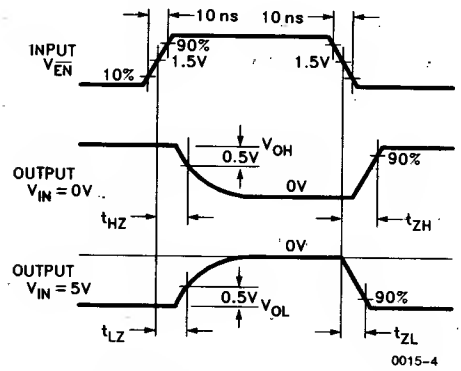
Q PACKAGE (TOP VIEW)



AC PARAMETER TEST CIRCUIT AND WAVEFORMS



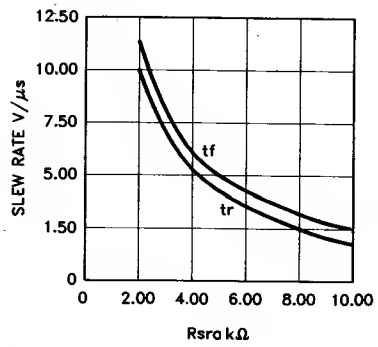
0015-3



0015-4

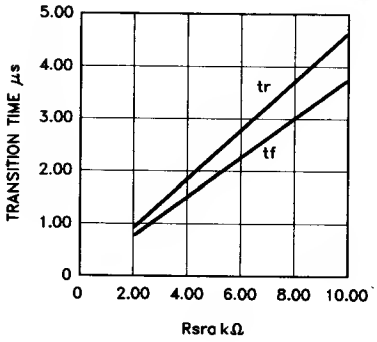
AC CHARACTERISTICS

Driver Slew Rate



0015-5

Driver t_r & t_f (10–90%) RS-423A Mode



0015-6

APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5170C is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10 kΩ which allows slew rates between 10 to 22 V/µs, respectively. The relationship between slew rate and R_{SRA} is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard RS-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 × t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

Output Voltage Programming

The UC5170C has two programmable output modes, either a low voltage mode which meets RS-423A specifications, or the high output mode which meets the RS-232C specifications.

The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supplies, M_{S+} to V^+ and M_{S-} to V^-.

The low output mode provides a controlled output swing and is accomplished by connecting both mode select pins to ground.

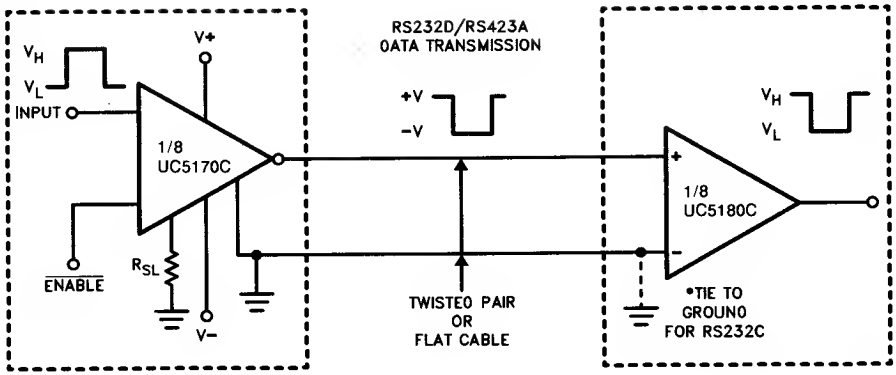
DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated these specifications hold for $|V^+| = |V^-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $R_{SRA} = +10k$) $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V^+ Range			9		15	V
V^- Range			−9		−15	V
V^+ Supply Current	I^+	R_L = Infinite $\overline{En}$ = 0V		25	42	mA
V^- Supply Current	I^-	R_L = Infinite $\overline{En}$ = 0V		−23	−42	mA
INPUTS						
High-Level Input Voltage	V_{IH}		2.0			V
Low-Level Input Voltage	V_{IL}				0.8	V
Input Clamp Voltage	V_{IK}	I_I = −15 mA		−1.1	−1.8	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		0.25	40	μA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	−200	−8.0		μA
OUTPUTS						
High Level Output Voltage (RS-423A)	V_{OH}	V_{IN} = 0.8V R_L = Inf., $\overline{En}$ = 0.8V R_L = 3k, R_L = 450	5.0 5.0 4.5	5.3 5.3 5.2	6.0 6.0 6.0	V V V
Low Level Output Voltage (RS-423A)	V_{OL}	V_{IN} = 2.0V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k R_L = 450	−5.0 −5.0 −4.5	−5.3 −5.6 −5.4	−6.0 −6.0 −6.0	V V V
Output Balance (RS-423A)	V_{BAL}	R_L = 450 $V_{OH} - V_{OL} = V_{BAL}$		0.2	0.4	V V
High Level Output Voltage (RS-232C)	V_{OH}	V_{IN} = 0.8V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k $M_{S+} = V^+, M_{S-} = V^-$	7.0 7.0	7.6 7.6	10 10	V V
Low Level Output Voltage (RS-232C)	V_{OL}	V_{IN} = 2.0V R_L = Inf. $\overline{En}$ = 0.8V R_L = 3k $M_{S+} = V^+, M_{S-} = V^-$	−7.0 −7.0	−7.7 −7.7	−10 −10	V V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, $V_O = \pm 6V$ $V^+ = 15V, V^- = -15V$	−100		100	μA
Short-Circuit Current	I_{OS}	V_{IN} = 0V, $\overline{En}$ = 0V V_{IN} = 5V, $\overline{En}$ = 0V	25 25	50 40		mA mA

AC ELECTRICAL CHARACTERISTICS at $|V^+| = |V^-| = +10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$ $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_r t_f	R_{SRA} = 2k R_L = 450, C_L = 50 pF	6.65 6.65	9.5 10	12.3 12.3	V/μs V/μs
Output Slew Rate	t_r t_f	R_{SRA} = 10k R_L = 450, C_L = 50 pF	1.33 1.33	1.9 2.2	2.45 2.45	V/μs V/μs
Propagation Output to High Impedance	t_{Hz} t_{Lz}	R_{SRA} = 10k, R_L = 450, C_L = 50 pF		0.3 0.5	1.0 1.0	μs μs
Propagation High Impedance to Output	t_{zH} t_{zL}	R_{SRA} = 10k, R_L = 450, C_L = 50 pF		6.0 7.0	15 15	μs μs

APPLICATIONS



0015–7

6

UC5180C

Octal Line Receiver

FEATURES

- Meets EIA 232D/423A/422A and CCITT V.10, V.11, V.28
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35 mA Max
- Input Noise Filter (UC5180C only)
- Internal Hystersis

DESCRIPTION

The UC5180C are octal line receivers designed to meet a wide range of digital communications requirements as outlined in EIA standards 232D, RS422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180C includes an input noise filter and is intended for applications employing data rates up to 200 Kb/s. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

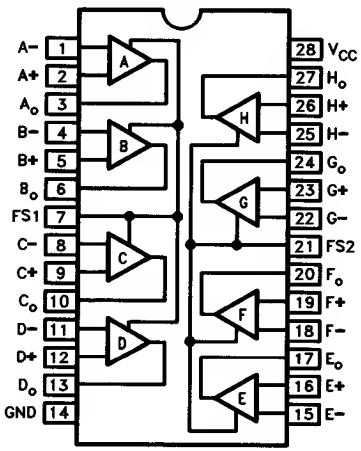
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	7V
Output Sink Current	50 mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to V_{CC}
PLCC Power Dissipation, T_A = 25°C	1000 mW
Derate at 10 mW/°C for T_A above 50°C	
Thermal Resistance, Junction to Ambient	100°C/W
DIP Power Dissipation, T_A = 25°C	1200 mW
Derate at 12.5 mW/°C for T_A above 50°C	
Thermal Resistance, Junction to Ambient	80°C/W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	-300°C

Note 1. All voltages are with respect to ground, pin 8. Currents are **positive into, negative out of the specified terminal**

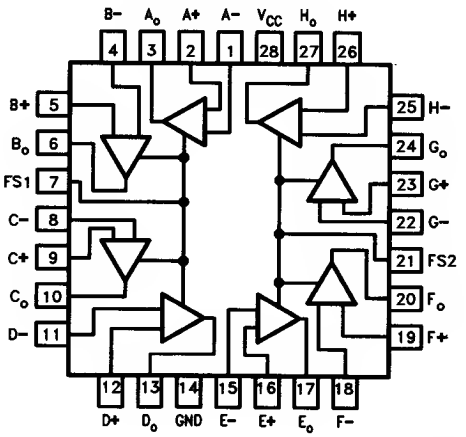
CONNECTION DIAGRAMS

28 PIN DIL



0014-1

28 PIN PLCC

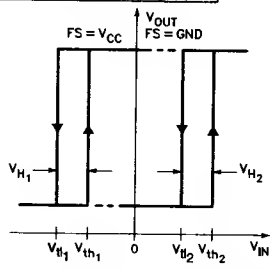


0014-2

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V) $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS		UC5180C MIN	UC5180C MAX	UNITS
DC Input Resistance	R_{IN}	$3V \le \lvert V_{IN} \rvert \le 25V$		3K	7K	Ω
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	$0 \le I_{OUT} \le 8$ mA, $V_{FAILSAFE}$ = 0V		0.45	V
			$0 \ge I_{OUT} \ge -400\ \mu A$, $V_{FAILSAFE} = V_{CC}$	2.7		
Differential Input High Threshold	V_{th}	V_{OUT} = 2.7V, $I_{OUT} = -440\ \mu A$ (See Figure 1)	R_S = 0 (Note 2)	50	225	mV
			R_S = 500 (Note 2)		425	
Differential Input Low Threshold	V_{tl}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 2)	−225	−50	mV
			R_S = 500 (Note 2)	−425		
Hysteresis	V_H	F_S = 0V or V_{CC} (See Figure 1)		50	140	mV
Open Circuit Input Voltage	V_{IOC}				60	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, $I_{OUT} = -440\ \mu A$		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = −1V (Note 3)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 4		20	100	mA
Supply Current	I_{CC}	$4.75V \le V_{CC} \le 5.25V$			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IH} = −10V	−3.25		

Notes: **2.** R_S is a resistor in series with each input.
3. Measured after 100 ms warm up (at 0°C).
4. Only 1 output may be shorted at a time and then only for a maximum of 1 sec.

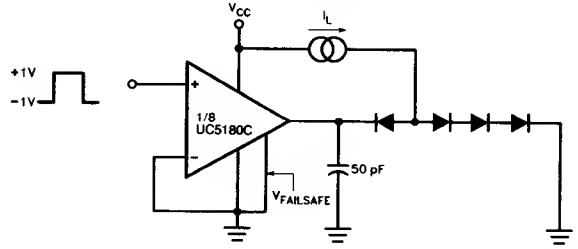


0014-3

Figure 1. V_{tl}, V_{th}, V_H Definition

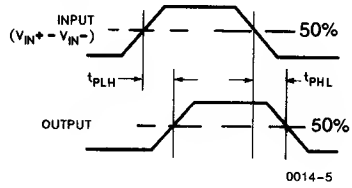
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%, T_A = 0°C to +70°C, Figure 2) $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS	UC5180C MIN	UC5180C MAX	UNITS
Propagation Delay — Low to High	t_{PLH}	C_L = 50 pH, V_{IN} = ± 500 mV		550	ns
Propagation Delay — High to Low	t_{PHL}	C_L = 50 pH, V_{IN} = ± 500 mV		550	ns
Acceptable Input Frequency	f_a	Unused Input Grounded, V_{IN} = ±200 mV		0.1	MHz
Rejectable Input Frequency	f_r	Unused Input Grounded, V_{IN} = ±500 mV	5.5		MHz



0014-4

Figure 2. AC Test Circuit



0014-5

APPLICATIONS INFORMATION

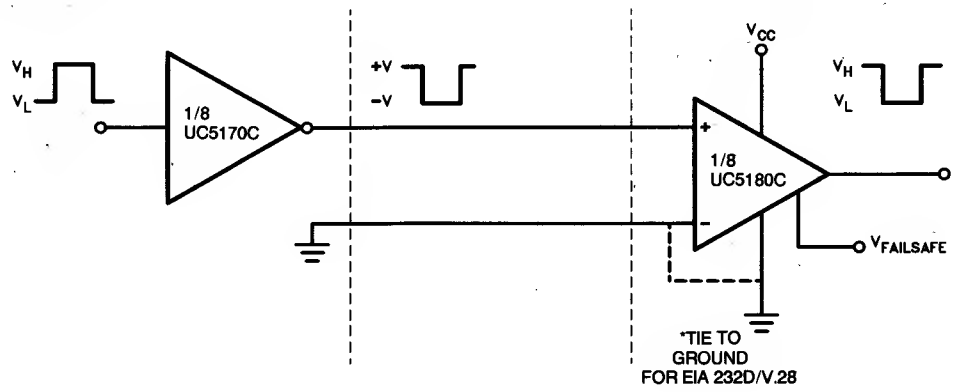
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS422A and RS423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5180C where each provides common failsafe control for four receivers.

Input Filtering (UC5180C)

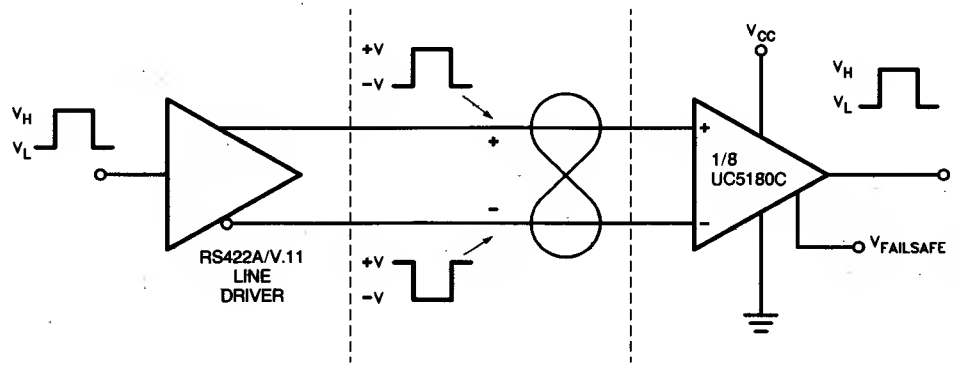
The UC5180C has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output.

EIA 232D/V.28 DATA TRANSMISSION
RS 423A/V.11



0014-6

RS 422A/V.11 DATA TRANSMISSION



0014-7

PACKAGING INFORMATION 7

Device Temperature Management

All circuit components will dissipate some power while operating and this causes their temperature to rise. Unitrode integrated circuits are designed to handle a considerable range of temperatures, but there are limits. Each part is characterized for a particular temperature range, and the user must see to it that the specified limits are not exceeded. This brief note will give a few hints on how to do this.

With the power turned off, all components of a given circuit will be at the same temperature as the ambient air (assuming, of course, that sufficient time has elapsed for all differences to settle). With the power on, the various components will be warmed up due to their internal power dissipation, until a new state of equilibrium is reached. In this state, some devices may be better than others, and the air temperature will also be higher than before, but for each device it will be true that the amount of heat generated internally is equal to the amount of heat removed by the air. In the case of an I.C., for example, heat transfer occurs between the device's case and the air, as well as by conduction through the P.C. board, or heatsink, and from there to the air.

Since all the heat is generated at the silicon chip, it is safe to assume that the chip must be hotter than the IC case; the case must be hotter than the air, or board, or heatsink; and the board or heatsink must be hotter than the air. In short, heat flows downhill, from points of higher temperature to cooler spots.

The rate of heat flow depends on the temperature difference (ΔT) between the two end points, and also on a quantity called "thermal resistance," which is represented by the symbol θ. Heat is a form of energy, and if we choose the joule as the measuring unit, we can specify the rate of heat flow in units of joules per second. Therefore,

$$\textit{Rate of heat flow} = \frac{\Delta T}{\theta} \; [\textit{joules per second}]$$

and since joules per second is the same as watts (W), we have

$$\theta = \frac{\Delta T}{W} \; [^{\circ}C \textit{ per watt}]$$

The quantity θ defines an important property of materials, with the better thermal conductors having the lowest θ values. Since IC chips must be protected by a variety of packages, it is important for the user to know the thermal resistance θ of each type of package, in order to make certain predictions about the thermal behavior of the device in his circuit.

Table 1 shows the following θvalues for Unitrode IC packages:

θ_{JC}: thermal resistance from chip junction to case.

θ_{JA}: thermal resistance from chip junction to air.

The values of θ_{JC} and θ_{JA} given in the table are not necessarily exact numbers, but rather conservative ones, so that by using them, you will tend to err on the side of improved reliability.

You will have noticed that Equation (1) is a sort of "thermal Ohm's law", and that if you know any of the quantities involved, you can calculate the third. With the θ values given in Table 1, you can always calculate the junction temperature by measuring the net input power to the IC.

Now, consider a device such as the UC3620. The data sheet gives us the following Absolute Maximum Ratings:

Total Power Dissipation

(T_{case} + 75°C) 25W
Storage & Junction Temp . . . . . +40°C to + 150°C

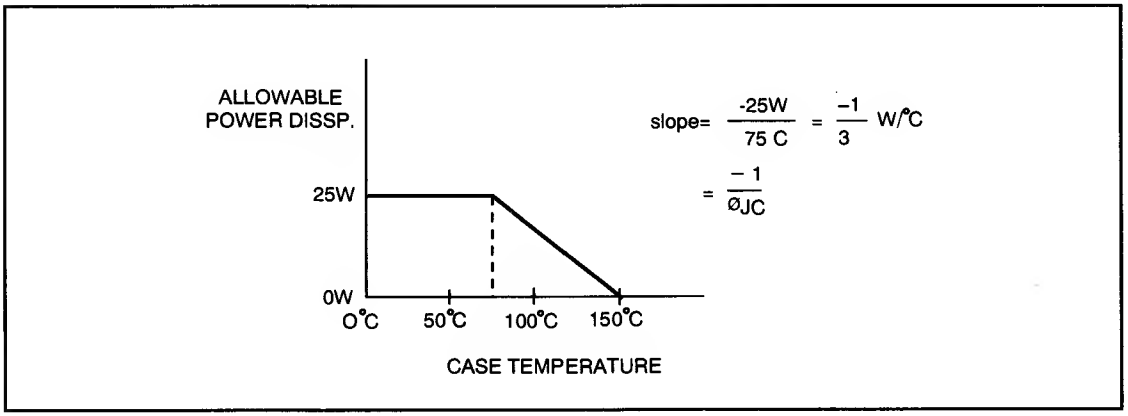
UICC PACKAGE RATINGS

PACKAGE			θjc (°C/W, typ.)	θja (°C/W, typ.)
PACKAGE SUFFIXES	#PINS	DESCRIPTION		
D,DW	14,16,20	SO-IC	N/A	150
G	3	TO-257 Non-Isolated Tab	3.5	42
H	3	TO-39, TO-5	20	130
IG	3	TO-257 Isolated Tab	4.0	42
J	8	Ceramic DIP	40	130
J	14	Ceramic DIP	30	80
J	16	Ceramic DIP	30	80
J	18	Ceramic DIP	5[1] (10[2])	75
JP	16	Ceramic Power	3[1] (6[2])	N/A
JP	24	Ceramic Power	3	35
K	3	TO-3	3	35
L	20	CLCC	15	70
N	8	Plastic DIP	60	125
N	14	Plastic DIP	50	100
N	16	Plastic DIP	50	100
N	18	Plastic DIP	40	90
N	24	Plastic DIP	35	80
N	16	Plastic Batwing	50	80
Q	20	PLCC	N/A	100
Q	28	PLCC	25	80
QP	28	PLCC	15	N/A
R	—	TO-66	5	40
S	—	Side-Braised Cer.	25	90
T	3,5	TO-220	3	60
V	15	Multiwatt®, Vertical Mt.	3	35
VH	15	Multiwatt®, Horiz. Mt.	3	35

Table 1 — Thermal resistance of various Unitrode IC packages. θ_{JC} is the thermal resistance from chip to case, while θ_{JA} is the value from chip to air.

NOTE 1: Junction to bottom plate
NOTE 2: Junction to top plate

We can sketch the curve below:



Although the data sheet does not specifically state the derating factor, we can calculate it from the information given; it is the slope of the line from +75°C +150°C. In this case, the value is — 1/3W/°C at case temperatures above +75°C. We note that the junction temperature anywhere along the curve is +150°C, and since this is the maximum allowable temperature, we must take steps to stay within the area below the curve.

The thermal resistance can be found simply taking the reciprocal of the derating factor. In the case of our UC3620 for example:

θ_{JC} = 3°C/W

which is also the value given in Table 1 for the 15-pin Multiwatt package.

Suppose one intends to use the UC3620 at 2A continuous output current. The data sheet states that the total voltage drop at the output statesis 3.6V maximum. At 2A, this will result in an internal dissipation of 7.2W. If the supply voltage is say, 36V, the quiescent current of 55mA maximum gives us an additional 2W of internal heating, for a total of 9.2W. Furthermore, we decide to provide sufficient cooling to keep the junction temperature at a maximum of 100°C— for increased reliability. Suppose the ambient temperature is to be +50°C maximum. Then, our ΔT is 100°C - 50°C = 50°C, and the required thermal resistance from junction to air will be

$$\theta_{CA} = \frac{50^\circ C}{9.2W} = 5.43^\circ C/W$$

We know already that θ JC =3°C/W. Mounting the IC to a heatsink will result in an additional thermal resistance in series. If you decide to use a mica insulator coated with thermal grease, you insert an additional 0.3°C/W (see any Semiconductor Accessories Catalog). Therefore, we need a heatsink with a θ_{CA} value of

θ_{CA} = 5.43 - 3 - 0.3 = 2.13°C/W

This is the maximum value of thermal resistance between mounting surface and air that will keep the junction temperature at or below the chosen value of 100°C. We need only to go through a heatsink manufacturer's catalog to find a suitable part or extrusion with the required θ_{CA} value.

THERMAL CHARACTERISTICS OF THE QP PLCC POWER PACKAGE

The Plastic Leadless Chip Carrier, or PLCC, surface mount package is a popular alternative for dense printed circuit board design. Unitrode offers many of its products in 20, and 28 pin outlines of this package, denoted by the "Q" suffix. These packages are generally limited to applications where power levels are at, or below, 2 Watts. The growing use of surface mount technology has spawned many applications where higher power levels are required.

The industry's response has been the development of custom, "Power" leadframes. These leadframes offer greatly improved thermal coupling between the power dissipating die and the printed circuit board. Improved thermal coupling is achieved by leaving several of the package's pins directly attached to the die mount pad, thus dedicating these pins as heat transfer paths.

The "QP" package follows a standard 28 pin PLCC outline, and utilizes a power leadframe where pins 12-18 are tied to the die mount pad. The resulting package, has 22 pins available, although the common lead, pins 12-18, are always electrically tied to the substrate of the die. With the added thermal coupling, the package can be used in the 2-4 Watt power range.

The actual power level a device can be used at is highly dependent on the entire, device-package-PC board system. To quantify the thermal characteristics of this system it is best to break the overall thermal resistance into two components, θ_{jb}, (thermal resistance junction to board in °C/Watt), and θ_{ba}, (thermal resistance board to ambient in °C/Watt). The thermal restrictions presented by the package are quantified by the parameter θ_{jb}.

Thermal resistance, junction to board

The junction to board thermal resistance of the "QP" power PLCC package, and for comparison, the standard 28 pin "Q" PLCC package, were measured using a thermal test die and a specially designed PC board. The thermal test die has the ability to dissipate a controlled power level, and also includes a transducer to monitor its own die temperature. The test board was made using "Thermal Clad, Thermal Management Substrate" material from Berquist. It is comprised of a 0.060 inch thick aluminum substrate with a 1 oz. copper interconnect layer electrically isolated from the aluminum with a 2 mil layer of thermally conductive epoxy. The board was layed out with 0.5 square inches of copper under pins 12-18, to thermally couple these pins to the board. This board, with its excellent thermal properties, allowed accurate measurement of the package characteristics.

The thermal resistance of the package to the PC board was measured over a range of power levels. The tests were done with the PC board suspended in a 1 cubic foot enclosure with no air flow. The results, graphed in figure 1, show the typical limiting thermal resistance, θ_{jb}, of the packages to be:

QP power 22 lead package — $\theta_{jb} \doteq 12.5$°C/Watt.

Q standard 28 lead package — $\theta_{jb} = 25.0$°C/Watt.

Thermal resistance, board to ambient

The remaining thermal parameter, θ_{ba}, must be evaluated on a "board-by-board" basis. In order to offer some insight into the characteristics, and tradeoffs, of PC board thermal performance, measurements on various PC board materials, sizes, and configurations were done. An effective thermal resistance from the board to surrounding ambient air was obtained. Some of these results are summarized below.

PC Board:

	area, sq. inches	thickness, inches	material	interconnect layers	Thermal Resistance board to ambient
1	5	0.060	fiberglass	1	θ_{ba} = 25.0°C/Watt
2	5	0.060	aluminum	1	θ_{ba} = 8.0°C/Watt
3	24	0.060	fiberglass	4	θ_{ba} = 13.5°C/Watt
4	5	0.060	fiberglass	1*	θ_{ba} = 11.0°C/Watt
5	5	0.060	fiberglass	1**	θ_{ba} = 16.0°C/Watt

*coupled with an aluminum extrusion to an infinite heatsink. The device was mounted 0.12 inches from the extrusion on the same side of the board

**with 200 FPM of airflow across the board.

All of the above numbers were obtained by suspending the test board, populated with only the test device, in a 1 cubic foot enclosure. The results are useful only as guidelines, and should not be used in place of a rigorous thermal evaluation in a given application.

If we pick case 3 from above as an example, then the total resulting thermal resistance for the "QP" package-board combination will be equal to the sum of the 12.5°C/Watt θ_{jb} and the 13.5°C/Watt θ_{ba}, or 26°C/Watt. For the 28 pin "Q" this number would be 38.5°C/Watt. Using these numbers, maximum power dissipation levels for a standard "Q", and the "QP" packages can be plotted versus ambient temperature as shown in figure 2. In this figure the maximum operating junction temperature is 150°C.

Conclusions

The power level that can be obtained from a surface mount device is predominantly determined by the ability of the package to couple the power to the PC board, the ability of the PC board to dissipate the coupled heat, and the operating conditions of the system. With the power leadframe offered in the "QP" package, the benefit over a conventional PLCC package is about 12.5°C/Watt. The resulting gains in power handling capability will be determined by the remaining variables in the expression for maximum dissipation.

$Pd_{MAX} = (T_{JMax} - T_{amb})/(\theta_{jb} + \theta_{ba})$.

where : T_{JMax} is the maximum operating junction temperature of the device.

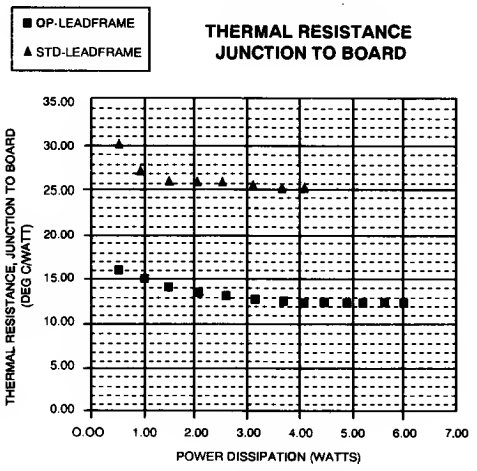


Figure 1: The ability of the package to couple heat to the board is greatly improved in the "QP" package, as shown in this comparison with a standard 28 lead PLCC.

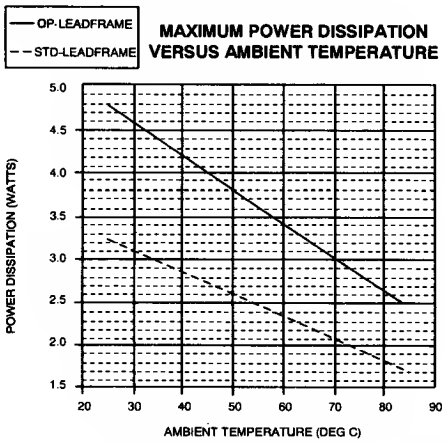


Figure 2: The overall limitation on power handling capability of a surface mount component is determined by the thermal prorperties of the device and PC board, as well as the ambient temperature. In this example the standard "Q" and "QP" packages are compared when mounted on a 4 layer fiberglass PC board.

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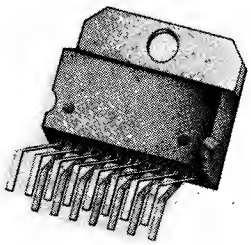
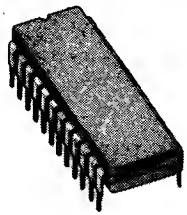
Telephone 603-424-2410 • FAX 603-424-3460

GENERAL INFORMATION

IC Packaging for Power and Size

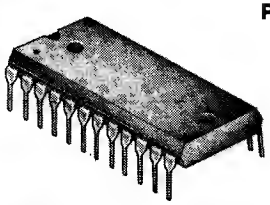


25W
15 Pin
Plastic



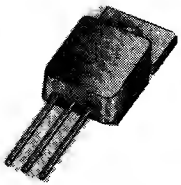
25W
24 Pin DIL
Power Package

10W
16 Pin
Power Package



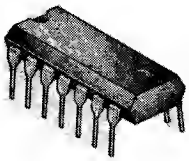
24 or 28
Pin DIL*

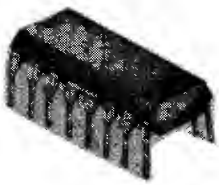
TO-3



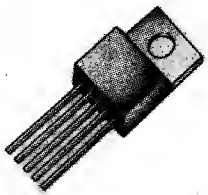
Hermetic
3 Pin
TO-220

1W
14/16/18
Pin*

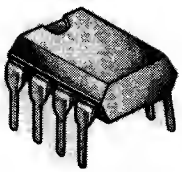




2W
16 Pin
Plastic

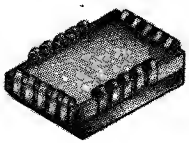


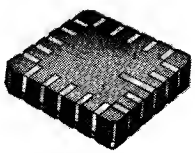
10W
5 Pin
TO-220



8 Pin
Mini
Dip

20 Pin
PLCC*





20 Pin
LCC*

16/20 Pin
SO (300 MIL)

*28 Pin LCC and PLCC also available.

Packaging Information

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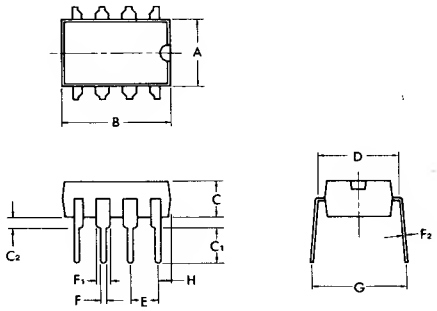
PACKAGING INFORMATION

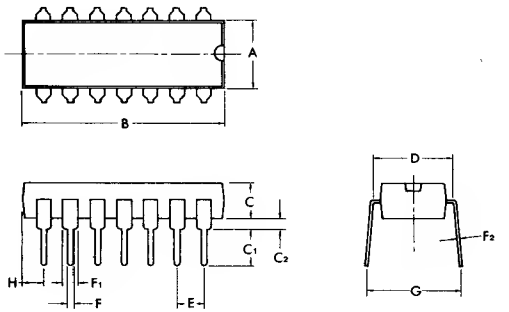
8-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	260	6.22	6.60
B	.370	.400	9.40	10.16
C	.125	.155	3.18	3.94
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.055	1.14	1.40
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.025	.045	0.64	1.14



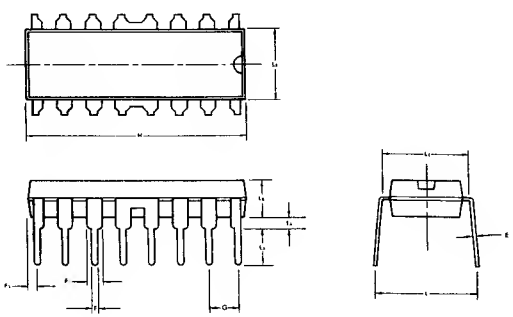
14-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.745	.810	18.92	20.57
C	.120	.140	3.05	3.56
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.065	1.14	1.65
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.065	.085	1.65	2.16



16-PIN PLASTIC POWER
NE PACKAGE SUFFIX

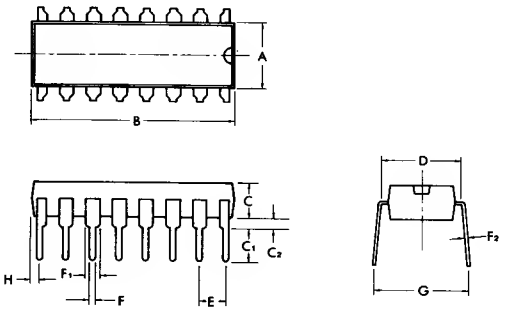
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
E	.008	015	0.20	0.38
F	.015	023	0.38	0.58
F_1	.045	065	1.14	1.65
F_3	025	.063	0.64	1.60
G	090	110	2.29	2.79
H	745	810	18.92	20.57
L	300	.400	7.62	10.16
L_1	290	.310	7.37	7.87
L_2	245	260	6.22	6.60
L_3	015	035	0.38	0.89
L_4	.125	150	3.18	3.81
L_5	.120	140	3.05	3.56



PACKAGING INFORMATION

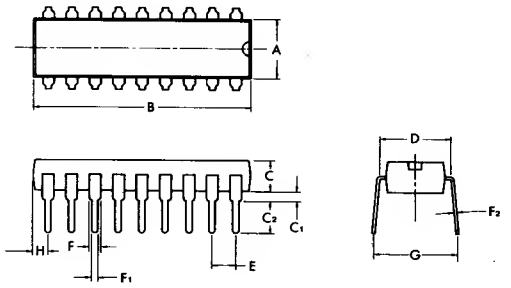
16-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.745	.810	18.92	20.57
C	.120	.140	3.05	3.56
C_1	.125	.150	3.18	3.81
C_2	.015	.035	0.38	0.89
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.015	.023	0.38	0.58
F_1	.045	.065	1.14	1.65
F_2	.008	.015	0.20	0.38
G	300	.400	7.62	10.16
H	.025	.063	0.64	1.60



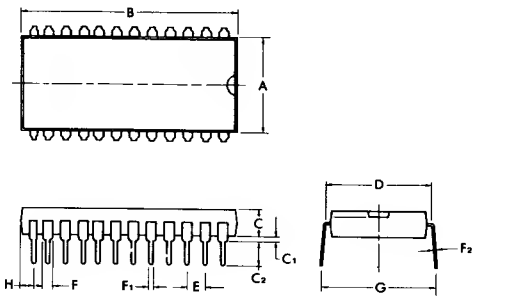
18-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.245	.260	6.22	6.60
B	.890	.920	22.61	23.39
C	.120	.140	3.05	3.56
C_1	.015	.035	0.38	0.89
C_2	.125	.150	3.18	3.81
D	.290	.310	7.37	7.87
E	.090	.110	2.29	2.79
F	.045	.065	1.14	1.65
F_1	.015	.023	0.38	0.58
F_2	.008	.015	0.20	0.38
G	.300	.400	7.62	10.16
H	.055	.080	1.40	2.03



24-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.550	12.70	13.97
B	1.230	1.270	31.24	32.26
C	.150	.160	3.81	4.06
C_1	.015	.035	0.38	0.89
C_2	125	.150	3.18	3.81
D	590	.610	14.99	15.49
E	.090	.110	2.29	2.79
F	.040	.065	1.02	1.65
F_1	.015	.023	0.38	0.58
F_2	.008	.015	0.15	0.38
G	.600	.700	15 24	17.78
H	.065	.085	1.65	2.16



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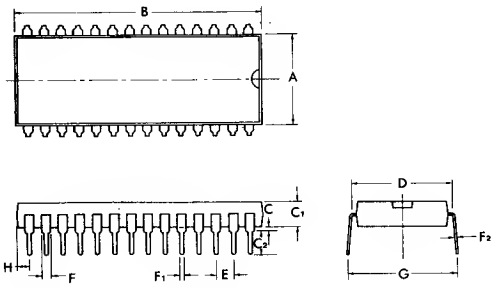
PACKAGING INFORMATION

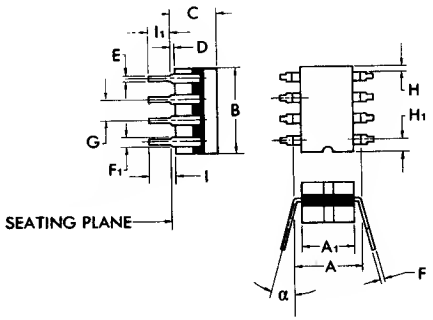
28-PIN PLASTIC
N PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.550	12.70	13.97
B	1.305	1.450	33.15	36.83
C	.015	.035	0.38	0.89
C_1	.140	.180	3.56	4.57
C_2	.125	.150	3.18	3.81
D	.590	.610	14.99	15.49
E	.090	.110	2.29	2.79
F	.040	.065	1.02	1.65
F_1	.015	.023	0.38	0.58
F_2	.008	.015	0.20	0.38
G	.600	.700	15.24	17.78
H	.065	.085	1.65	2.16



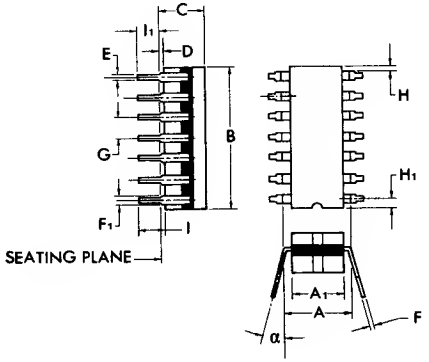
8-PIN CERAMIC
J PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.405	---	10.29
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.055	---	1.35
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



14-PIN CERAMIC
J PACKAGE SUFFIX

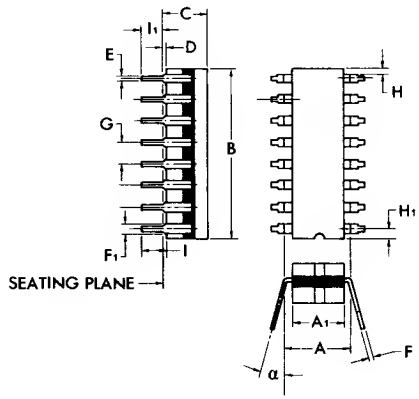
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	---	.785	---	19.94
C	---	.200	---	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.098	---	2.49
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



PACKAGING INFORMATION

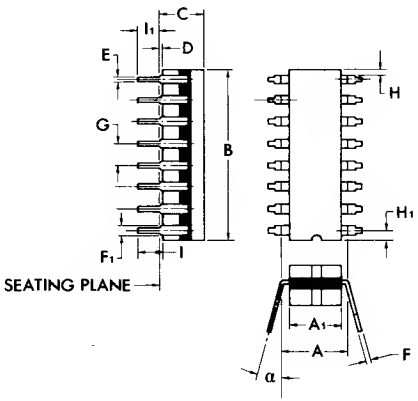
16-PIN CERAMIC J PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	...	.840	...	21.34
C	...	.200	...	5.08
D	.015	.060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.038	.065	0.96	1.65
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	...
H_1	...	.080	...	2.03
I	.150	---	3.81	---
I_1	.125	.200	3.18	5.08
α	0°	15°	0°	15°



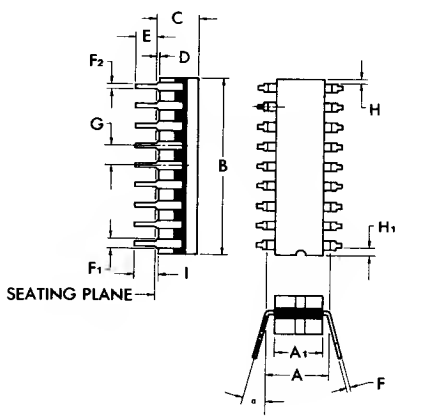
16-PIN CERAMIC POWER J P PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	...	.840	...	21.34
C	...	.200	...	5.08
D	015	060	0.38	1.52
E	.014	.023	0.36	0.58
F	.008	.015	0.20	0.38
F_1	.038	.065	0.96	1.65
G	.100 BSC		2.54 BSC	
H	.005	...	0.13	...
H_1	...	080	...	2.03
I	.150	...	3.81	...
I_1	125	.200	3.18	5.08
α	0°	15°	0°	15°



18-PIN CERAMIC J PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.290	.320	7.37	8.13
A_1	.220	.310	5.59	7.87
B	...	.960	...	24.38
C	...	200	...	5.08
D	015	.060	0.38	1.52
E	.125	.200	3.18	5.08
F	.008	.015	0.20	0.38
F_1	.038	.065	0.96	1.70
F_2	014	.023	0.36	0.58
G	.100 BSC		2.54 BSC	
H	.005	...	0.13	...
H_1	...	098	...	2.49
I	.150	...	3.81	...
α	0°	15°	0°	15°



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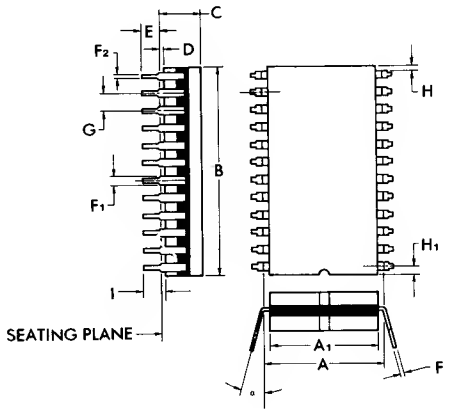
PACKAGING INFORMATION

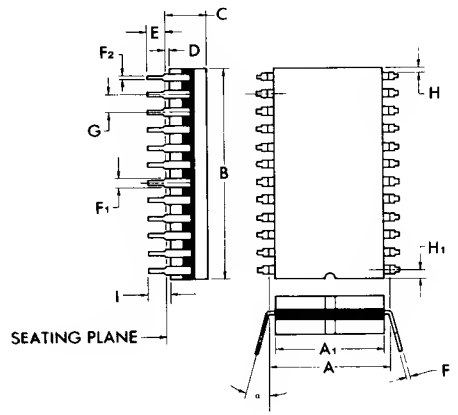
24-PIN CERAMIC J PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.620	12.70	15.75
A_1	.500	.610	12.70	15.49
B	---	1.290	---	32.77
C	---	.225	---	5.72
D	.015	.075	0.38	1.91
E	.120	.200	3.05	5.08
F	008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
F_2	.014	.023	0.36	0.58
G	.100 BSC		2.54 BSC	
H	.005	---	0 13	---
H_1	---	.098	---	2.49
I	.150	---	3.81	---
α	0°	15°	0°	15°



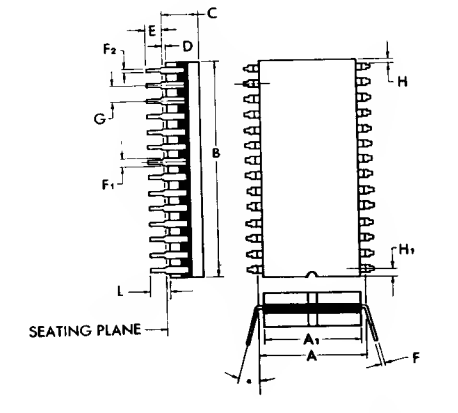
24-PIN CERAMIC POWER J P PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.620	12 70	15.75
A_1	.500	.610	12.70	15.49
B	...	1 290	---	32.77
C	...	.225	...	5.72
D	.015	.075	0.38	1 91
E	.120	200	3.05	5.08
F	.008	.015	0.20	0.38
F_1	.030	.070	0.76	1.78
F_2	.014	023	0 36	0.58
G	.100 BSC		2.54 BSC	
H	.005	---	0.13	---
H_1	---	.098	---	2.49
I	150	---	3.81	---
α	0°	15°	0°	15°



28-PIN CERAMIC J PACKAGE

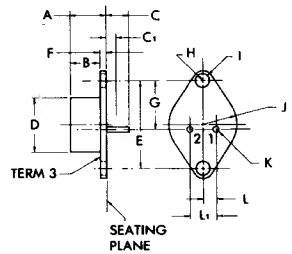
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0 590	0.625	14 99	15.75
A1	0.570	0 605	14 48	15 37
B	1 380	1 460	35 05	37 08
C	0 150	0 190	3.81	5 71
C1	—	0 225	—	5 72
D	0 15	0.070	0 38	1 40
E	0 125	0 200	3.18	5 08
F	0.008	0.015	0.203	0 381
F1	0.050	0.070	1 27	1 78
F2	0.015	0 023	0.38	0.58
G	100BSC		2 54BSC	
H	005	0.0065	0 76	1 65
H1	0.030	0.0065	0.76	1.65
L	0.145	0.245	3.18	4 45
α	0°	15°	0°	15°



PACKAGING INFORMATION

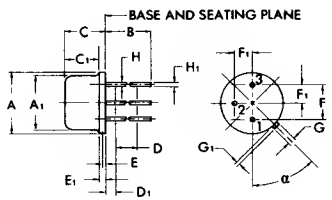
3-PIN TO-3 METAL
K PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.250	.280	6.35	11.43
B	.190	.230	4.83	8.00
C	.430	.470	10.92	11.94
C_1	...	.050	...	1.27
D	.770	.875	19.56	22.26
E	1.177	1.197	29.90	30.40
F	.060	.065	1.52	1.65
G	.655	.675	16.64	17.14
H	.169	.176	4.29	4.47
I	.152	.160	3.89	4.06
J	.495	.505	12.6	12.8
K	.038	.040	0.97	1.02
L	.205	.225	5.21	5.72
L_1	.420	.440	10.67	11.18



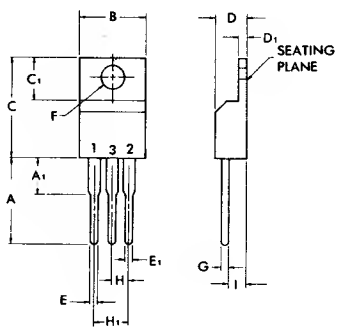
3-PIN TO-5 METAL
H PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
A_1	.305	.335	7.75	8.51
B	.500	...	12.70	...
C	.165	.185	4.19	4.70
C_1	.125	.154	3.18	3.91
D	.152	.165	3.86	4.19
D_1	...	.050	...	1.27
E	.009	.041	0.23	1.04
E_1	...	.050	...	1.27
F	.200 T.P.		5.08 T.P.	
F_1	.100 T.P.		2.54 T.P.	
G	.028	.034	0.71	0.86
G_1	.029	.045	0.74	1.14
H	.016	.019	0.41	0.48
H_1	.016	.021	0.41	0.53
α	45° T.P.		45° T.P.	



3-PIN TO-220 PLASTIC
T PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A_1	...	.250	...	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C_1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D_1	.045	055	1.14	1.39
E	.020	.045	0.51	1.14
E_1	.045	.070	1.14	1.77
F	.139	.147	3.53	3.73
G	.015	.025	0.38	0.64
H	.090	.110	2.29	2.79
H_1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



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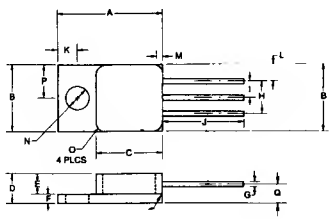
PACKAGING INFORMATION

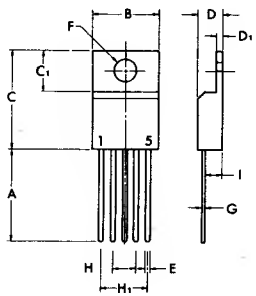
3-PIN TO-257 HERMETIC G PACKAGE

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	.645	.665	16.38	16.64
B	.410	.420	10.41	10.67
C	.410	.430	10.41	10.67
D	.190	.200	4.95	5.48
E	.150	.165	3.94	4.45
F	.035	.045	.089	1.14
G	.027	.033	0.69	0.84
F	.035	.045	089	1.14
G	.025	.035	.069	0.84
H	.015	.025	0.38	0.84
I	.100BSC		2.41	2.67
J	.500	—	12.70	—
K	.115	.121	2.92	3.07
L	.107 REF		2.72 REF	
M	.035	.045	0.89	1.14
N	.140	.150	3.48	3.76
O	.050	.060	1.27	1.52
P	.204	.210	5.16	5.33
Q	120 BSC		—	—



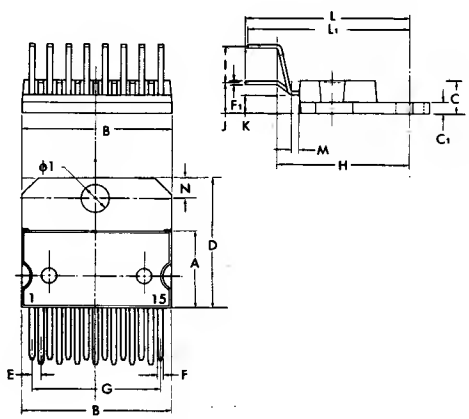
5-PIN TO-220 PLASTIC T PACKAGE SUFFIX

	DIMENSIONS			
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C_1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D_1	.020	.055	0.51	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.012	.045	0.30	1.14
H	...	.134	...	3.40
H_1	...	.268	...	6.81
I	.080	.115	2.03	2.92



15-PIN VERTICAL MULTI WATT V PACKAGE SUFFIX

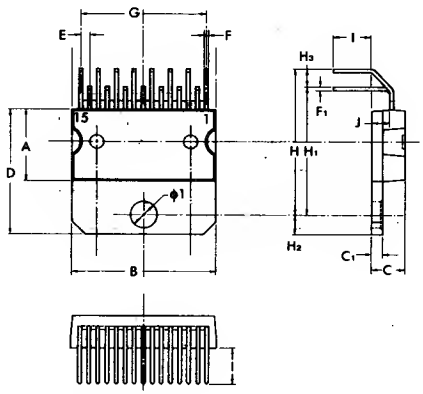
	DIMENSIONS					
SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	.413	.417	.421	10.50	10.80	10.70
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.42	4.50	4.58
C_1	.059	.060	.061	1.49	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.038	.050	.062	0.97	1.27	1.57
F	.026	.028	.029	0.66	0.70	0.72
F_1	.019	.020	.021	0.49	0.52	0.54
G	.688	.700	.712	17.48	17.78	18.08
H	.699	.704	.709	17.75	17.88	18.00
I	.187	.200	.207	4.75	5.08	5.26
J	.163	.169	.175	4.15	4.30	4.45
K	.089	.096	.104	2.25	2.45	2.65
L	.872	.880	.888	22.15	22.35	22.55
L_1	.870	.878	.886	22.10	22.30	22.50
M	—	0.40	—	—	1.00	—
N	.108	.110	.112	2.75	2.80	2.83
ϕ1	.147	.150	.151	3.73	3.80	3.82



PACKAGING INFORMATION

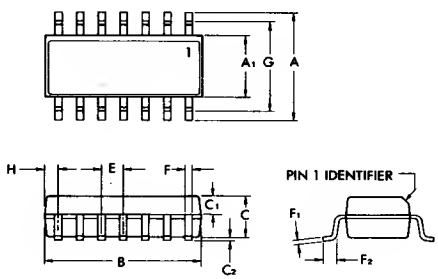
15-PIN HORIZONTAL MULTI WATT HV PACKAGE SUFFIX

SYMBOL	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	.413	.417	.421	10.50	10.60	10.70
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.42	4.50	4.58
C_1	.059	.060	.061	1.49	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.038	.050	.062	0.97	1.27	1.57
F	.026	.028	.029	0.66	0.70	0.72
F_1	.019	.020	.021	0.49	0.52	0.54
G	.685	.700	.712	17.48	17.78	18.08
H	.804	.810	.818	20.42	20.57	20.72
H_1	.707	.713	.719	17.97	18.12	18.27
H_2	.109	.110	.112	2.77	2.80	2.85
H_3	.087	.096	.106	2.20	2.45	2.70
I	.213	.219	.224	5.40	5.55	5.70
I_1	.205	.211	.217	5.20	5.35	5.50
J	.089	.096	.104	2.25	2.45	2.65
$\phi 1$	.147	.150	.151	3.73	3.80	3.83



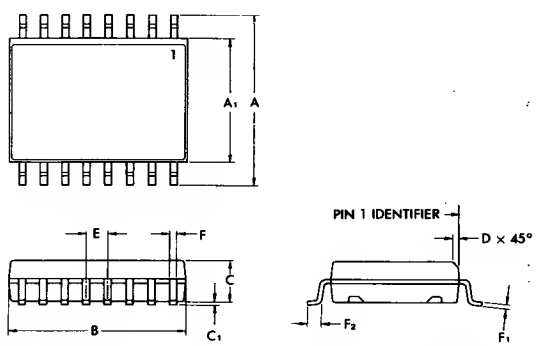
14-PIN PLASTIC SO IC SURFACE MOUNT D PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A_1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C_1	.024	.031	0.61	0.78
C_2	.004	.008	0.10	0.20
D	.015 BSC		0.37 BSC	
E	.050 BSC		1.27 BSC	
F	.014	.018	0.35	0.45
F_1	.007	.009	0.19	0.22
F_2	.025	.030	0.64	0.77
G	.181	.205	4.60	5.20
H	.018	.022	0.45	0.56



16-PIN PLASTIC SO IC SURFACE MOUNT DW PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.410	10.16	10.41
A_1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C_1	.0055	.0115	0.140	0.292
D	.011	.016	0.28	0.41
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
F_1	.010		0.25	
F_2	.018	.035	0.46	0.89



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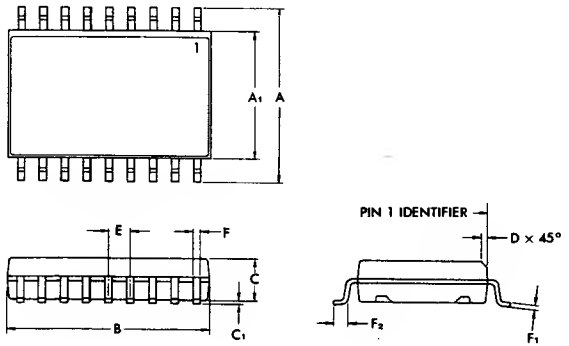
PACKAGING INFORMATION

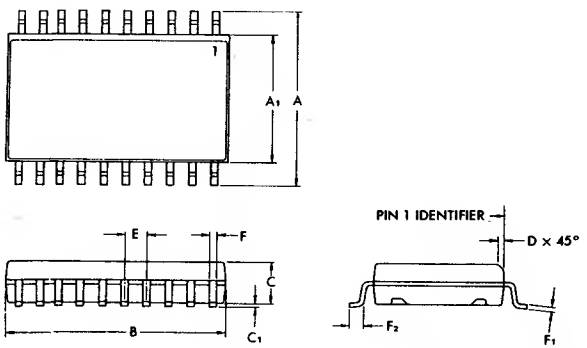
18-PIN PLASTIC SO IC SURFACE MOUNT
DW PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.410	10.16	10.41
A_1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C_1	.0055	.0115	0.140	0.292
D	.011	.016	0.28	0.41
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
F_1	.010		0.25	
F_2	.018	.035	0.46	0.89



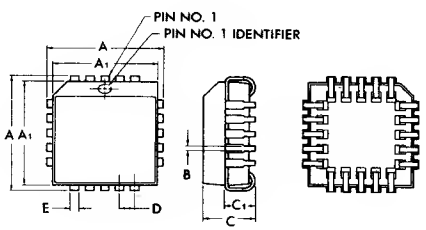
20-PIN SO IC SURFACE MOUNT
DW PACKAGE

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	410	10.16	10.41
A1	.292	299	7.42	7.59
B	504	511	12.80	12.98
C	097	.104	2.46	2.64
C1	0055	0115	0.140	0.292
E	050BSC		1.27BSC	
F	014	.019	0.36	0.48
F1	.010		0.25	
F2	.018	.035	0.46	0.89



20-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE SUFFIX

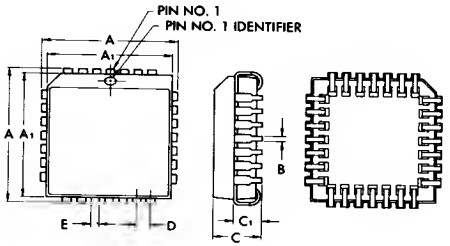
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.385	.395	9.78	10.03
A_1	.350	.356	8.89	9.04
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C_1	.100	.110	2.54	2.79
D	0.50		1.27	
E	.026	.032	0.66	0.81



PACKAGING INFORMATION

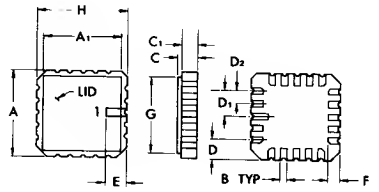
28-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.485	.495	12.32	12.57
A_1	.450	.454	11.43	11.53
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C_1	.100	.110	2.54	2.79
0	.050		1.27	
E	.026	.032	0.66	0.81



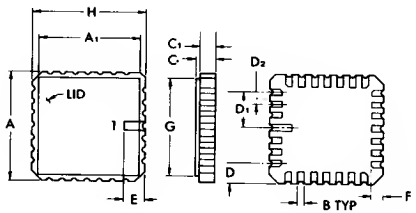
20-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.342	.358	8.69	9.09
A_1	---	.358	---	9.09
B	.022	.028	0.56	0.71
C	.064	.100	1.63	2.54
C_1	.054	.088	1.37	2.24
0	.075 REF		1.91 REF	
0_1	.100 BSC		2.54 BSC	
D_2	.050 BSC		1.27 BSC	
E	.077	.107	1.96	2.72
F	.045	.055	1.14	1.40
G	---	.358	---	9.09
H	.342	.358	8.69	9.09



28-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.442	.460	11.23	11.68
A_1	---	.460	---	11.68
B	.022	.028	0.56	0.71
C	.065	.100	1.63	2.54
C_1	.054	.088	1.37	2.24
0	.075 REF		1.91 REF	
0_1	.150 BSC		3.81 BSC	
0_2	.050 BSC		1.27 BSC	
E	.077	.107	1.96	2.72
F	.045	.055	1.14	1.40
G	---	.460	---	11.68
H	.442	.460	11.23	11.68



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SURFACE MOUNT CONNECTION DIAGRAMS

8

SURFACE MOUNT CONNECTION DIAGRAMS
By Part Number Family

The following pages contain connection diagrams for some of the most requested part number series in standard surface mount packages.

SMD Package Suffix	Description
Q	20 Pin PLCC (Plastic)
Q	28 Pin PLCC (Plastic)
QP	28 Pin Power PLCC (Plastic)
L	20 Pin CLCC (Ceramic)
D	SO-IC (Narrow – Body Plastic)
DW	SO-IC (Wide – Body Plastic)

Please see mechanical data shown in a previous section for package details.

SURFACE MOUNT CONNECTION DIAGRAMS

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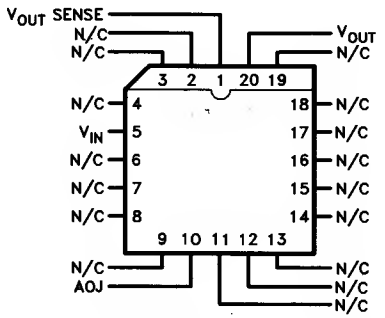

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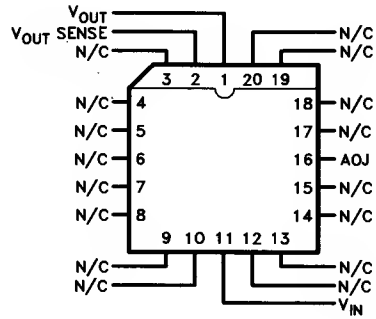

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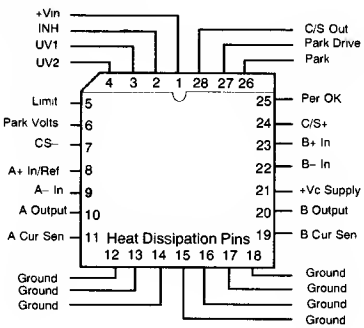

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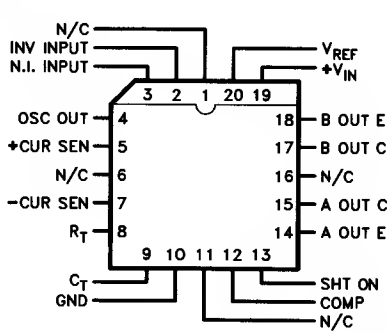

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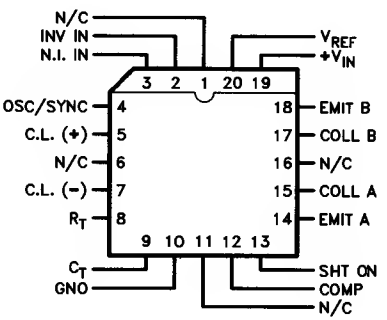

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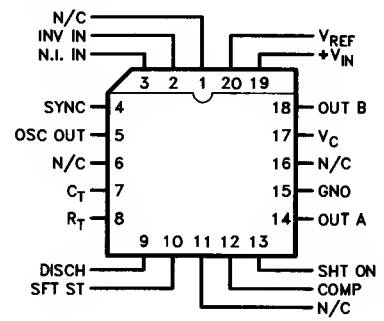

SURFACE MOUNT CONNECTION DIAGRAMS

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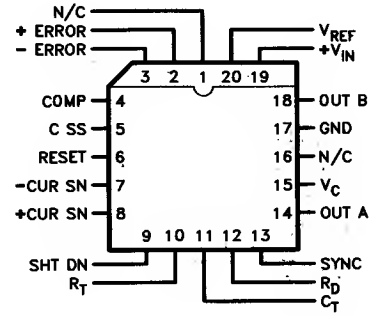

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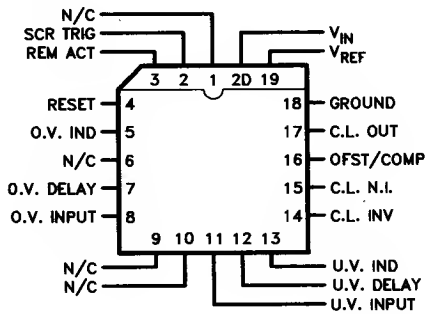

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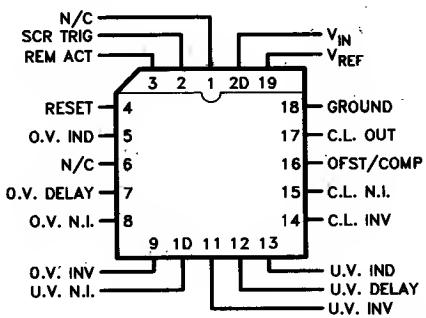

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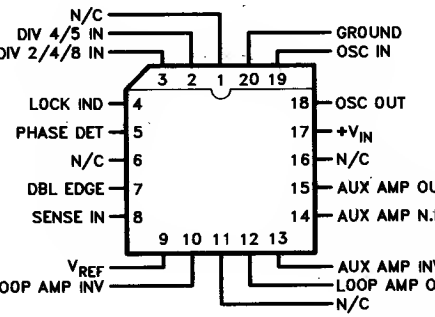

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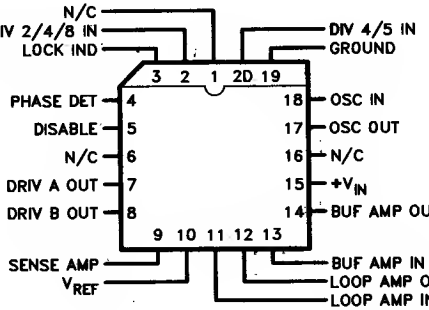

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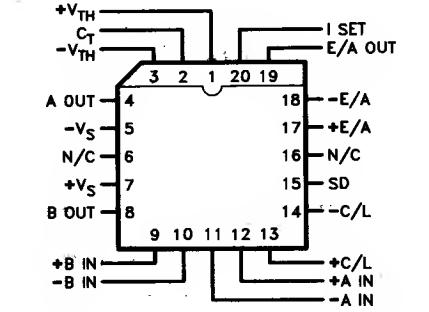

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SURFACE MOUNT CONNECTION DIAGRAMS

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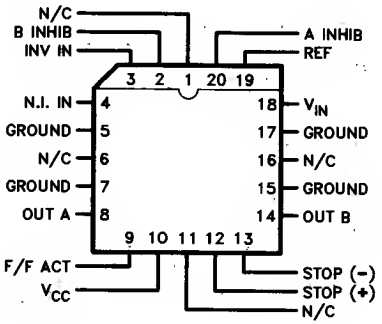

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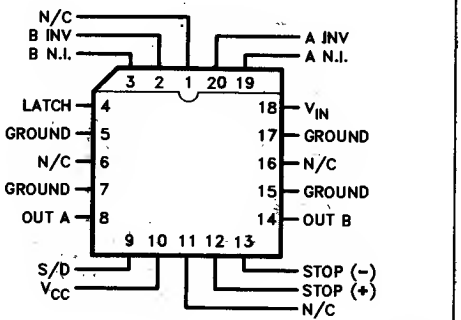

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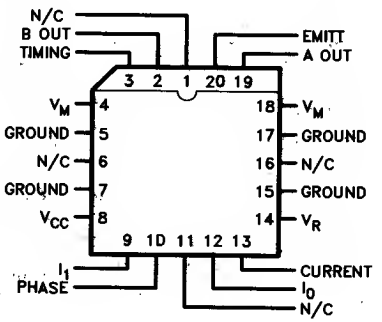

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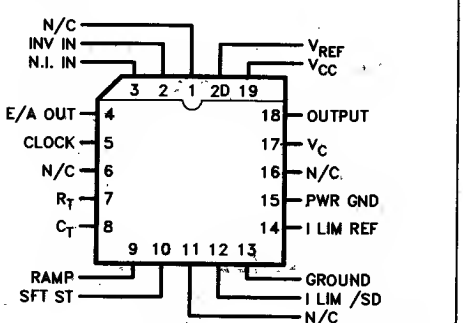

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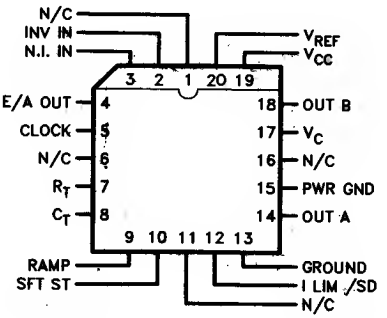

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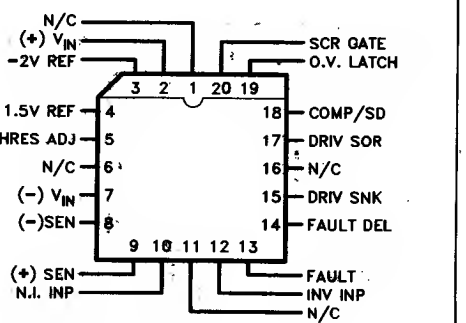

SURFACE MOUNT CONNECTION DIAGRAMS

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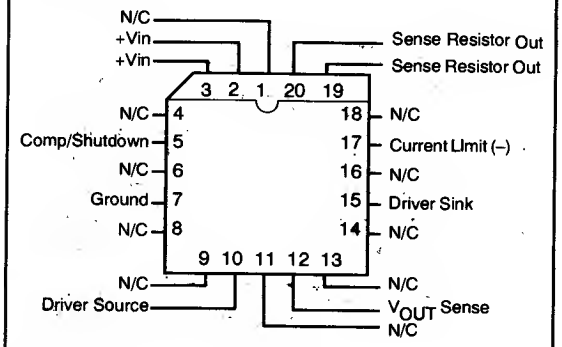

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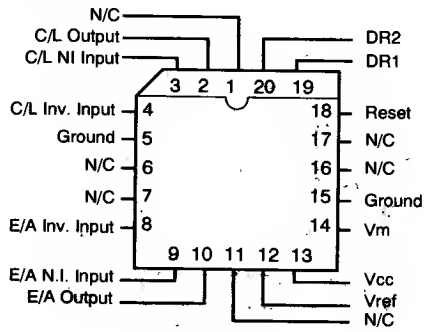

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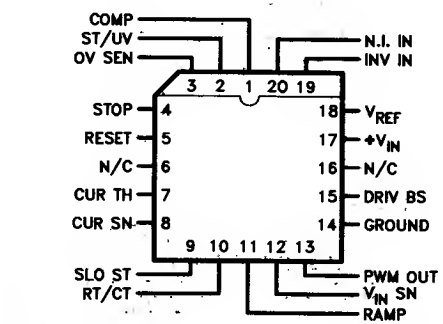

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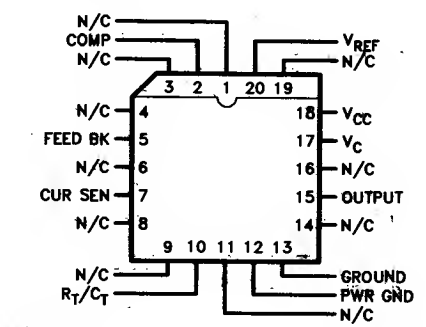

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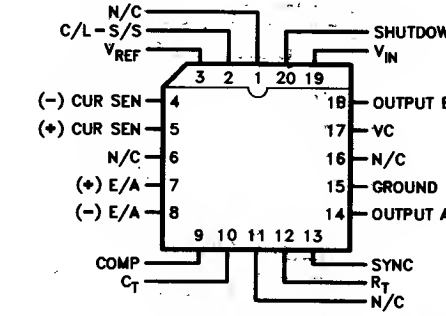

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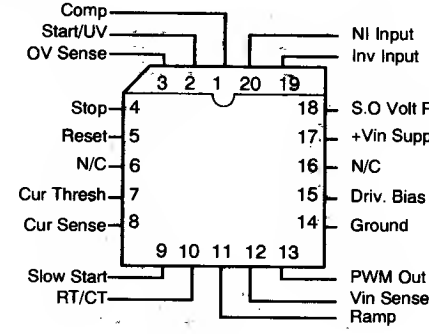

8

SURFACE MOUNT CONNECTION DIAGRAMS

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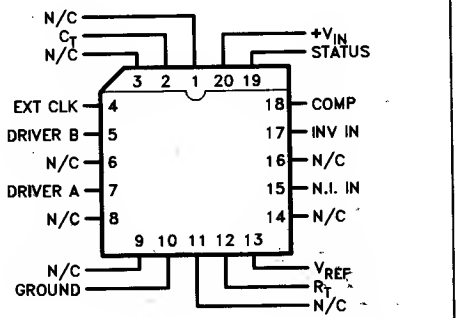

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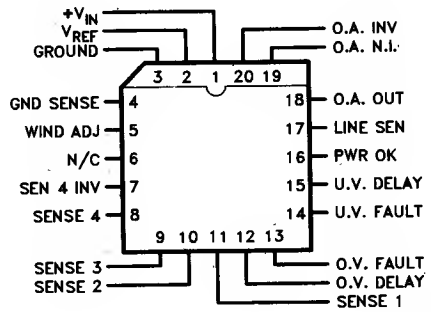

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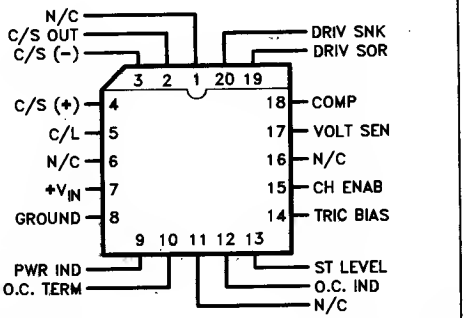

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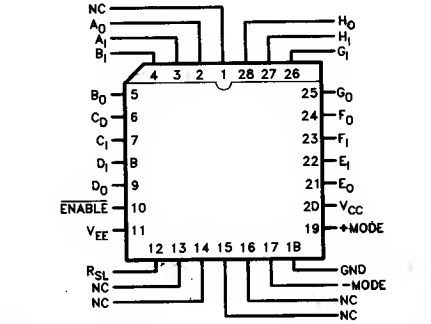

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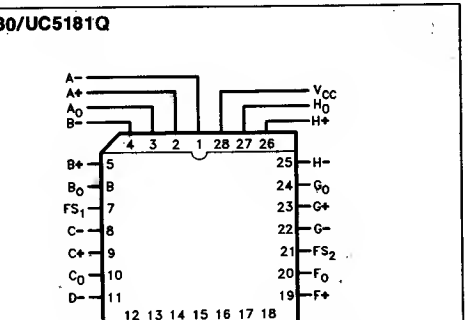

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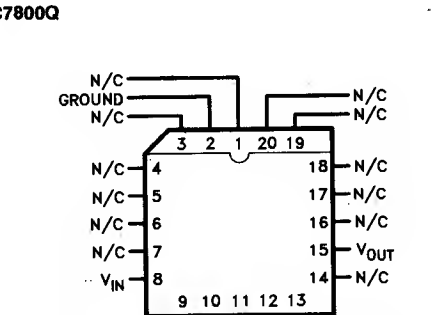

SURFACE MOUNT CONNECTION DIAGRAMS

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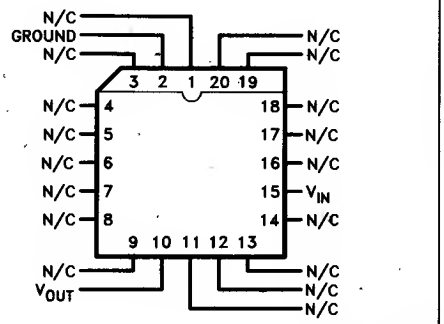

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Military Surface Mount Connection Diagrams

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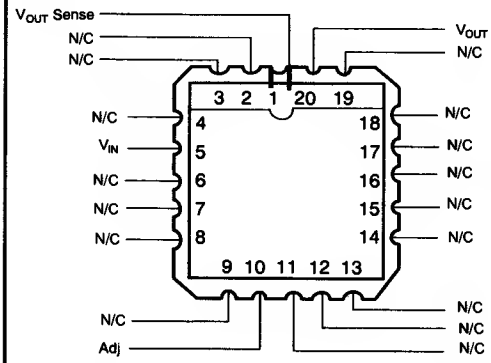

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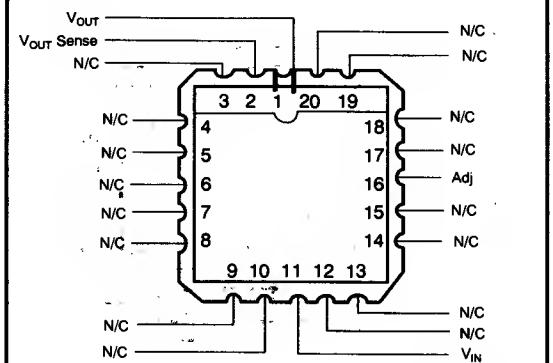

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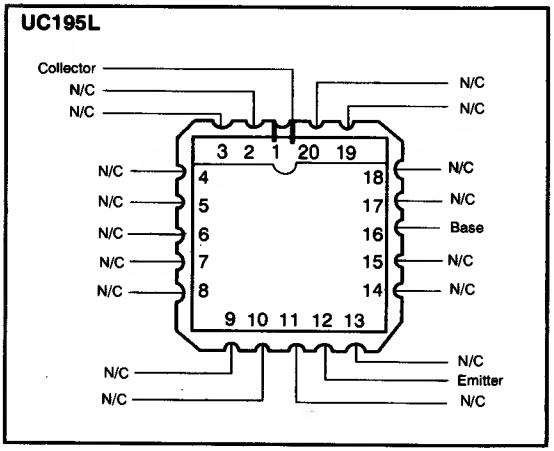

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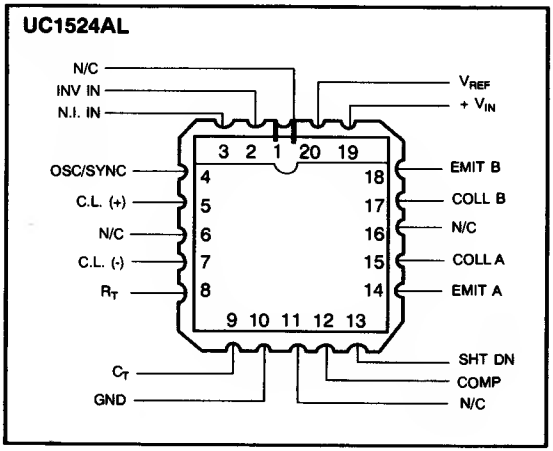

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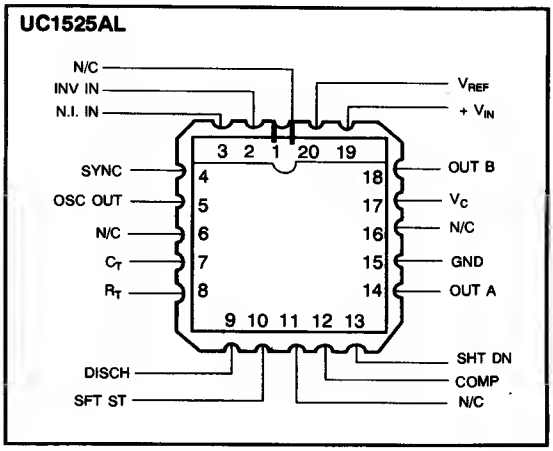

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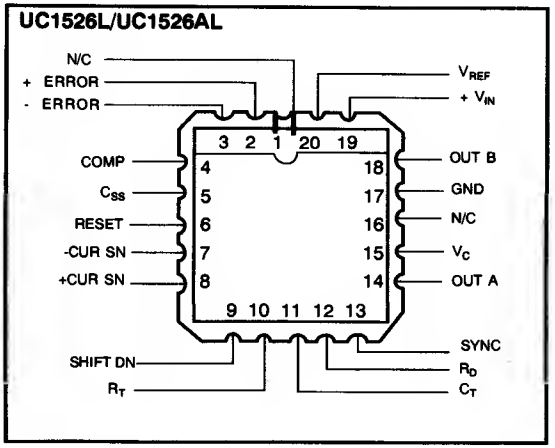

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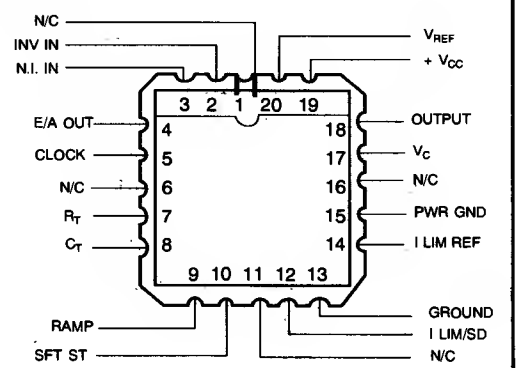

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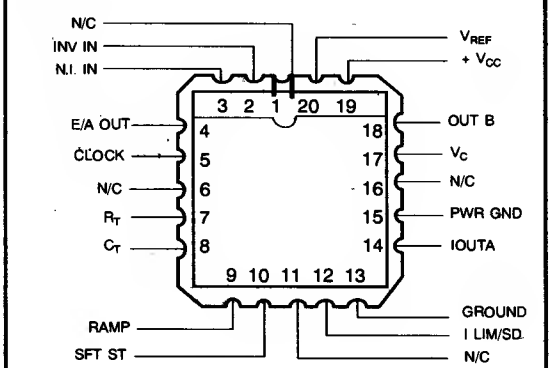

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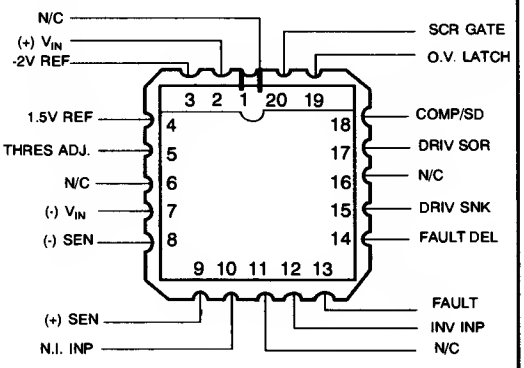

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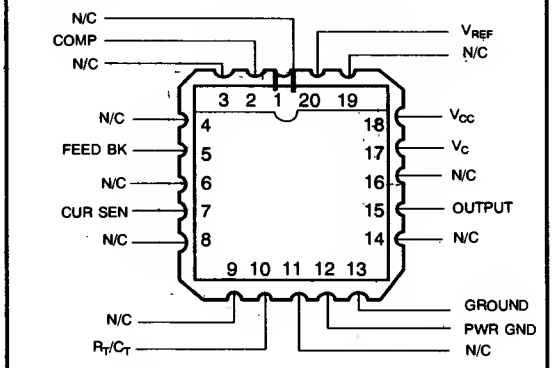

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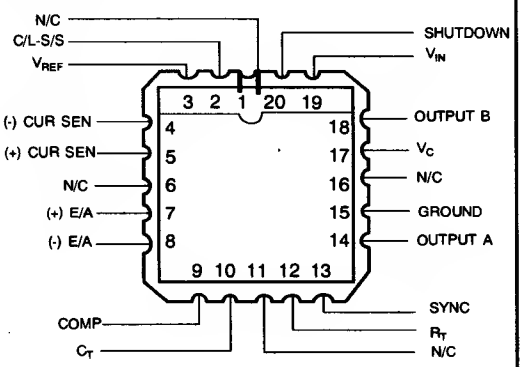

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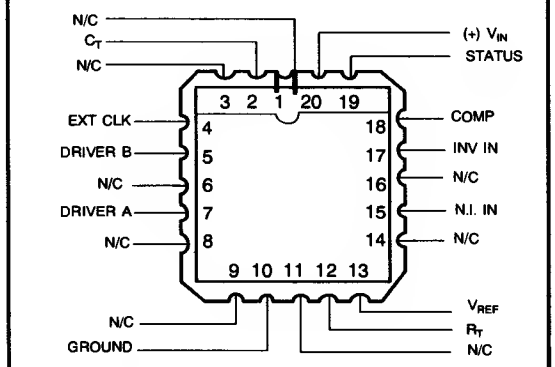

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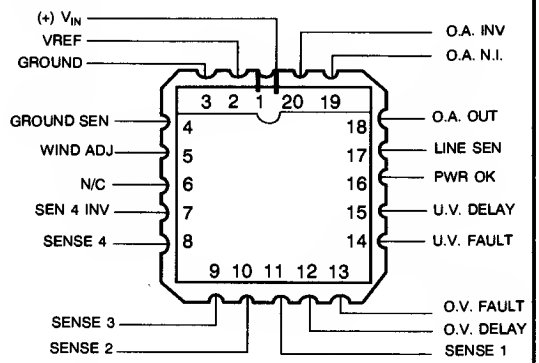

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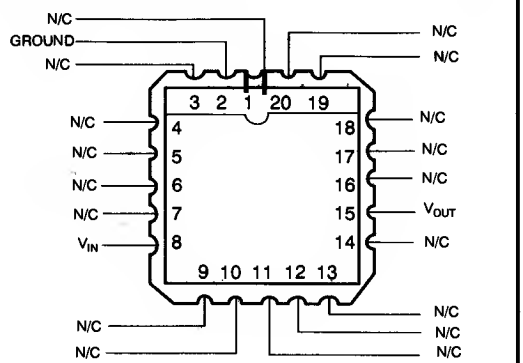

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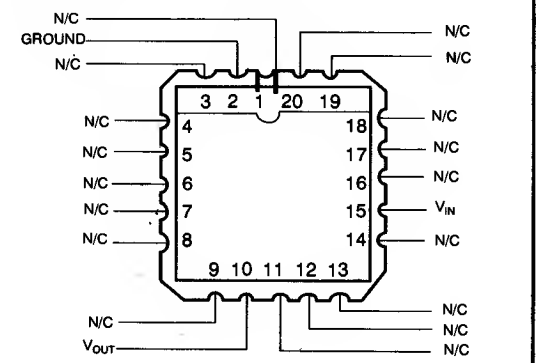

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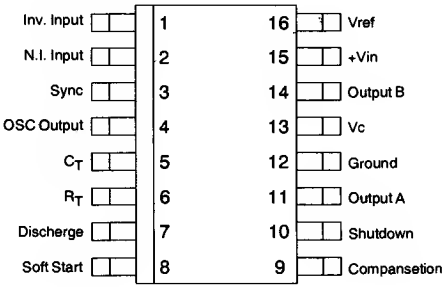

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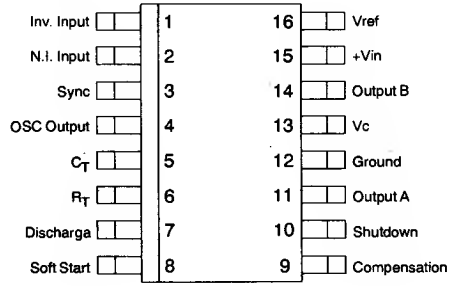

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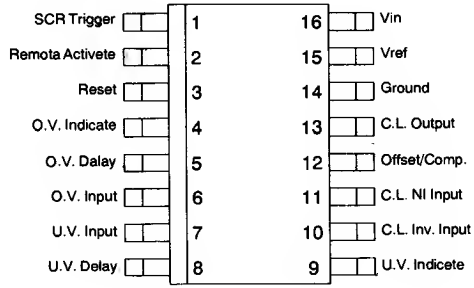

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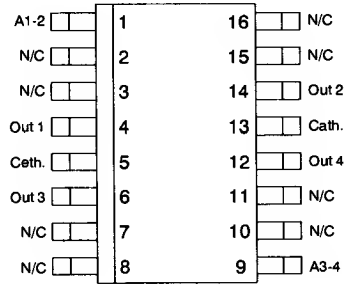

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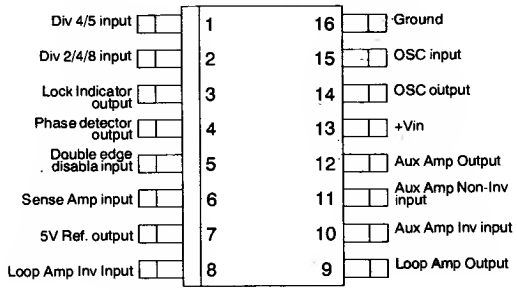

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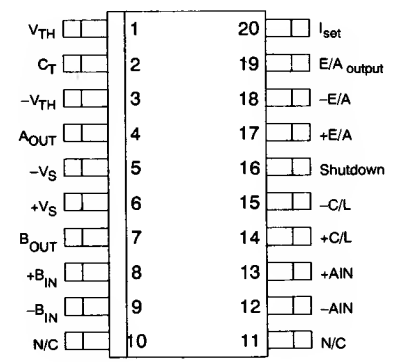

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SURFACE MOUNT CONNECTION DIAGRAMS

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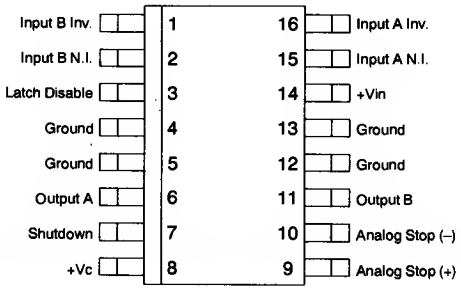

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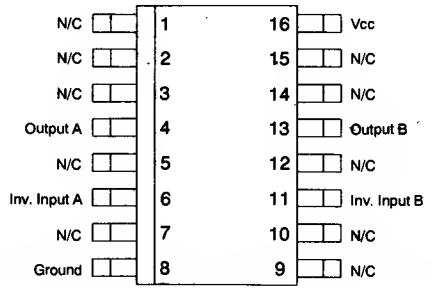

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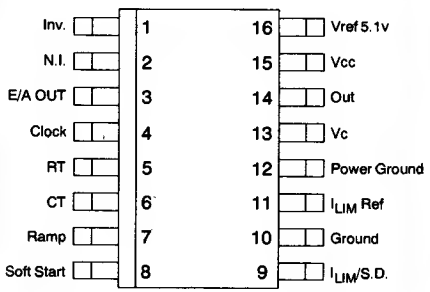

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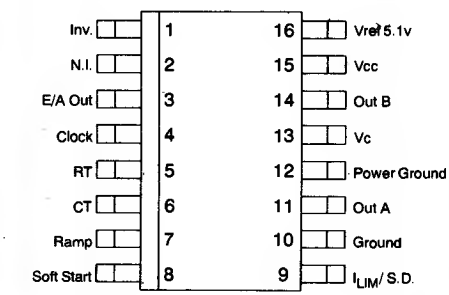

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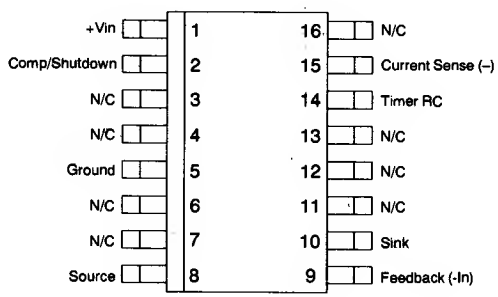

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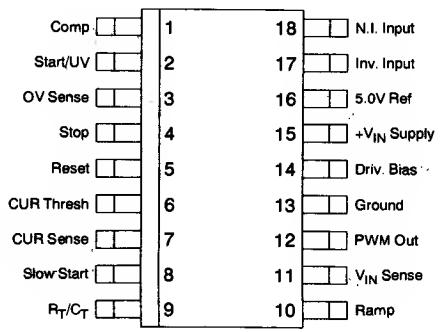

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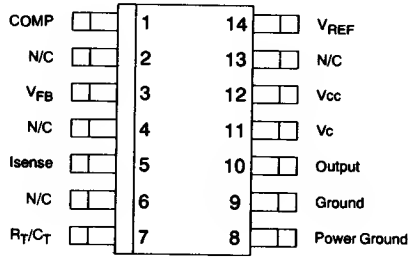

NOTE: Pin-Out Same For "A" Versions

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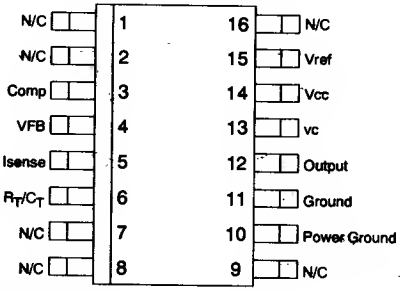

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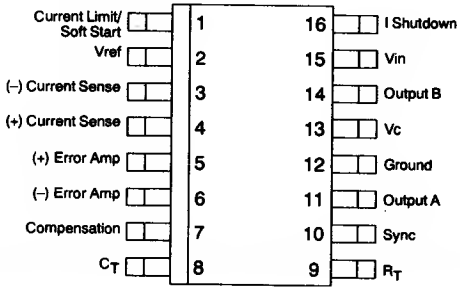

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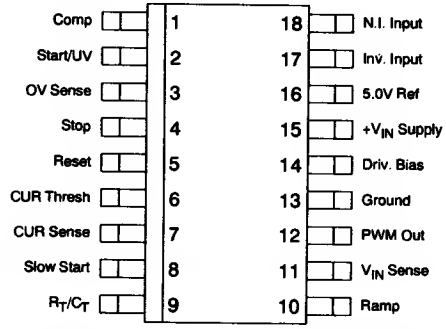

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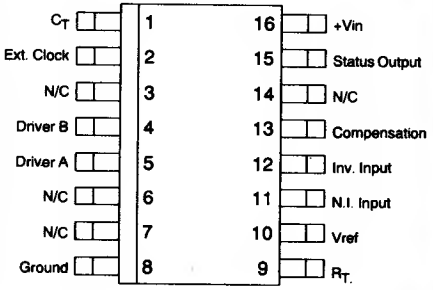

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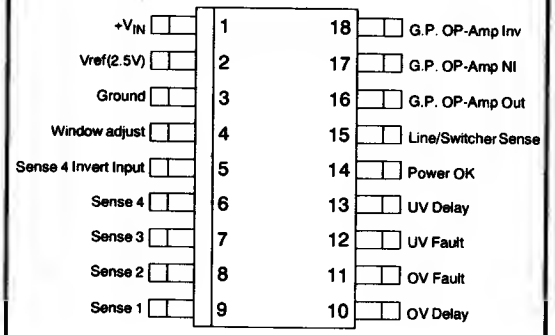

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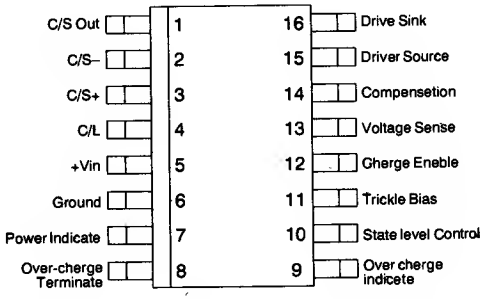

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A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

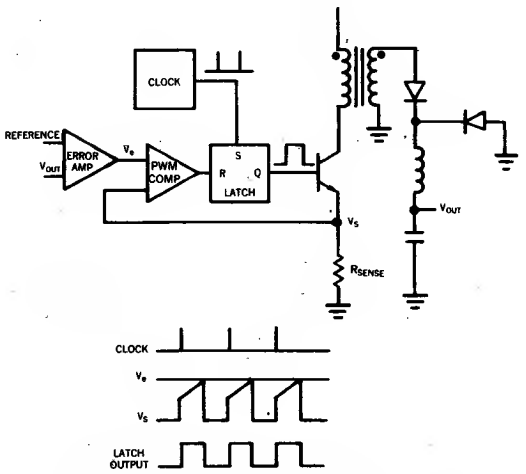


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

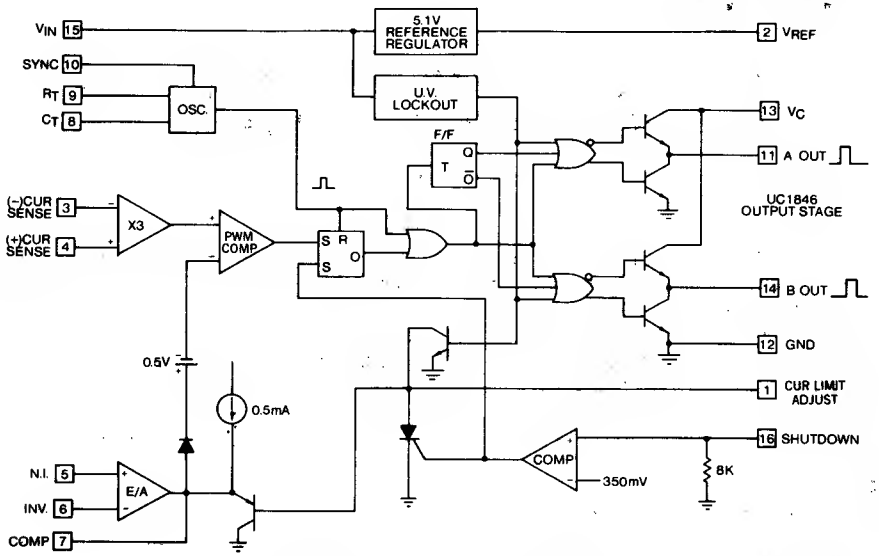


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz .
- An error amplifier with common mode range from ground to V_{cc}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

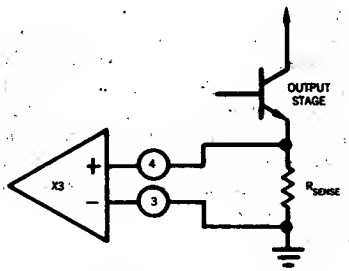
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

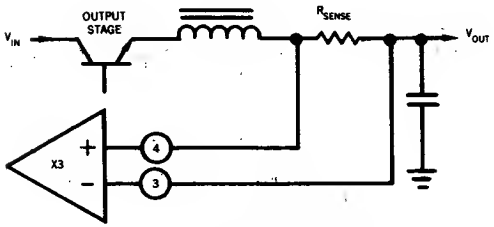
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

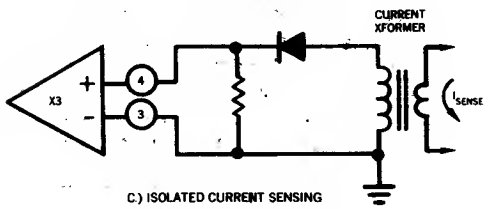
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

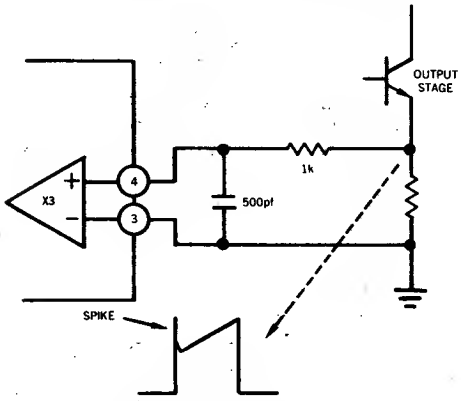


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1MHz.

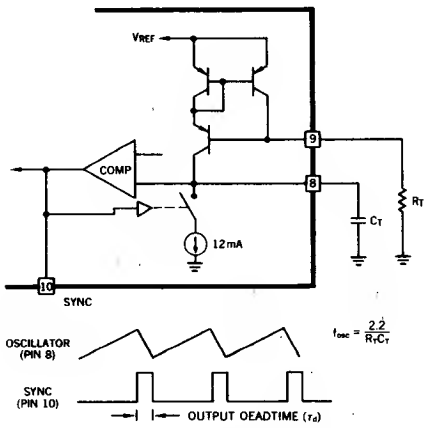


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

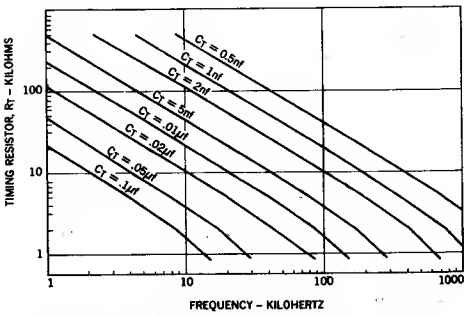


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

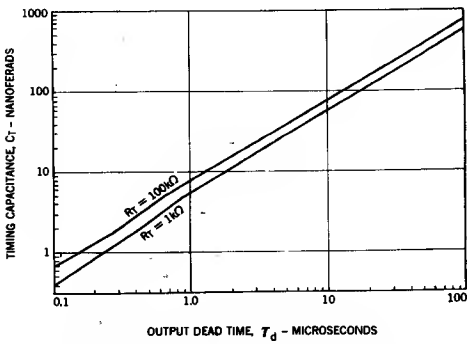


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

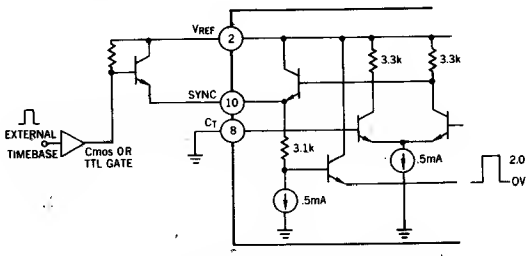


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

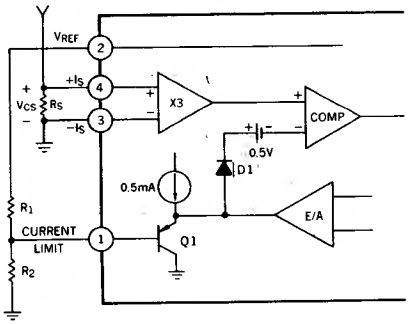


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ −0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2\ (V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

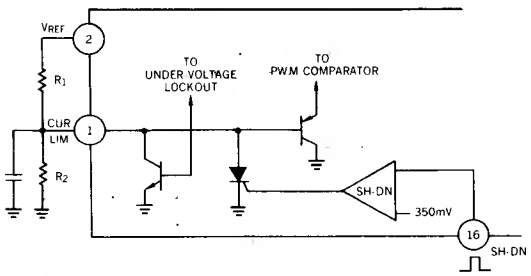


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

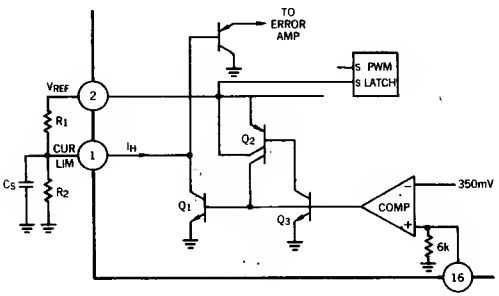


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

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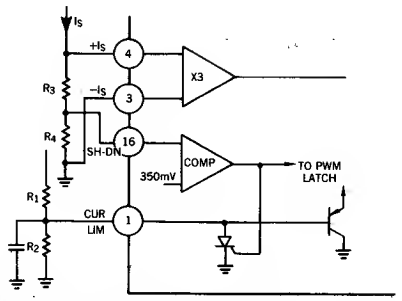


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Exampie

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4-6]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

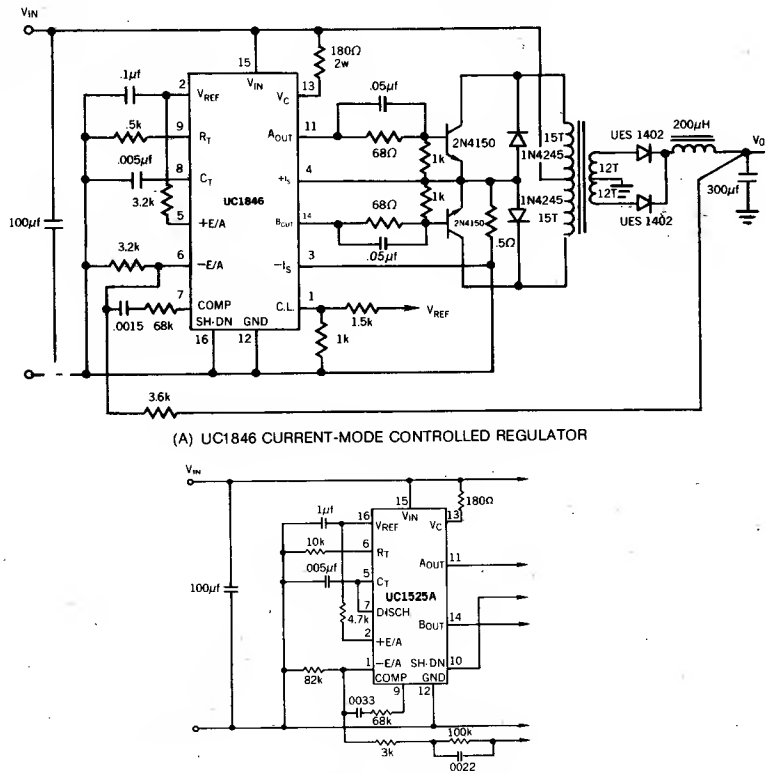
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, −E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

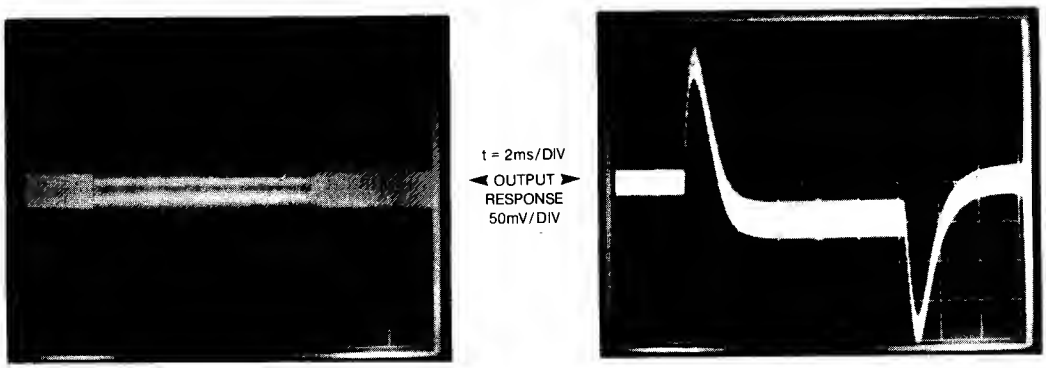
difference between switch currents of the UC1846. However, the UC1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.



(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR

(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS

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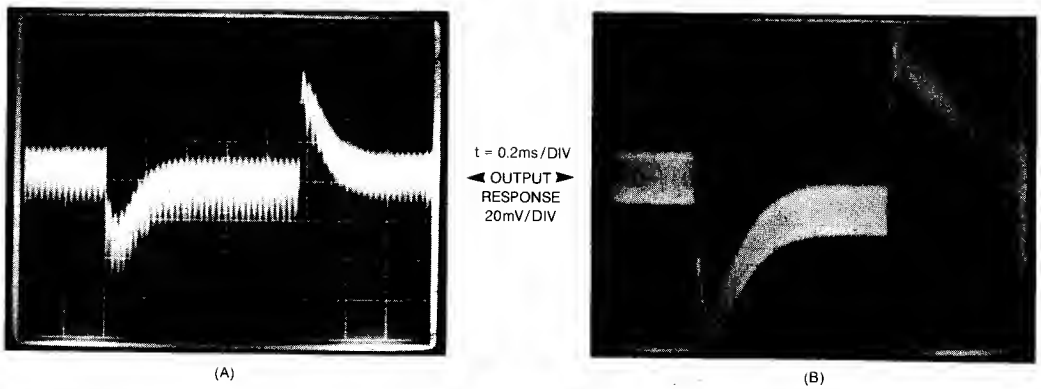

FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

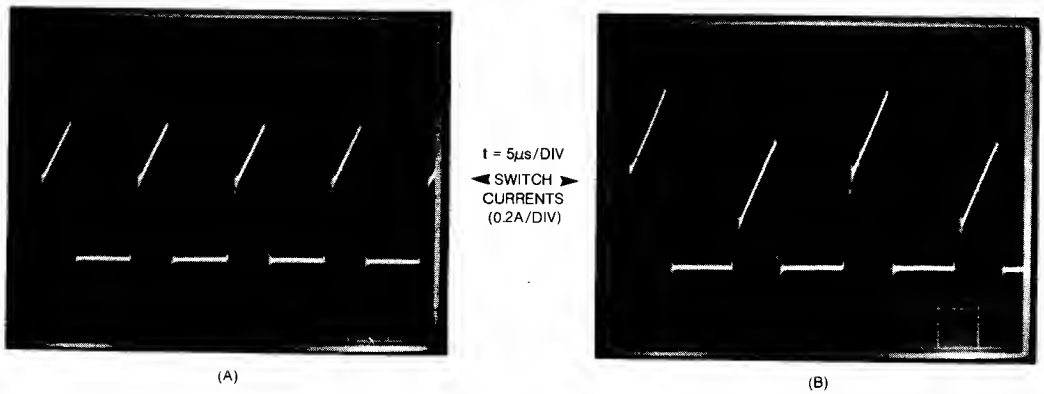

FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

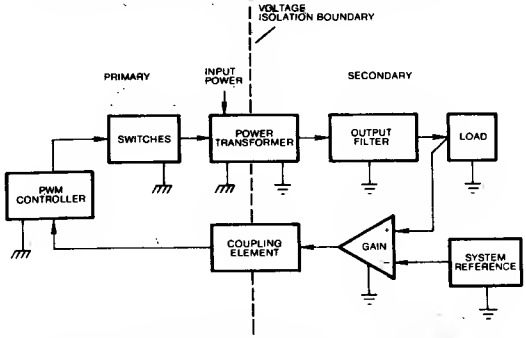


FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best undestood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

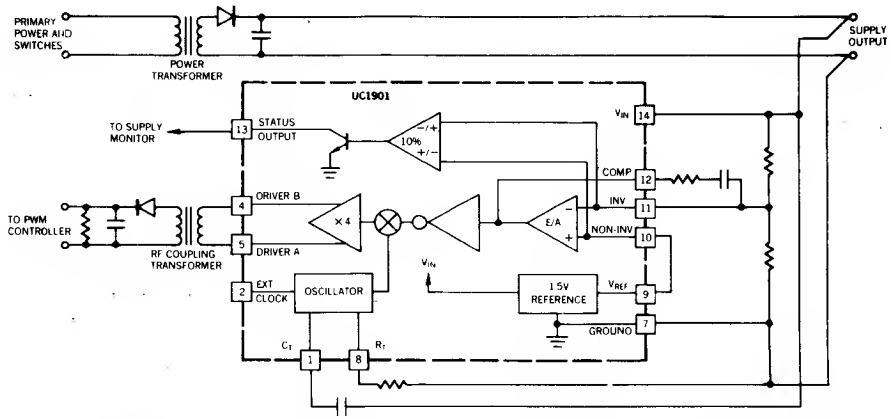


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

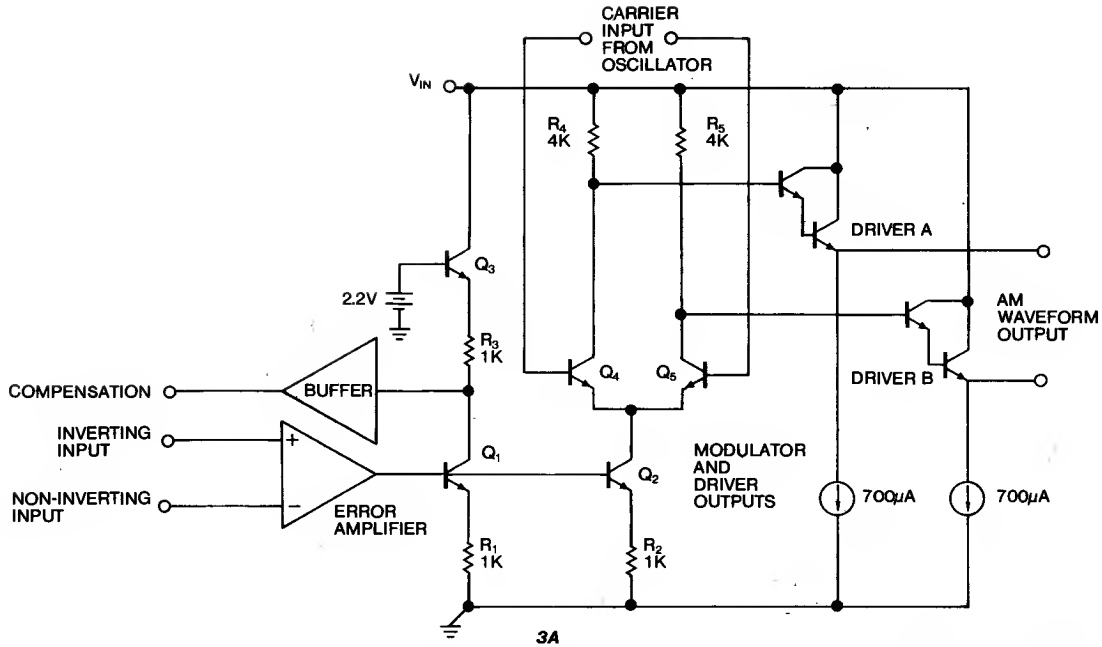


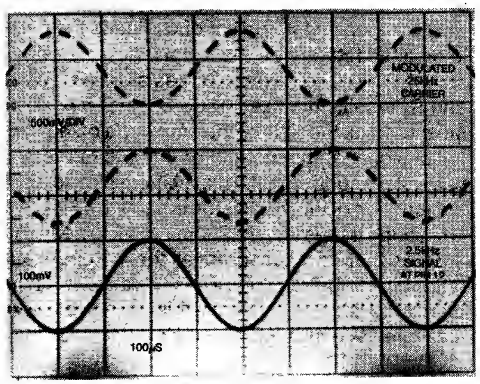
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward converters are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.



3B

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Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

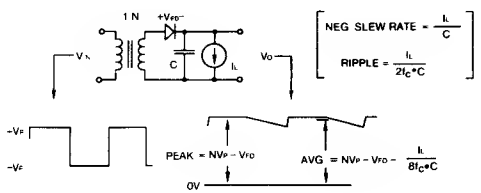

FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

$$(1) \qquad L_M \geq \frac{V_P}{4 f_c I_P}$$

Where: L_M = the magnetizing inductance,
V_P = the peak carrier voltage across transformer inputs,
f_C = the UC1901 operating frequency,
I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

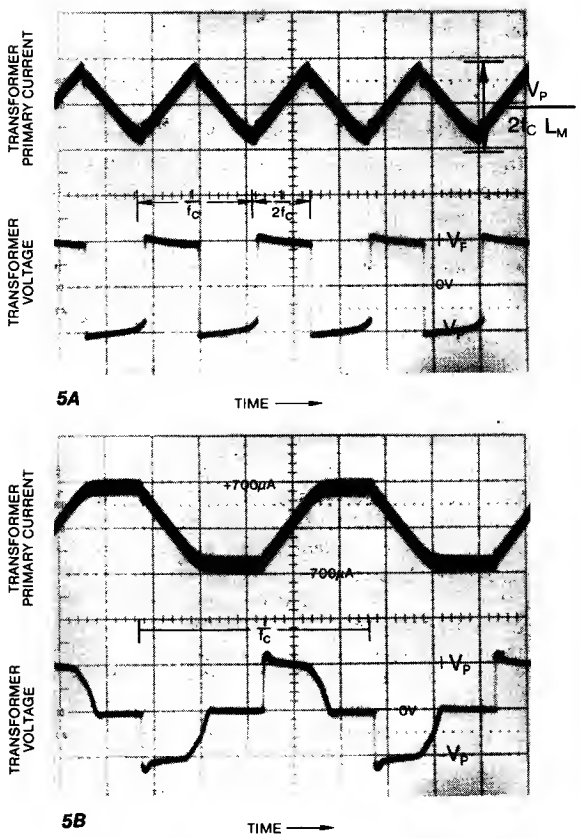

FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

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bias levels. The imbalance will be sufficient to cause the peak current to be reached during the >50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt. When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 10kΩ. A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

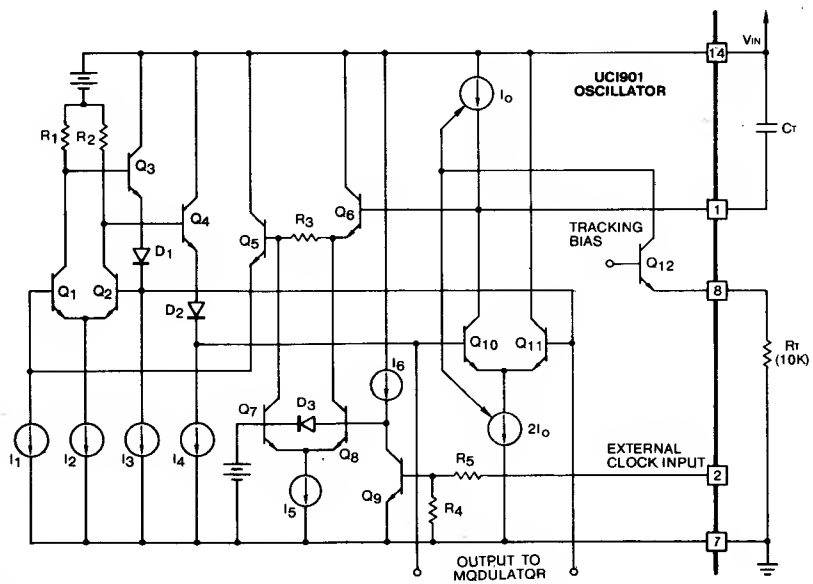

FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

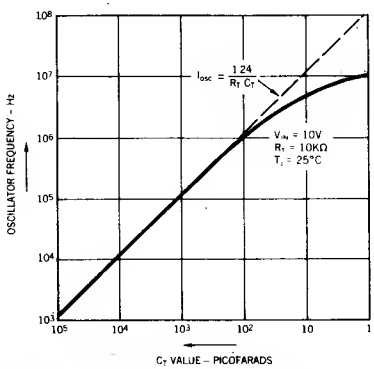

FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

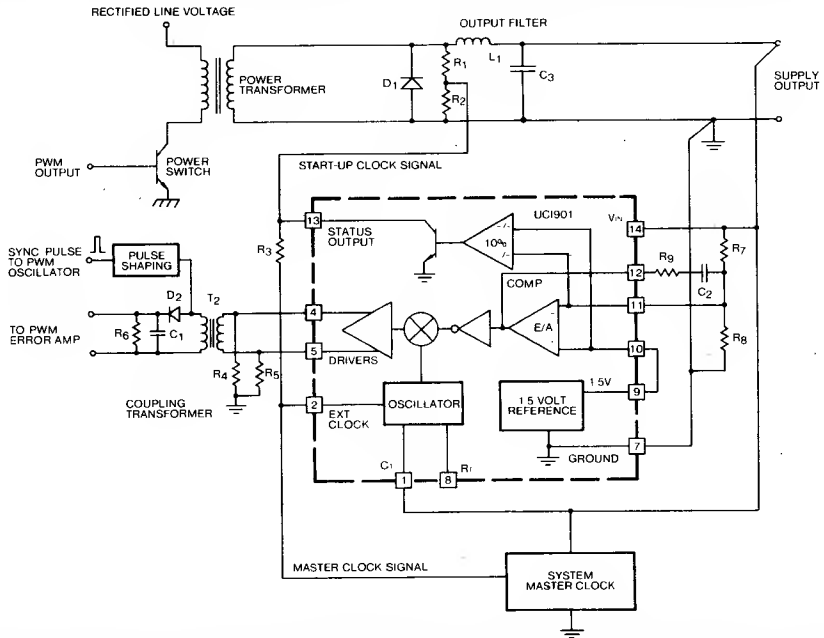

FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (< 150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3) \quad \frac{V_{OUT}}{V_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

V_{IN} = level of the rectified line voltage,

V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,

T_P = One period of the switching frequency,

L_M = Magnetizing inductance of the primary winding,

C_F = A total effective output filter capacitor,

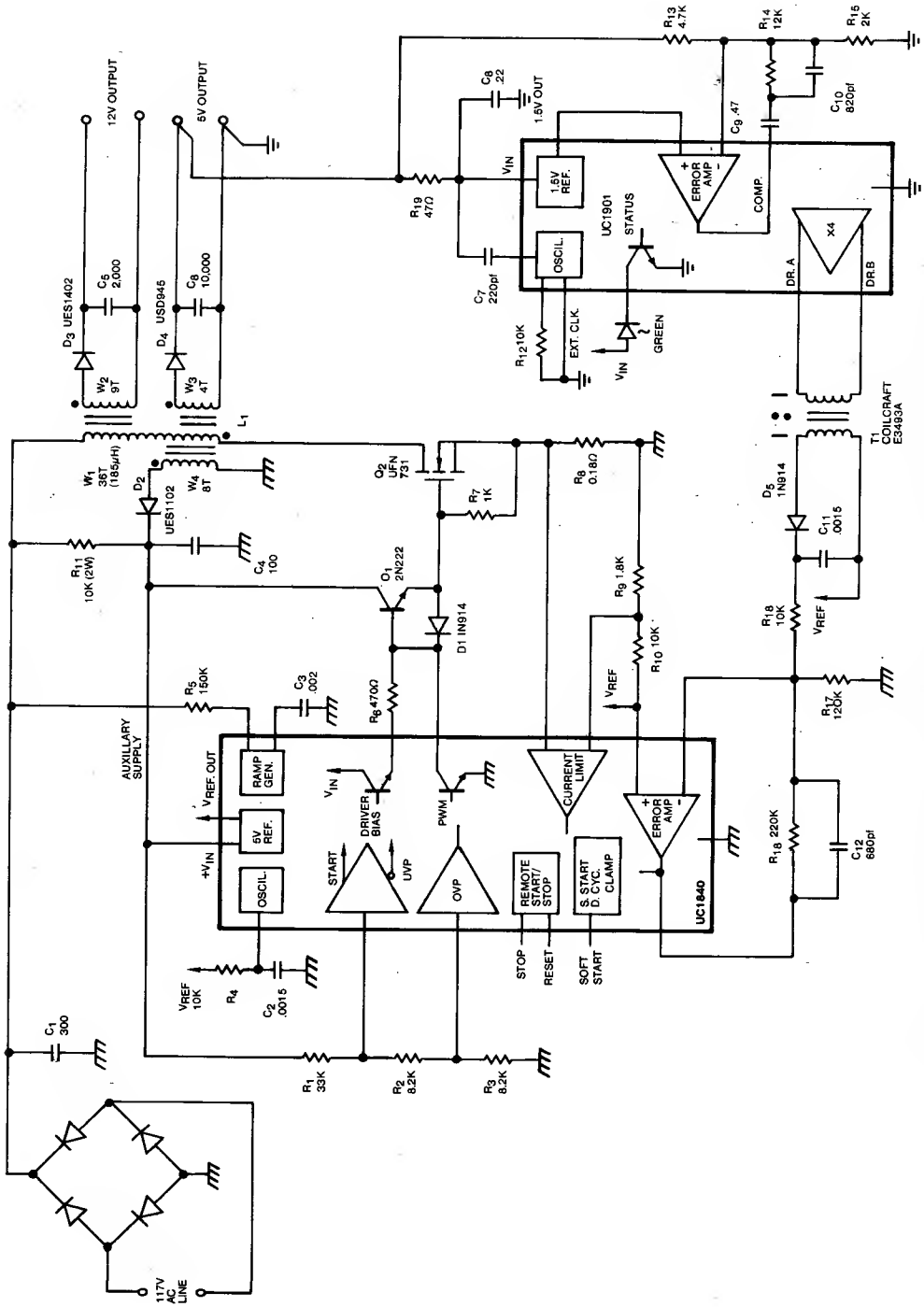

FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\, T_P}{R_5\, C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

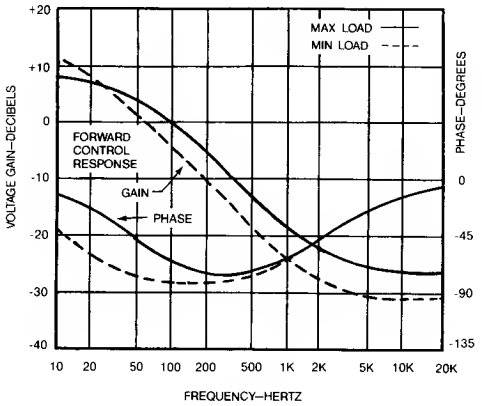

FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

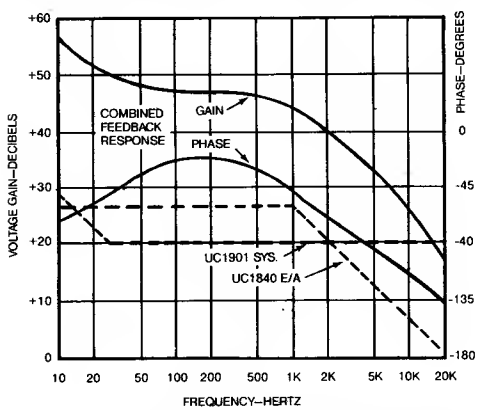

FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

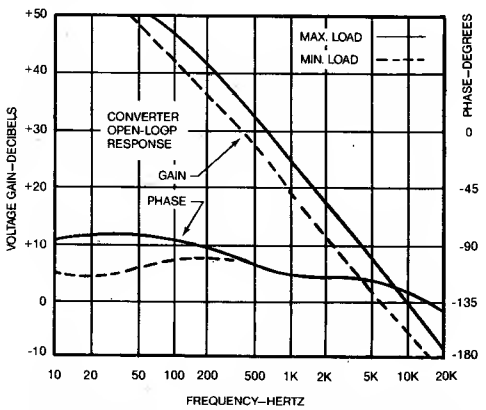

FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of > 50°.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

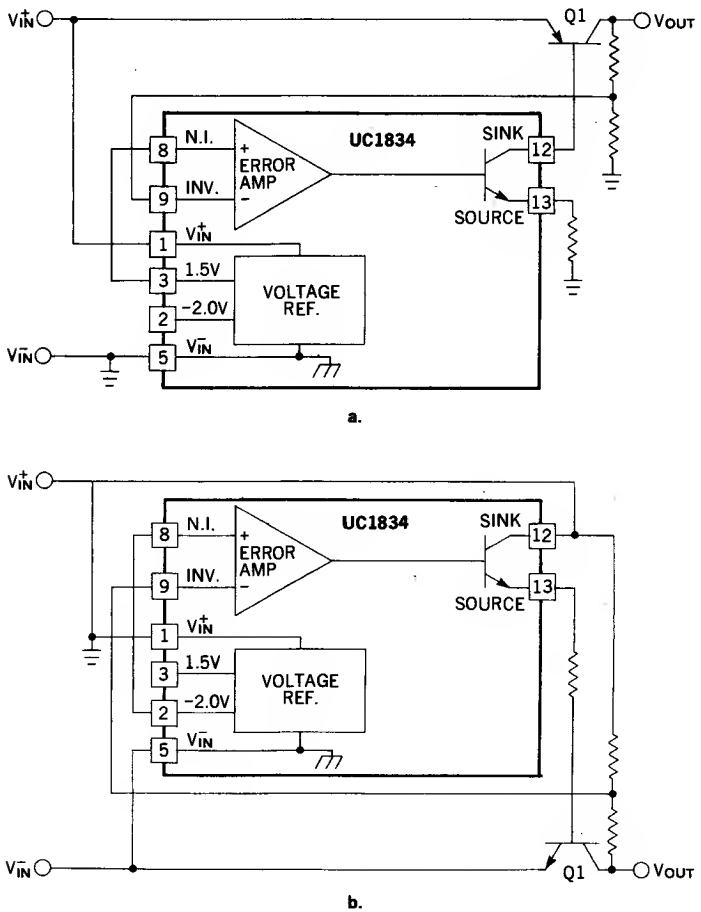

Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators Implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

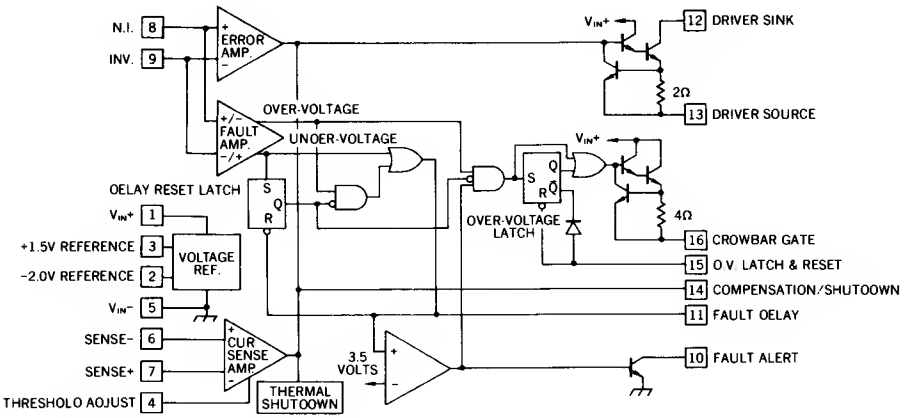

Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~30A) is possible with the Darlington pass elements of Figure 3d.

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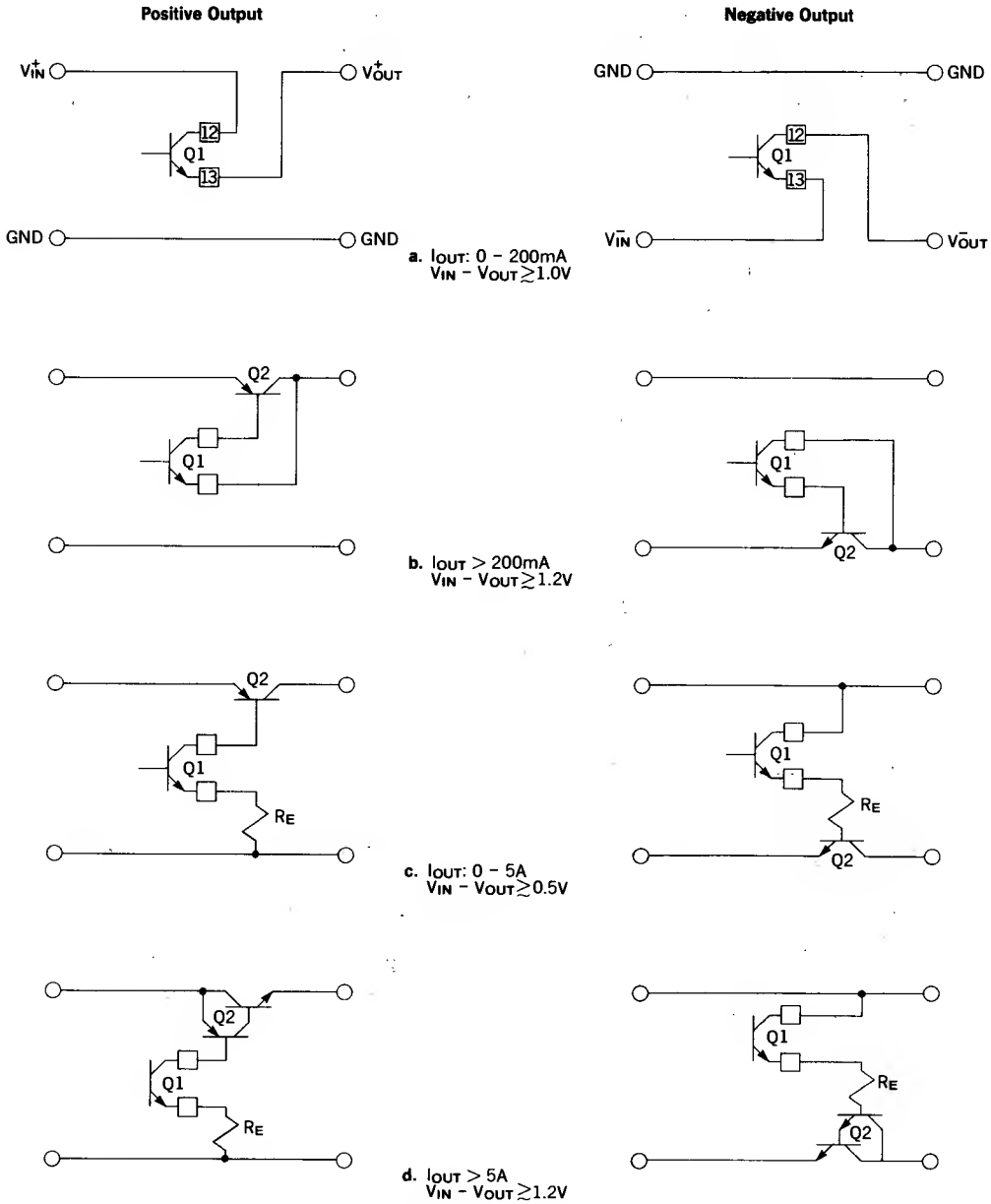


Figure 3. Pass Transistor Configurations

Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

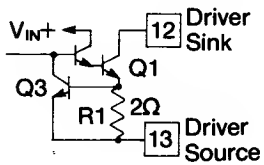
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

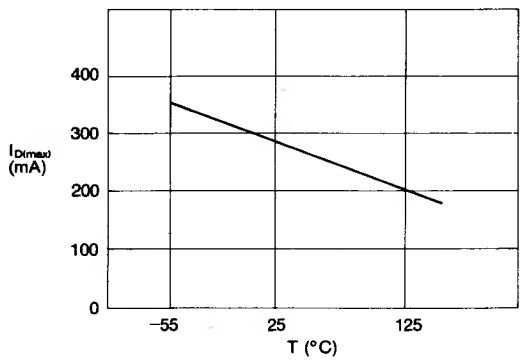
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\,out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

9

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

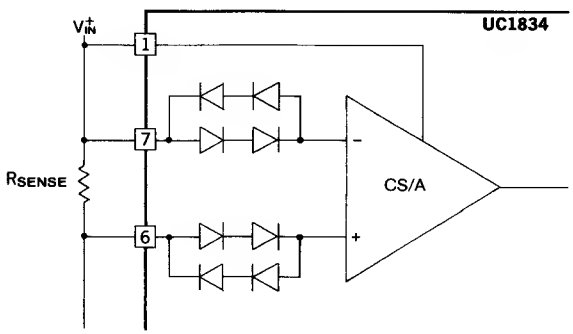


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

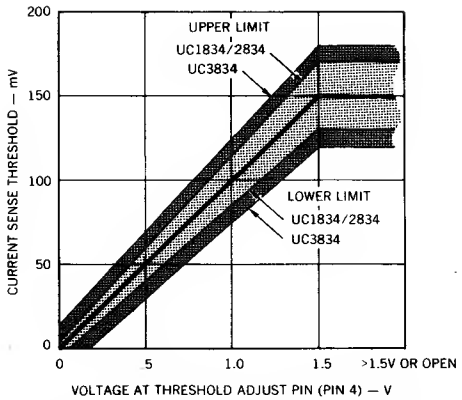


Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

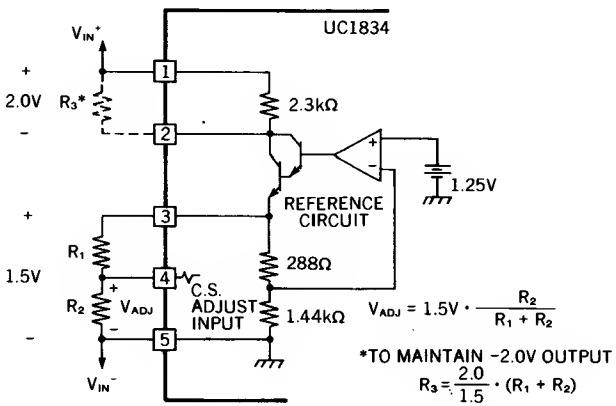


Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage. The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

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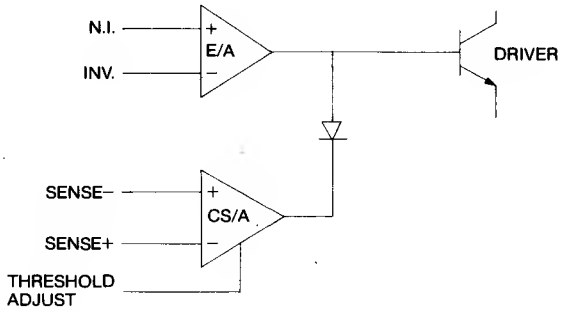

Figure 8. Current Sense Tied to E/A Output

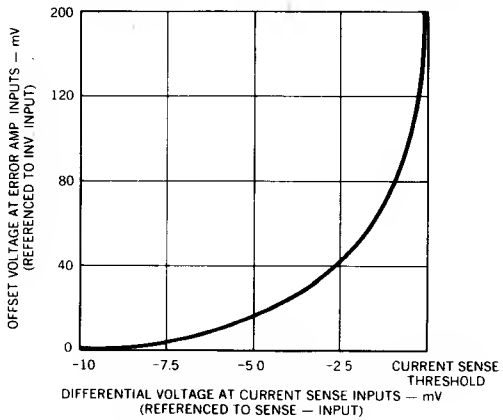

Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$$I_{E(max)} \cdot V_{CE} \simeq K \qquad \text{where K is a constant}$$

or: $$I_{E(max)} \simeq K/(V_{IN} - V_{OUT}) \quad \text{(ignoring the sense resistor voltage drop).}$$

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

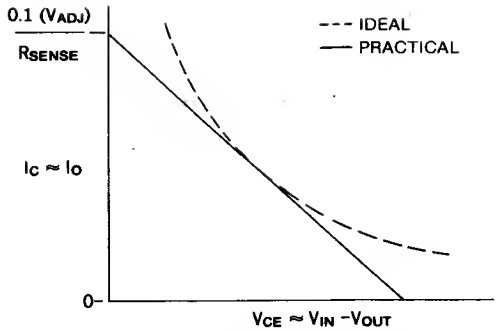

Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

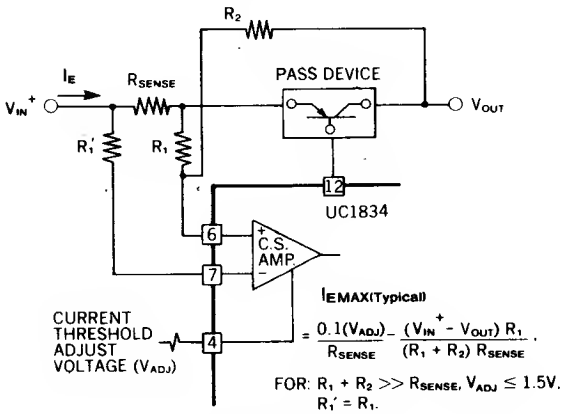

Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

9

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

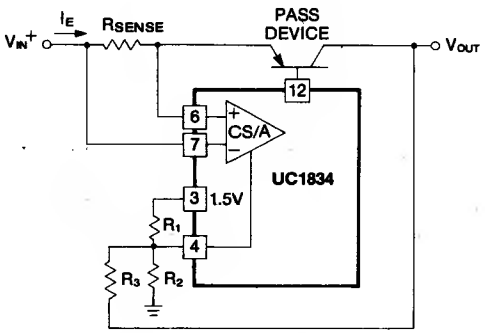

Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

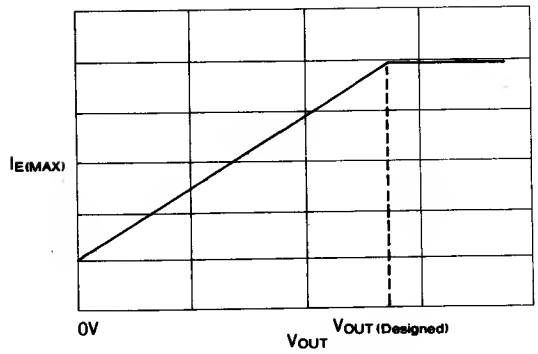

Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

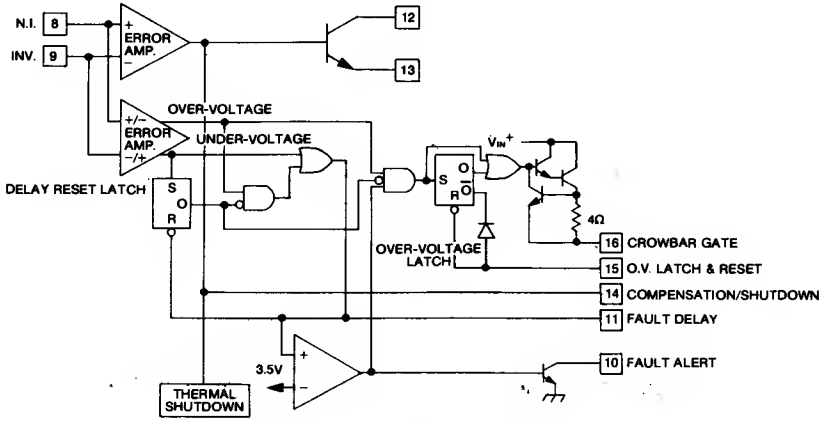

Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_c) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_c.

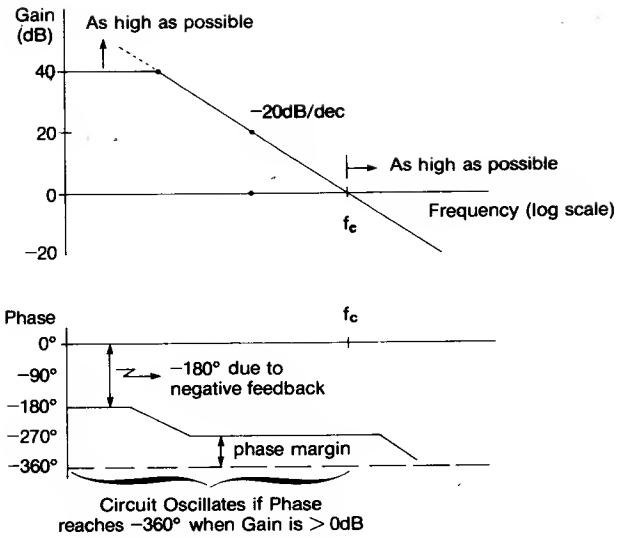

Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

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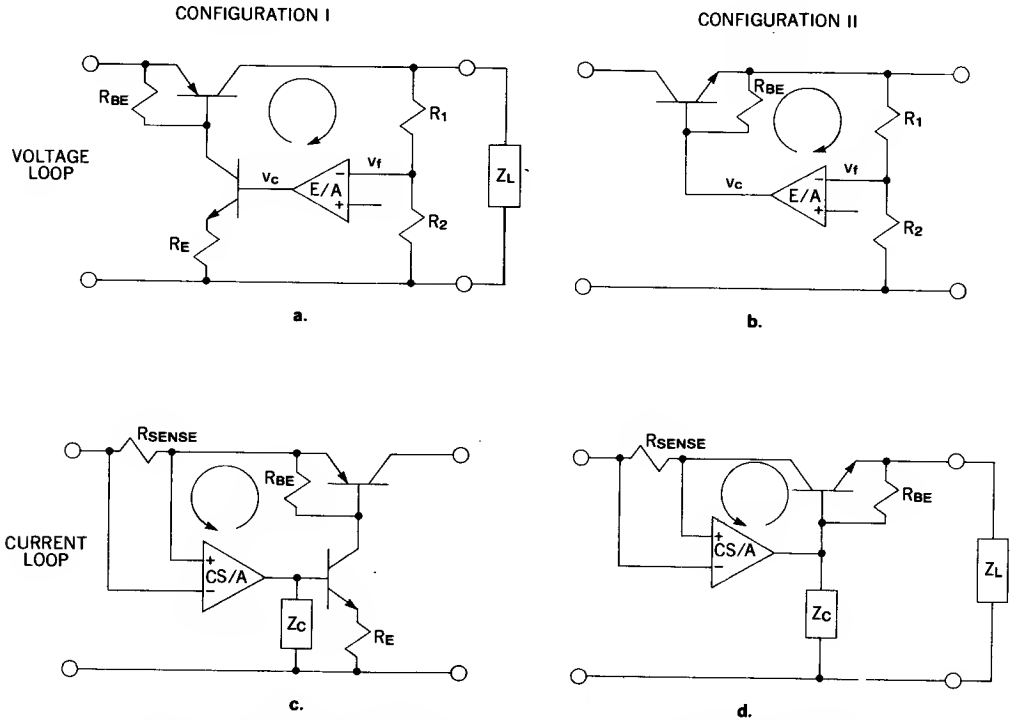

Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50MHz}{200} = 250kHz$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51k\Omega}{(1.7 + 0.51)\ k\Omega} = 20 = 26dB.$$

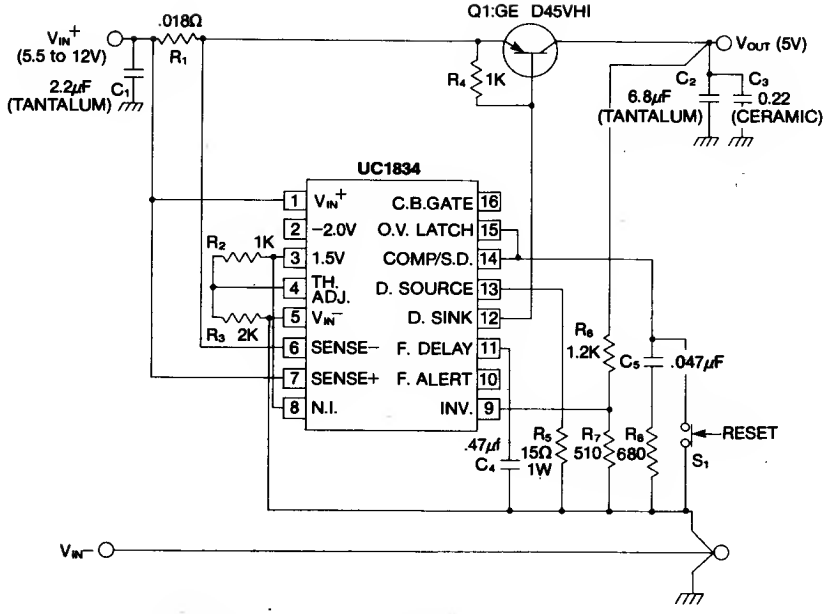

Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

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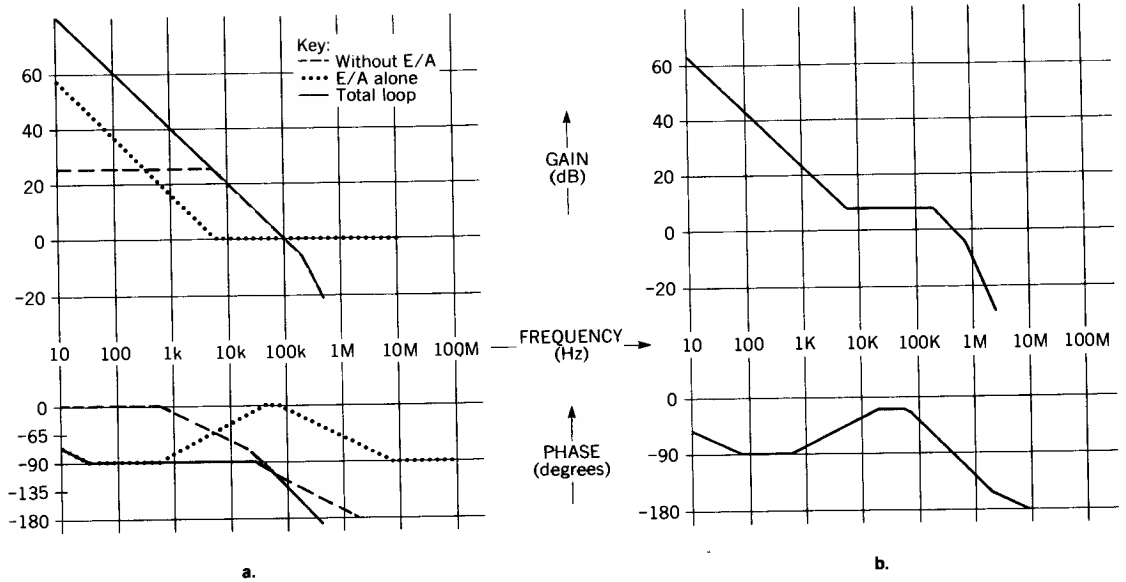


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

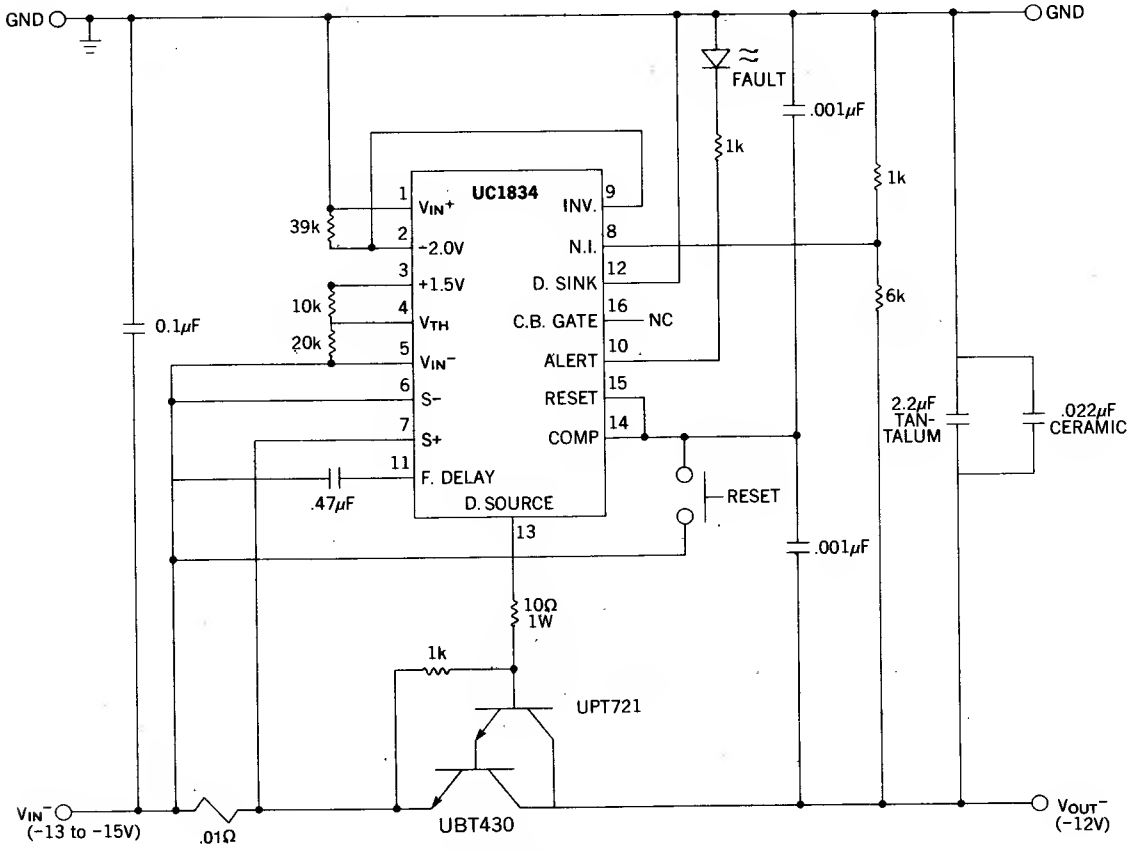


Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{0.026mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

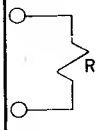
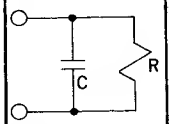
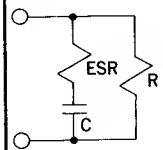
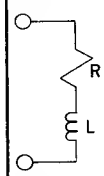
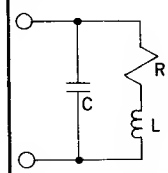
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_C \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

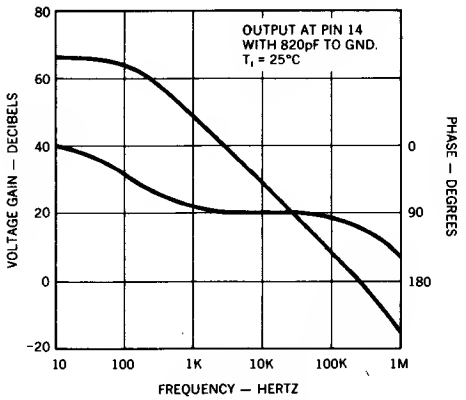


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

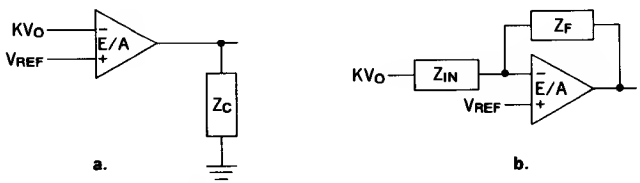


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

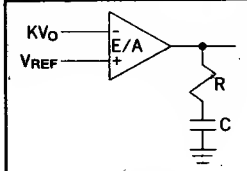
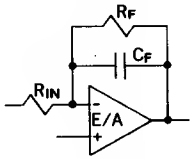
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s R_F C_F)}$	$\frac{1}{2\pi R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

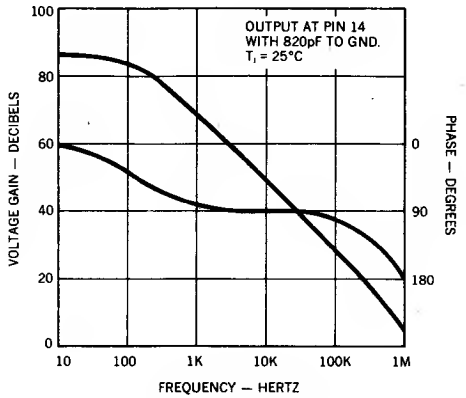


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d).Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right).$$

A 25 WATT OFF-LINE FLYBACK SWITCHING REGULATOR

Introduction

This Application Note describes a low cost (less than $10.00) switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc...The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC3844 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOSFET (UFN833) is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. −12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750 Volts
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

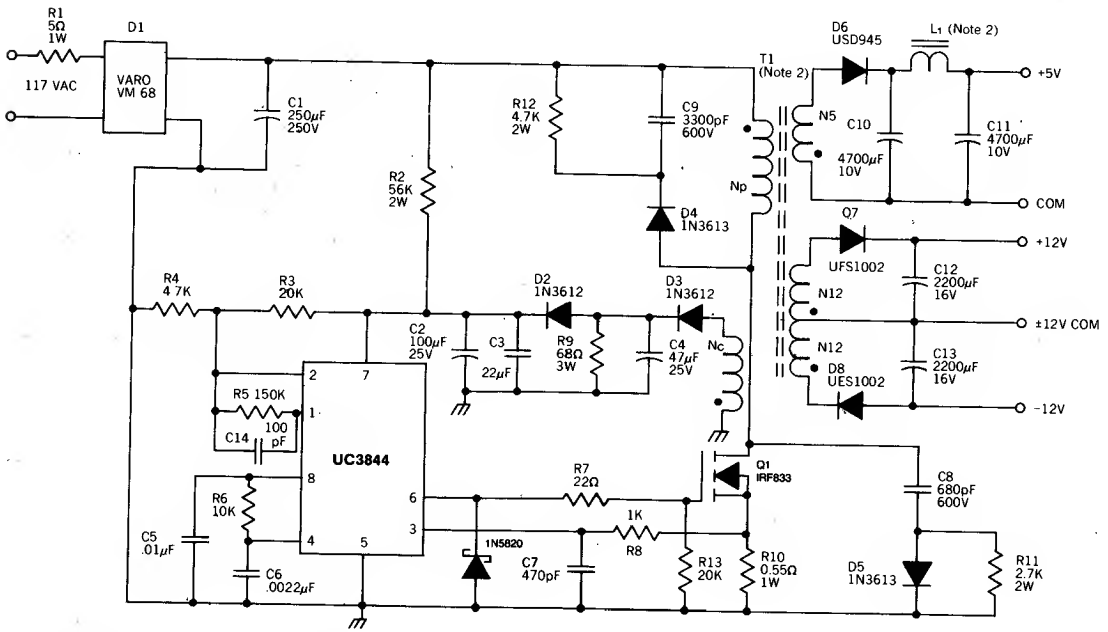
The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOSFET Q1. During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 volt reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding, Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

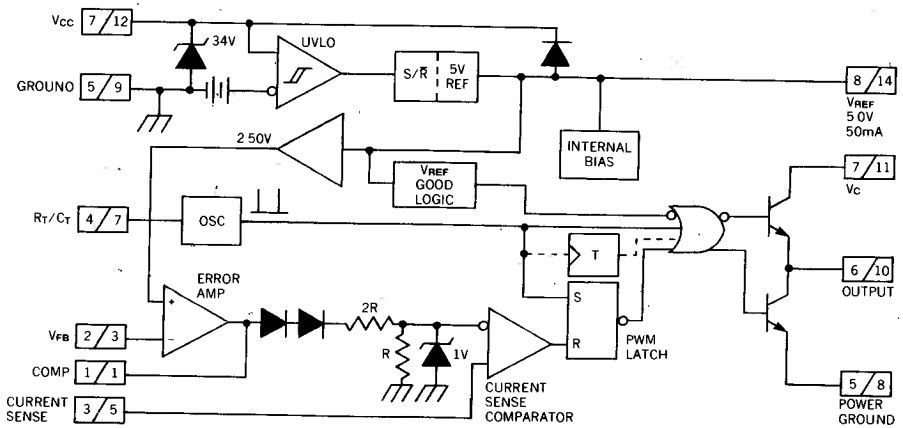
A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

25W OFF-LINE FLYBACK REGULATOR



Notes: 1. All resistors are ¼ watt unless noted
2. See Appendix for construction details

BLOCK DIAGRAM

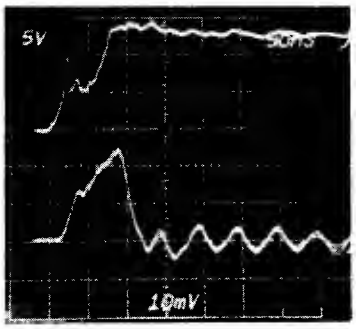


Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.

UC3842/3/4/5 CURRENT MODE PWM CONTROLLER

TYPICAL SWITCHING WAVEFORMS

T_{on} — Drive waveforms

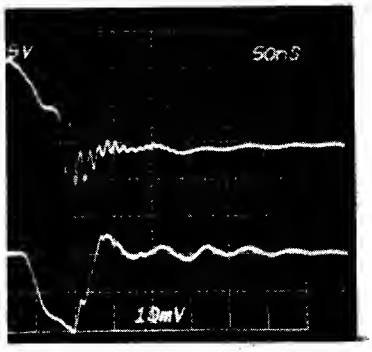


5V/DIV

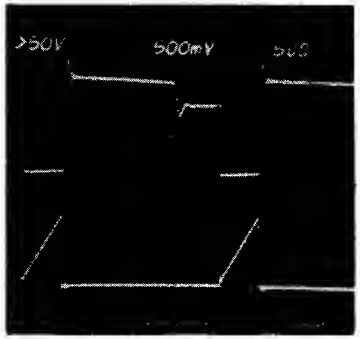
200mA/DIV

Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current

T_{off} — Drive waveforms



Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current



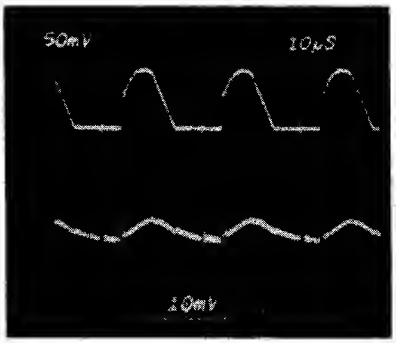
100V/DIV

0.5A/DIV

Upper trace: Q_1 — Drain to source voltage
Lower trace: Primary current — I_D

5A/DIV

50mV/DIV



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

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PERFORMANCE DATA

CONDITIONS		5V out	12V out	−12V out
Low Line (95VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.211	12.05	−12.01
	4.0A	4.854	12.19	−12.14
± 12 @ 300mA	+5V @ 1.0A	5.199	11.73	−11.69
	4.0A	4.950	11.68	−11.63
Nominal Line (120VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.220	12.07	−12.03
	4.0A	4.875	12.23	−12.18
± 12 @ 300mA	+5V @ 1.0A	5.208	11.73	−11.68
	4.0A	4.906	11.67	−11.62
High Line (130VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.207	12.06	−12.02
	4.0A	4.855	12.21	−12.15
± 12V @ 300mA	+5V @ 1.0A	5.200	11.71	−11.67
	4.0A	4.902	11.66	11.61
Overall Line and Load Regulation		±3.5%	±2.3%	±2.4%

PARTS LIST

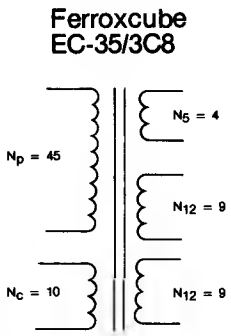
IC's		**CAPACITORS**		C10, C11	4700µF, 10V	R7	22Ω
IC1	UC3844	C1	250µF, 250V	C12, C13	2200µF, 16V	R8	1K
POWER MOSFET		C2	100µF, 25V	C14	100pF, 25V	R9	68Ω, 3W
Q1	UFN833	C3	0.22µF, 25V	**RESISTORS**		R10	0.55Ω, 1W
RECTIFIERS		C4	47µF, 25V	R1	5Ω, 1W	R11	2.7K, 2W
D1	VM68 varo	C5	.01µF, 25V	R2	56K, 2W	R12	4.7K, 2W
D2, D3	1N3612	C6	.0047µF, 25V	R3	20K	R13	20K
D4, D5	1N3613	C7	470pF, 25V	R4	4.7K	**MAGNETICS**	
D6	USD945	C8	680pF, 600V	R5	150K	T_1	see appendix
D7, D8	UES1002	C9	3300pF, 600V	R6	10K	L_1	see appendix

APPENDIX

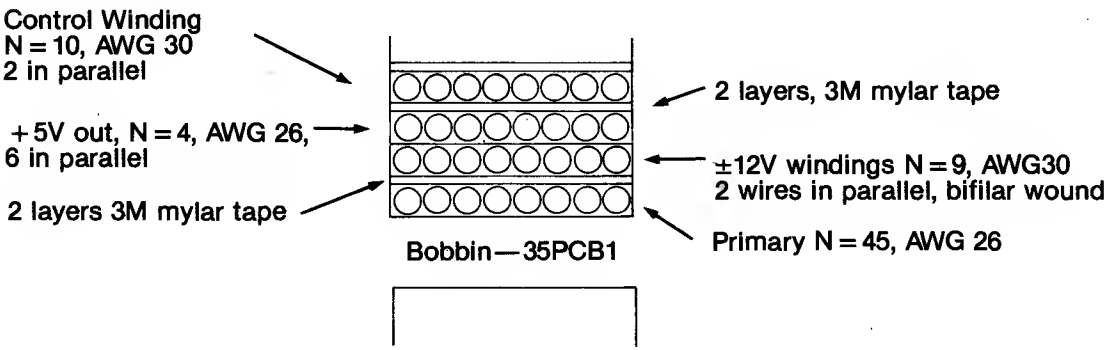
POWER TRANSFORMER—T1

Core: Ferroxcube EC-35/3C8
Gap: 10 mil in each outer leg

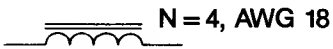
NOTE: For reduced EMI put gap in center leg only. Use 20 mil.



TRANSFORMER CONSTRUCTION



5V OUTPUT INDUCTOR



Ferroxcube
204 T 250 — 3C8 (toroid)

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Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
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MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated[1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation – usually a single resistor – adds to its attractiveness. However, this introduces a new problem – that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from, yet containing elements of each. Although this has been addressed in part by several authors[1, 2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

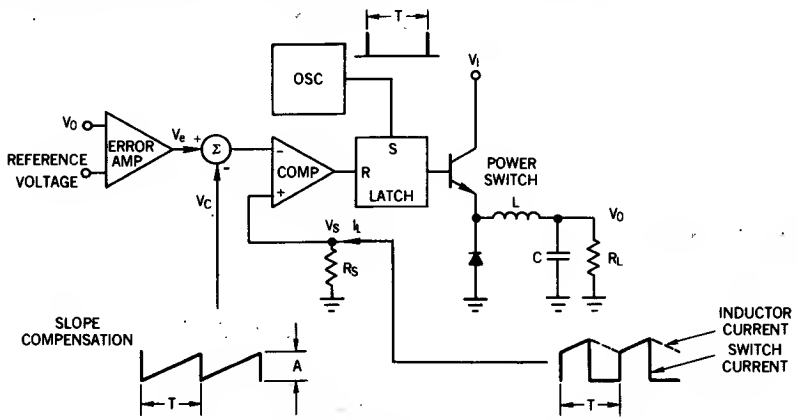

FIGURE 1 – A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in(1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle – regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

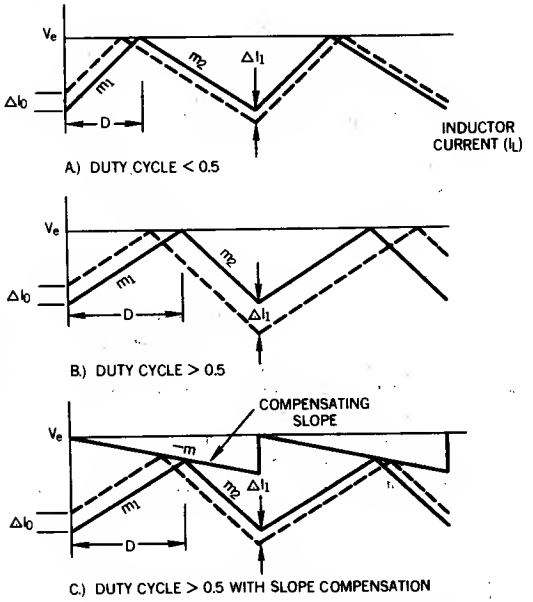

FIGURE 2 – DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for $D < 0.5$ (Figure 2A), and increase with time for $D > 0.5$ (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope $-m$ as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

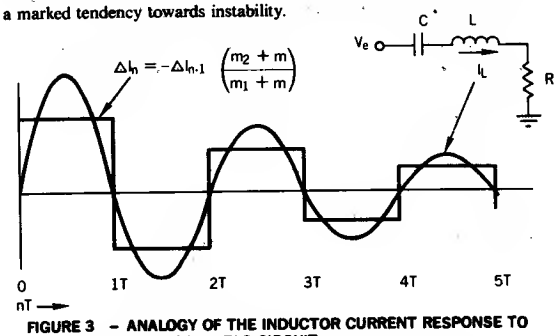

FIGURE 3 – ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

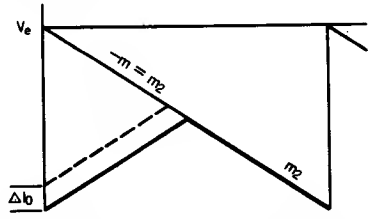

FIGURE 4 – FOR THE CASE OF $m = -m_2$, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

9

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and – because of excess phase shift in the modulator – can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

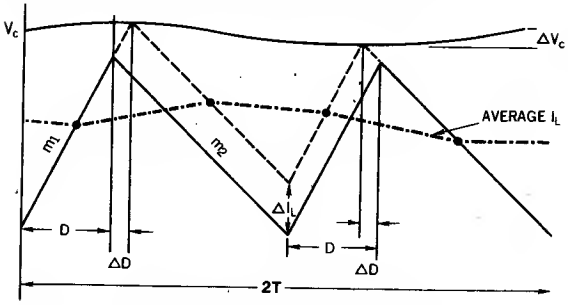

FIGURE 5 – CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation.

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \qquad (4)$$
$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \qquad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \qquad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \qquad (7)$$

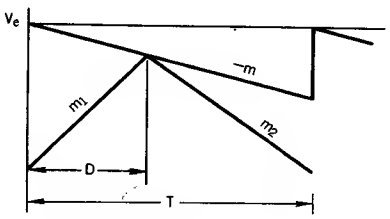

FIGURE 6 – ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \qquad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \qquad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \qquad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = ½f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \qquad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = ½\, f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \qquad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = ½f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \qquad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation. A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = ½f_S$, then for the case of $m = 0$ (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -½m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

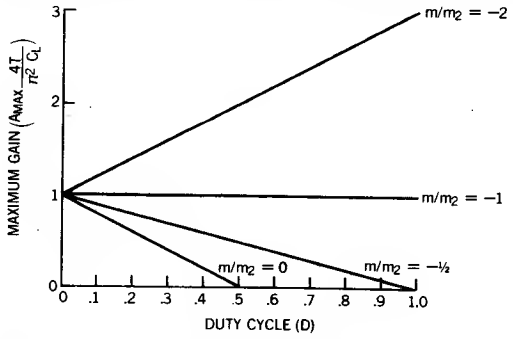

FIGURE 7 – MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage – in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output – or feedforward characteristics. If we choose to add slope compensation equal to $m = -\frac{1}{2} m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -\frac{1}{2} m_2$.

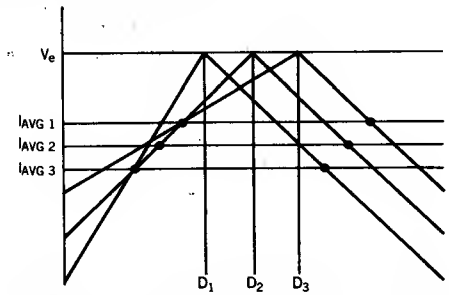

FIGURE 8 – PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

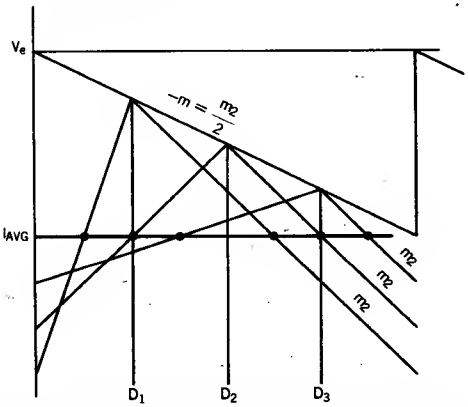

FIGURE 9 – AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUTY CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -\frac{1}{2} m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons – reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the sballow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current – not just the ripple current. This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -\frac{1}{2} m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

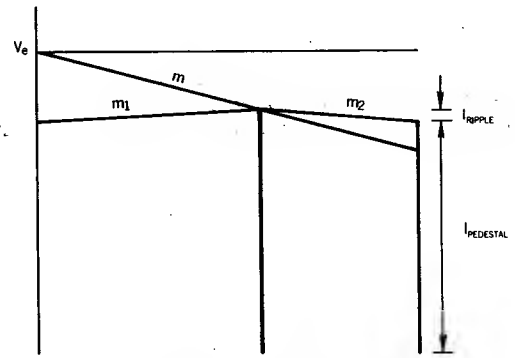

FIGURE 10 – A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

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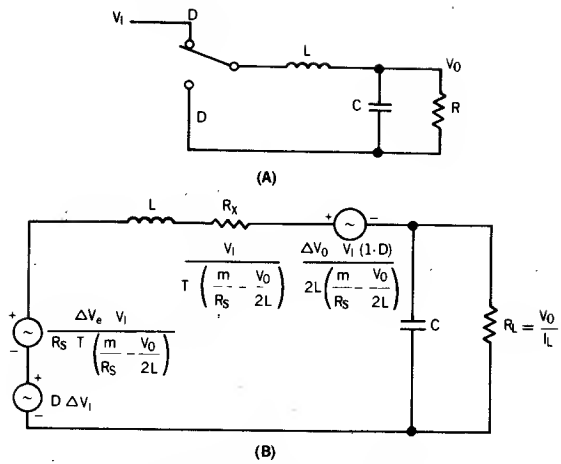


FIGURE 11 – BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations – that in substitute $V_I + \Delta V_I$, $V_O + \Delta V_O$, $D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables – and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_O}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_O = \frac{\Delta I_L}{C} - \frac{\Delta V_O}{CR} \qquad (17)$$

A third equation – the control equation – relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\,V_O\,T\,R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S}-\frac{V_O}{2L}\right) - \frac{T}{2L}(1-D)\,\Delta V_O \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state-space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e \; V_I}{R_S \; LT\left(\frac{m}{R_S}-\frac{V_O}{2L}\right)} - \frac{\Delta V_O \; V_I\,(1-D)}{2L^2\left(\frac{m}{R_S}-\frac{V_O}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S}-\frac{V_O}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_O = \frac{\Delta I_L}{C} - \frac{\Delta V_O}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation ($m = 0$), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to $L\left(m \gg \frac{R_S\,V_O}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S\,V_O}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S\,V_O}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_O/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_O = 12V
V_I = 25V
L = 200μH
C = 300μf
T = 20μS
R_S = .5Ω
R_L = 1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced, ripple rejection slowly degrades to that of a voltage-mode converter (−6.4dB for this example).

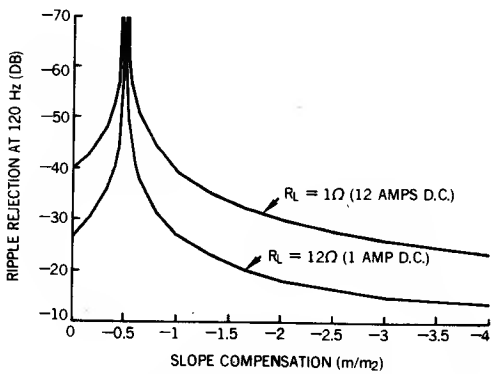


FIGURE 12 – RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used, as is the case for R_L = 1 ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}$ m_2, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used, the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift.

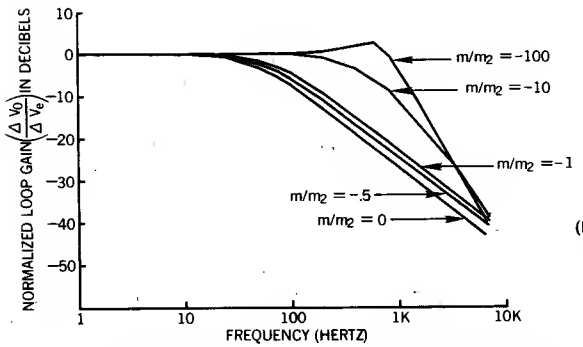
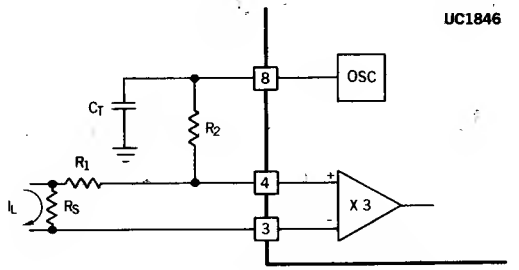
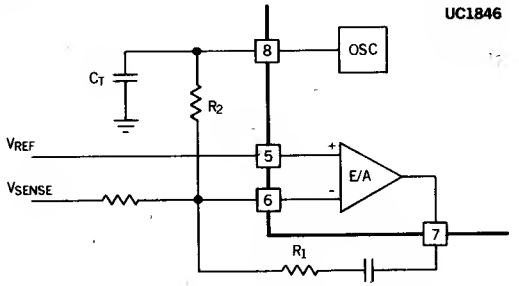


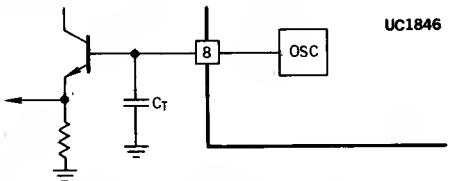
FIGURE 13 – NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 – ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

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(4) W. Burns, A. Ohri, "Improving Off-Line Converter Performance with Current-Mode Control," Powercon 10 Proceedings, Paper B-2, 1983.

(5) B. Holland, "A New Integrated Circuit for Current-Mode Control," Powercon 10 Proceedings, Paper C-2, 1983.

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UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor

A chopper drive which uses the inductance of the motor as the controlling element causes a temperature rise in the motor due to hysteresis and eddy current losses. For most motors, especially solid rotor constructions, this extra heat can force the designer to go to a larger motor and then derate it, or to a more expensive laminated construction in order to produce enough output torque for the job. Regardless of the motor type, *any* extra heat generated within a system will have to be removed or else other system components will be stressed unnecessarily. This could mean using a fan where convection cooling might otherwise have sufficed. In addition, the EMI generated from both the motor and its leads is of serious concern to the designer in view of ever-increasing EMI regulations.

These problems can be virtually eliminated by borrowing a simple technique from switching power supply designs, i.e., by placing a properly designed low-pass L-C filter across the output and using *this* L to control the UC3717. This removes the high frequency AC chopping losses in the motor by providing it with almost pure DC current. It also confines the EMI-causing, high frequency AC components to within the driver where they are easier to handle. This could allow increased wire lengths and possibly free up some design constraints, but remember that even though DC emits no EMI, the driver will still commutate the windings and can produce some components of frequency as high as 10 kHZ. The design of the L-C filter is straight-forward and its small additional cost can be recovered easily. The Unitrode UC3717, a complete chopper drive for one phase winding on a monolithic IC, makes the design job simple. The end result, a cooler running and EMI quieter step motor, can be achieved with just a few additional passive components.

Preliminary Considerations

For our analysis, we will use a "23" frame, bipolar motor with a solid rotor and the following specifications:

P_{max} =	9.0 Watts	= Maximum power dissipation at 25°C
V_{max} =	3.75 Volts	= Maximum voltage per motor phase at 25°C
I_{max} =	1.25 Amps	= Maximum current per motor phase at 25°C
R_m =	3.0 Ohms	= Resistance of one phase at 25°C
*L_m =	8.4 mH	= Inductance of one phase winding

*It should be noted that L_m, as given in a manufacturer's data sheet, is not always *true average* inductance as seen at high current in a circuit, but rather the inductance reading you would obtain from a low current inductance bridge. This value can differ from in-circuit inductance by a factor of 2 or more! The in-circuit inductance for this motor is 5.0 mH.

We begin by calculating the electrical time constant of one phase winding using the resistance value given above and the *actual* motor inductance:

$$\tau_m = \frac{L_m}{R_m} = \frac{5.0\ \text{mH}}{3.0\ \text{Ohms}} = 1.67\ \text{msec} \qquad (1)$$

If one were using a standard voltage drive then it would take approximately τ_m or 1.67 msec to reach the current level required for proper operation. This places a severe restriction on motor speed. Increasing the drive voltage will allow the motor to run faster but will cause it to draw too much current and overheat. Maximum motor speed may be increased by decreasing the time constant. Since L_m is fixed, the only parameter we can change is the effective value of R_m by placing a resistor in series with it. If we place a resistor 4 times R_m in series such that total R is 5 times R_m and increase the drive voltage by a factor of 5 then we will have reduced the time constant by a factor of 5 to 330 μsec and also increased both the maximum motor speed and maximum power output by a factor of 5 each. Unfortunately, we will have increased wasted power by a factor of 5 also.

The Chopper Drive

Using a chopper drive enables one to run at a higher voltage and thus reach proper operating current faster while still protecting the motor from excessive current that would otherwise flow due to the higher voltage. The high voltage is first applied across the motor winding and then, when I_{max} is reached, it is switched off. (If it were not switched off then the maximum current rating of the motor would be quickly exceeded.) The current is then allowed to circulate in a loop within the driver and motor for a fixed time period (t_{off}) after which the voltage is re-applied to the motor. The operating frequency, which is determined by both the motor inductance and t_{off} should be high enough that the resulting current ripple is small compared to the average DC current. Power efficiency is relatively high because there is no external resistor used.

Nothing is free in the world of physics, however, and the price one pays for the extra power output capability is an increase in wasted heat due to hysteresis and eddy current losses *within* the motor instead of in an external resistor. Being within the motor, it can now cause overheating as well as reliability problems. Since the excess heat increases rapidly with the overdrive ratio, this means that at low overdrive ratios (less than 5-to-1) there will be almost negligible heating, but at higher overdrive ratios (more than 10-to-1) the induced motor losses can become as great as, or actually exceed, the I^2R losses! By placing a low-pass L-C filter in the circuit these induced losses can once again become negligible. The L and C components selected should be capable of operating at frequencies of 25 kHz or higher without heating effects in the inductor core or inductive effects in the capacitor.

UC3717 and L-C Filter

Designing with the UC3717

Using a supply voltage (v_s) of 40 volts (approximately a 10/1 overdrive), the turn-on rise-time becomes:

$$t_{rse} = -\tau_m \times Ln\,(1 - V_m/V_s) = -1.67 \times 10^{-3} \times Ln\,(1 - 3.75 / 40)$$
$$= 164\ \mu sec \qquad (2)$$

or *an improvement of approximately 10-to-1 in speed capability.*

Using an off-time (t_{off}) of 30 μsec as suggested on the UC3717 data sheet and limiting current (I_w) to 850 mA establishes a voltage across the resistive component of the winding ($V_{w\text{-}on}$) during the "on" time of:

$$V_{w\text{-}on} = I_w \times R_w = .85 \times 3.0 = 2.55\ Volts \qquad (3)$$

and during the "off" time (due to a 2.6 volt drop across the upper transistor, as shown in the data sheet, and a 0.4 volt drop across the Schottky "catch" diode) of:

$$V_{w\text{-}off} = V_{transistor} + V_{diode} = 2.6 + 0.4 = 3.0\ Volts \qquad (4)$$

Since the voltage and current changes are small, we can substitute a resistance (R_e) equivalent to $V_{w\text{-}off}/I_w$ in series with R_w to adjust the time constant and allow us to calculate the approximate current ripple (ΔI_w) during t_{off}:

$$\Delta I_w = I_w \left(1 - \exp\left[\frac{-t_{off}(R_w + R_e)}{L_m}\right]\right)$$
$$= .85 \times \left(1 - \exp\left[\frac{-30x10^{-6} \times (3.0 + 3.5)}{5x10^{-3}}\right]\right)$$
$$= 33\ mA\ p\text{-}p \qquad (5)$$

Knowing ΔI_w, we can now calculate the on-time (t_{on}):

$$t_{on} = \frac{\Delta I_w \times L_m}{V_s - V_{w\text{-}on}} = \frac{33x10^{-3} \times 5x10^{-3}}{40 - 2.55} = 4.4\ \mu sec \qquad (6)$$

and can also find our operating frequency (f) by:

$$f = 1 / (t_{on} + t_{off}) = 1 / (4.4 + 30) \times 10^{-6} = 29.1\ kHz \qquad (7)$$

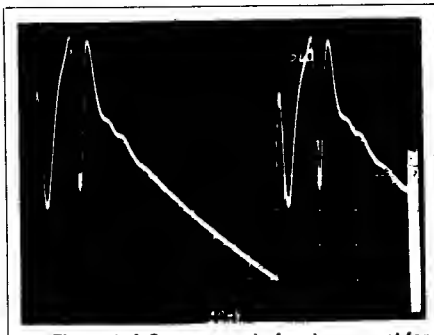

Figure 1. A-C component of motor current for standard chopper configuration.

Since this frequency is well above audible ranges, it will not cause any objectionable sound, but there are still the problems of EMI and excess motor heating to deal with. It is possible to generate EMI due to the current switching that occurs in the motor leads because they carry not only the primary frequency, but also many higher harmonics as well, so they require careful routing, shielding, or both. We can put in a low pass L-C filter to remove these high frequencies and still pass normal commutation currents without any significant loss of motor performance.

Design of the L-C Filter

Figure 2 is a block diagram of a motor connected to 2 UC3717s with the low-pass L-C filters in place.

Again we will use a current of 850 mA in each winding, an off-time of 30 μsec, and an on-time of 4.4 μsec but now we will use an

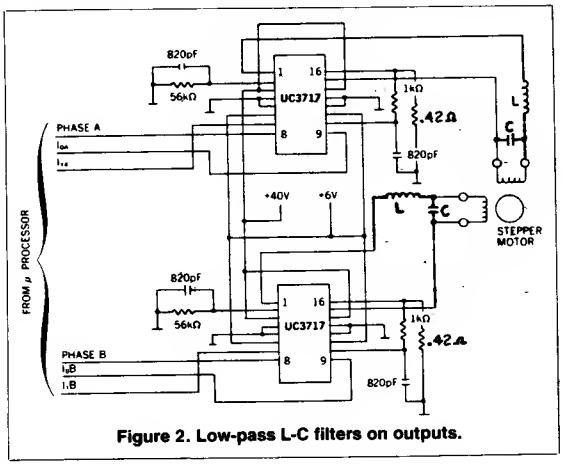

Figure 2. Low-pass L-C filters on outputs.

external inductance (L) to control the chopping. V_{drop} is the sum of the source (V_{so}) and sink (V_{si}) voltage drops at 850 mA:

$$V_{drop} = V_{so} + V_{si} + V_{sense} = (2.6 + 1.9 + 0.36)$$
$$= 4.9\ volts \qquad (8)$$

In order to minimize the effects of L on the motor current risetime we will make it 10 times smaller than L_m or 500 μH. In order to keep the peak current in the UC3717 below 1 amp we will use a 0.42 ohm sense resistor and also limit $_{\Delta}I_L$ to 300 mA. Using a variation of equation (6) we can check that:

$$L = \frac{(V_s - V_{drop}) x\ t_{on}}{{}_{\Delta}I_L} = \frac{(40 - 4.9) \times 4.4x10^{-6}}{300x10^{-3}} = 515\ \mu H \qquad (9)$$

is in keeping with the constraints outlined above.

Similarly, we would like to find a value for the capacitor (C) such that it will have less than 1/10 the impedance of L at 29.1 kHz:

$$C = \frac{10}{(2 \times \pi \times f)^2 \times L} = \frac{10}{(2 \times 3.14 \times 29100)^2 \times 500x10^{-6}} \qquad (10)$$
$$= 0.6\ \mu F$$

The test motor and driver, operated unloaded (nothing connected to the output shaft) and in the configuration of *Figure 2*, used values of 500 μH for the inductor and 0.47 μF for the capacitor. *Figure 1* and *Figures* 3 through 6 are waveforms obtained from that motor.

The lower trace of *Figure* 3 (*Figure* 3*b*) shows the 330 mA current sawtooth in the inductor, while the upper trace (*Figure* 3*a*) shows an 8 mA p-p current ripple in the motor winding. While this may seem to indicate only a 12 dB reduction in EMI over *Figure 1*, comparing the *sinusoidal* waveform of *Figure* 3a to the "noisy" *sawtooth* waveform of *Figure 1* will quickly point out sources of

9

UC3717 and L-C Filter

EMI. In *Figure 1*, the oscillations immediately following each switch of the driver are due to the motor's distributed capacitance resonating with its inductance and are a possible source of EMI. In addition, sharp current spikes are allowed to pass along the motor leads and through the motor's distributed capacitance unhindered, thus creating high frequency EMI. EMI spikes were virtually eliminated from *Figure 3a* by using a low ESR capacitor and connecting the motor leads close to the body of the capacitor.

Figure 4 shows motor current superimposed over the inductor current. Just to the left of the center graticle line a ringing occurs in the inductor current that also appears in the motor current, although attenuated. This ringing occurs at a frequency of:

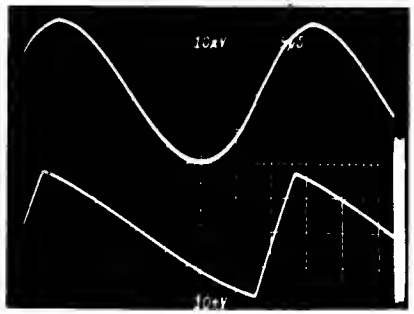

Figure 3. Motor end inductor current waveforms.

$$f_{res} = 1 / 2\pi\sqrt{L \times C} = 1 / 6.28 \times \sqrt{500\times10^{-6} \times 0.47\times10^{-6}}$$
$$= 10.4 \text{ kHz} \quad (11)$$

which is the resonant frequency of the L-C filter. This frequency can be lowered by increasing the value of either L or C, although at a cost of reducing the high speed performance of the motor.

The high frequency sawtooth waveforms at the upper, flat portion of the motor current waveform are the 29.1 kHz chopping currents in the inductor. They cause a small corresponding ripple in the motor current but, because the chopping frequency is more than twice the break frequency of the 2-pole L-C filter, we would expect, and can see, an attenuation greater than 12 dB.

In a 2 phase step motor (sometimes referred to as a 4 phase step motor because of the 4 windings used in the unipolar version) the STEP RATE, in full steps per second (FSPS), is 4 times the primary frequency of the motor current waveform. The two phases of the step motor are operated in quadrature and thus will generate 4 distinct states in the 2 phases which correspond to 4 mechanical steps for each electrical cycle.

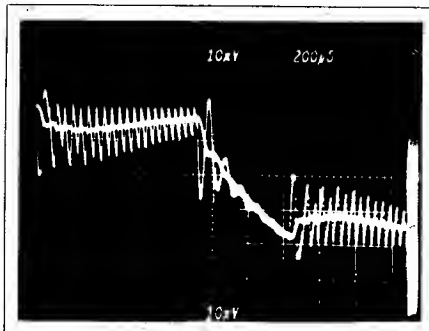

Figure 4. Filter current weveform superimposed over motor current weveform.

FSPS = 4 x frequency (for a 2 or "4" phase step motor) (12)

It is important to note at this time that 10.4 kHz is the highest *frequency* that can be passed to this motor without attenuation using the selected components, but that this corresponds to a *step rate* of 41,600 FSPS! The test motor was able to run at 17,000 full steps per second with the L-C filter in place, which is high enough for most situations.

Figures 5 and *6* are current waveforms for the motor running at 1600 FSPS and 16,000 FSPS respectively. The motor was operated with the L-C filter on only the lower trace winding so that the waveforms could be compared easily. Looking at *Figure 5*, one can see that the leading edges of both waveforms have the same risetimes, although the filtered one has more suscepibility toward ringing. From *Figure 6*, one can see that torque is down only 3 dB at 16,000 FSPS and that there are "glitches" in the unfiltered waveform that do not appear in the filtered waveforms.

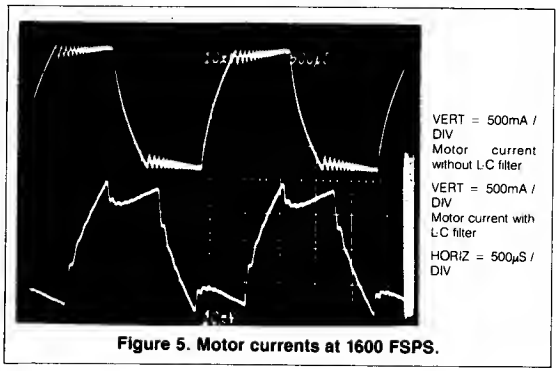

Figure 5. Motor currents at 1600 FSPS.

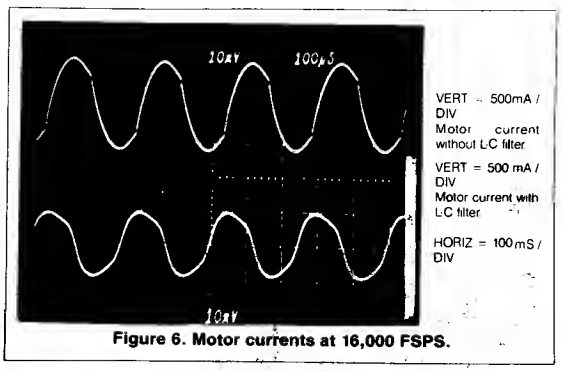

Figure 6. Motor currents at 16,000 FSPS.

Conclusions

The use of a low-pass filter can be an effective heat and EMI reduction mechanism when used with a step motor chopper driver such as the UC3717. The price one pays for a "clean" EMI environment is a *small* loss in very high speed performance. The technique may be applied equally well to non-IC chopper drivers but the peak currents must be accounted for and the minimum value of L adjusted accordingly. 500 µH is the smallest practical L that should be used with the UC3717 since we do not want the

UC3717 and L-C Filter

peak of the ripple to exceed 1.0 amps. This limits the usefulness of the technique to motors with inductances of 2 mH or more. At average currents less than 300 mA, the value of L may have to be larger in order to maintain continuous current in the inductor, but the physical size may be decreased. If an average current in excess of 850 mA is required, then a power amplifier may be added as shown in *Figure 7*. This will extend the peak current capabilities of the chopper drive to higher current and will also allow the value of L to be decreased.

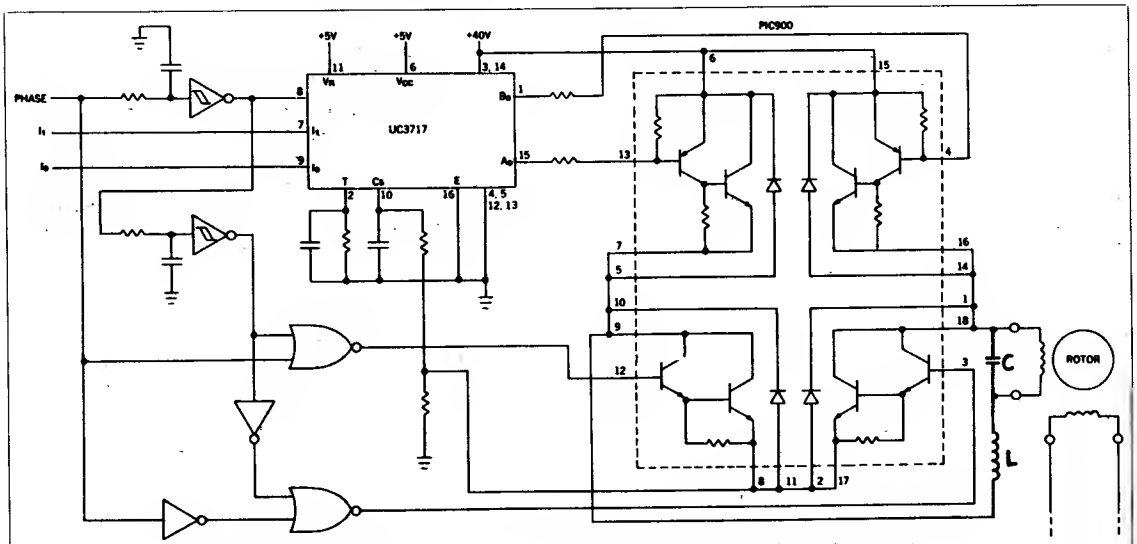

Figure 7. UC3717 chopper drive with PIC900B Power Ampilfier on one phase of step motor.

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UC3842/3/4/5 PROVIDES LOW-COST CURRENT-MODE CONTROL

INTRODUCTION

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845. Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

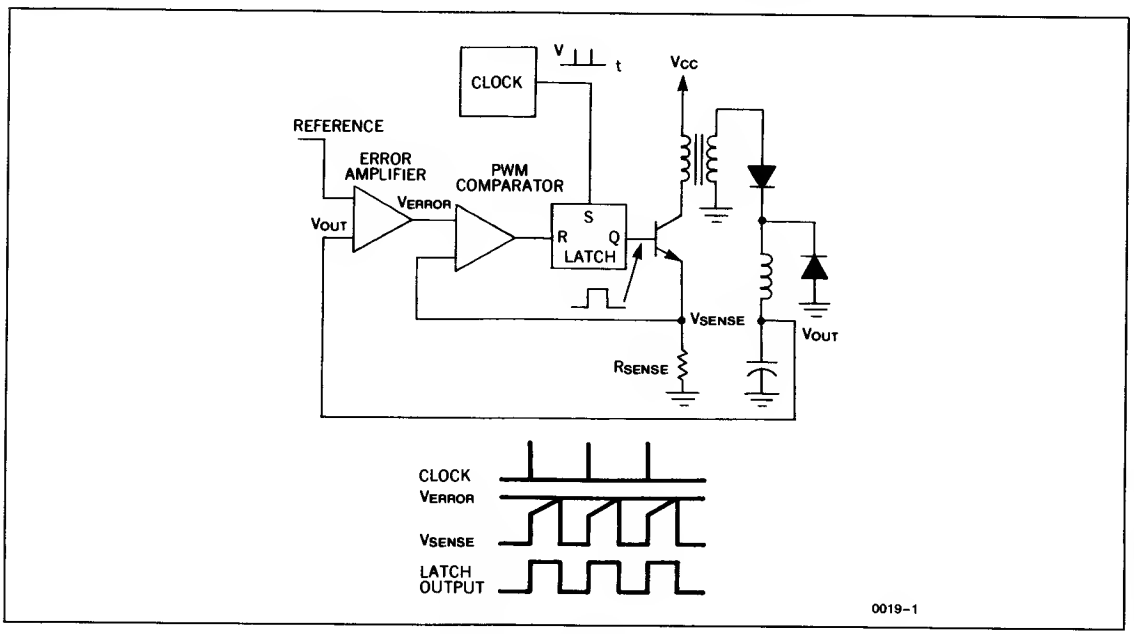


Figure 1. Two-Loop Current-Mode Control System

error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

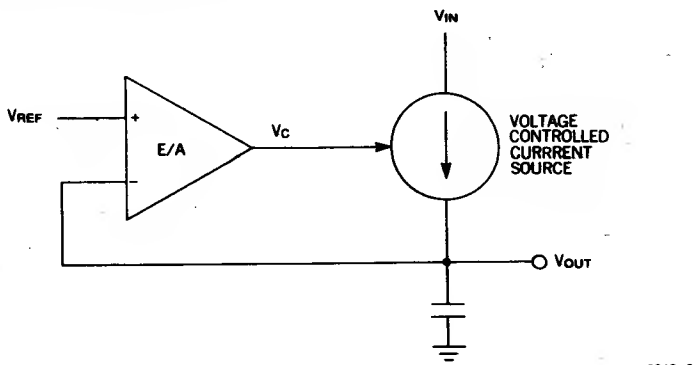
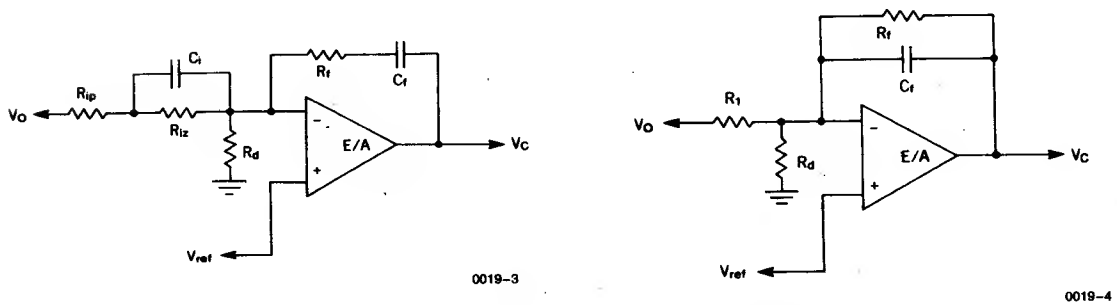


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control **B) Current Mode Control**

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

9

THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

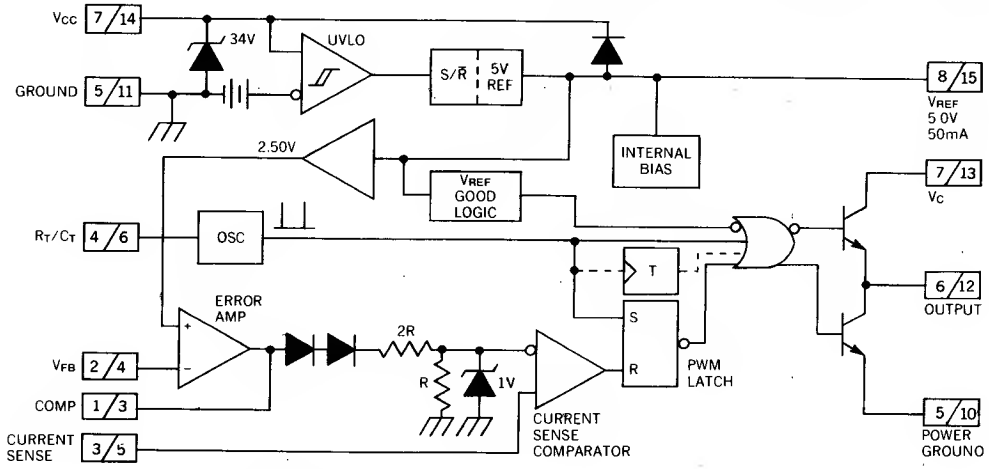
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



Note: 1. A/B A= DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

Figure 4

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.

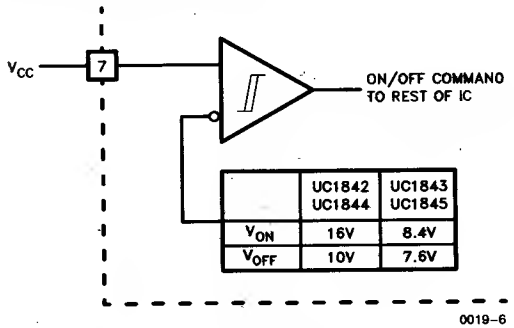


Figure 5.

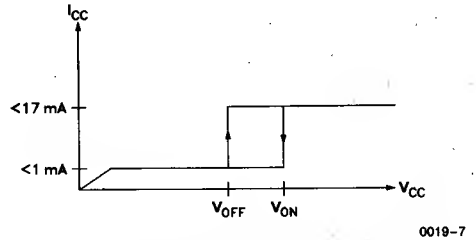


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor C_T is charged from V_{REF} (5V) through the timing resistor R_T, and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of C_T for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72 / (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

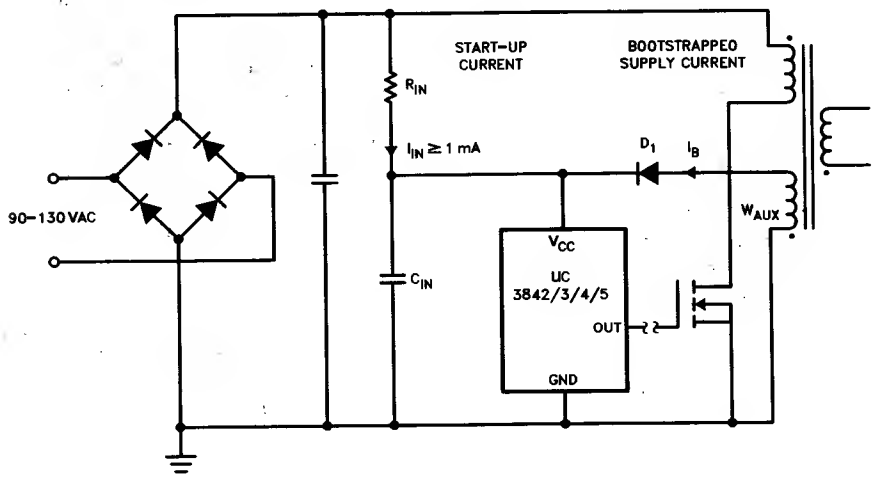


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

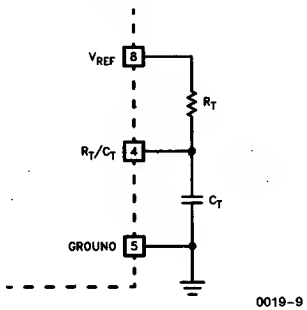


Figure 8

Deadtime vs C_T (R_T > 5k)

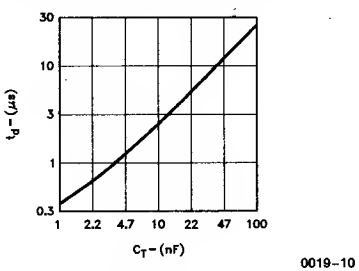


Figure 9

Timing Resistance vs Frequency

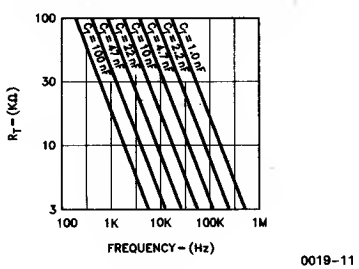


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as **Figure 11** illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_S}$$

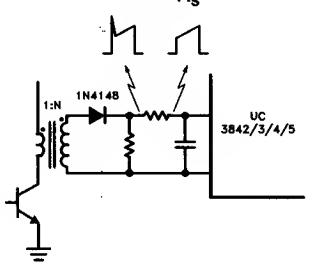


Figure 11. Transformer-Coupled Current Sensing

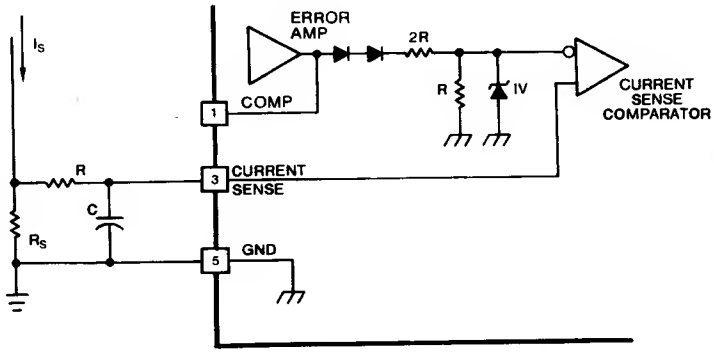


Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = 1/2\pi\ R_F C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

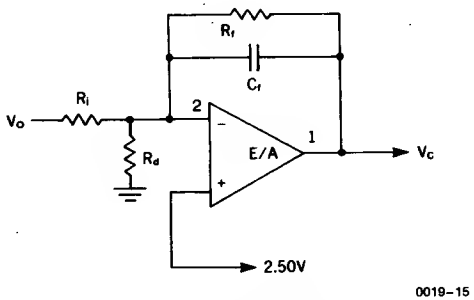


Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

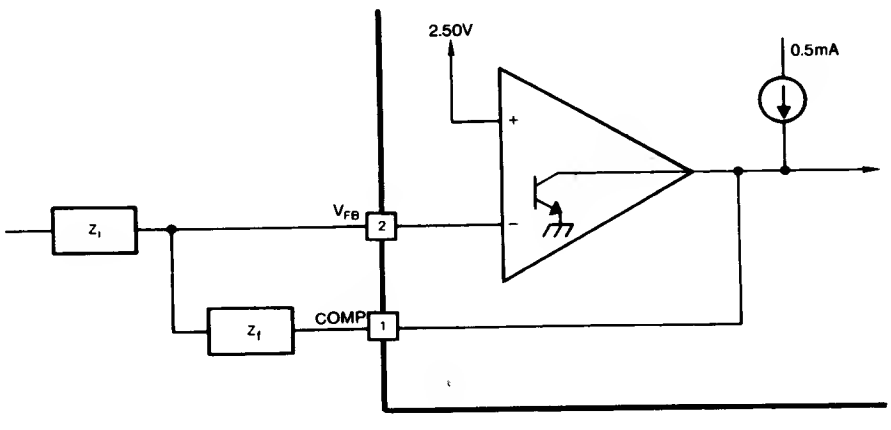


Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I, resulting in a DC error in output voltage (V_O) given by:

$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I$,

It is therefore desirable to keep the value of R_I, as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ±1 amp peak for driving MOSFET gates, and a ±200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most 1- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

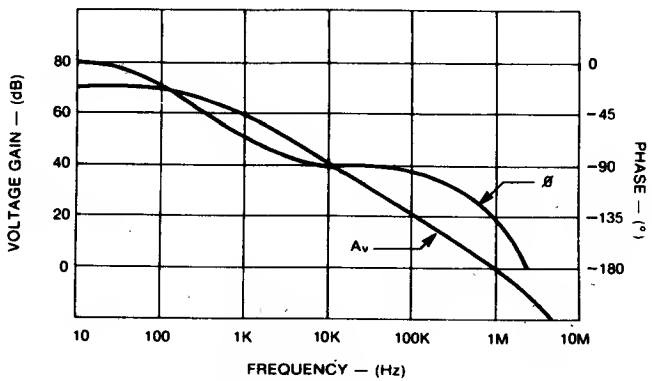


Figure 15. Error Amplifier Open-Loop Frequency Response

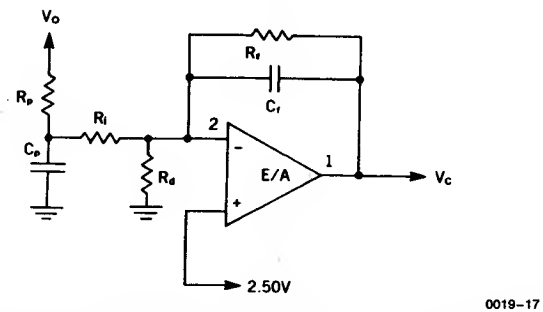


Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ±1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

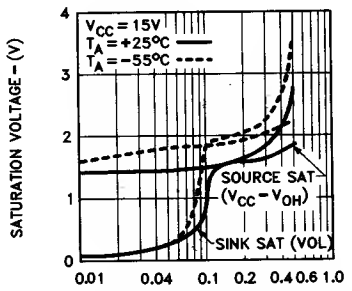


Figure 17. Output Saturation Characteristics

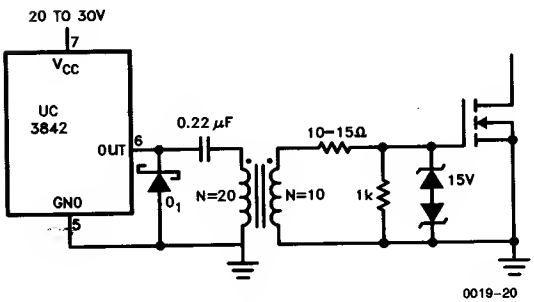


Figure 19. Isloated MOSFET Drive

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

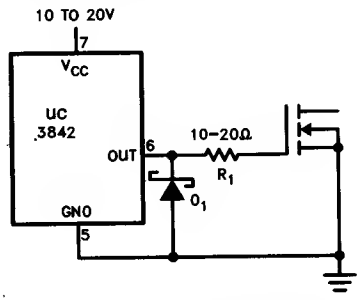


Figure 18. Direct MOSFET Drive

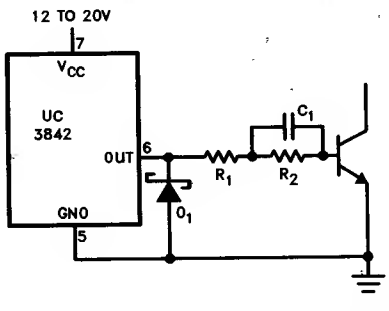


Figure 20. Bipolar Drive with Negative Turn-Off Bias

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 21 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 31 results in an R_T/C_T waveform like that of Figure 21B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

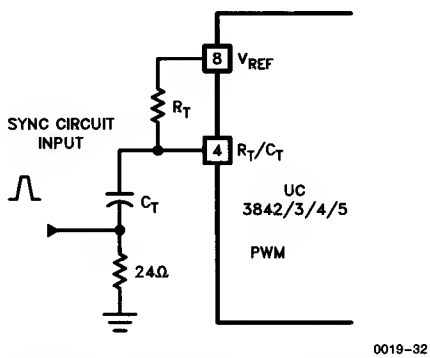


Figure 22. Sync Circuit Implementation

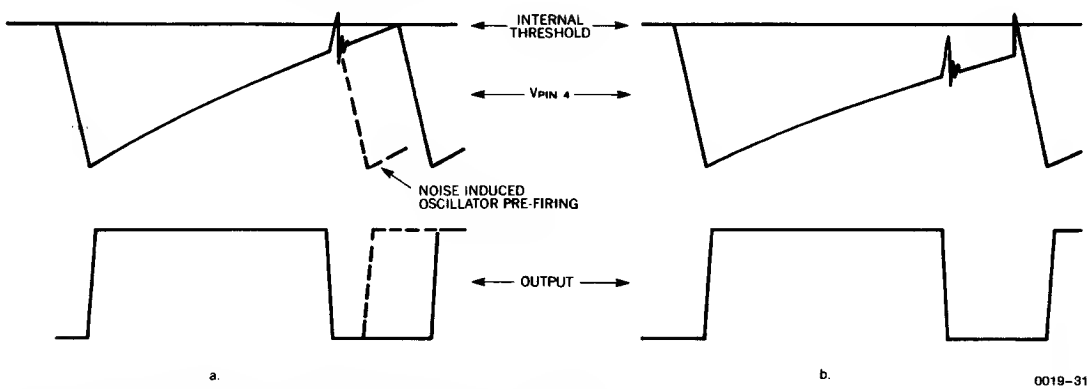


Figure 21. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

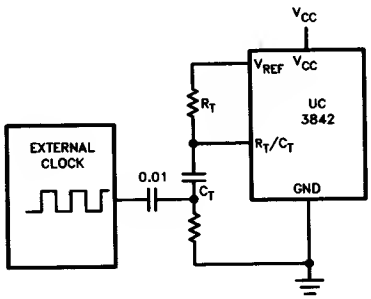
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in "Practical Considerations in Current Mode Power Supplies" listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 23.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a "dead" or off time for the output.

A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



$D_{Max} = t_L / (t_H + t_L)$
$t_H = 0.693 (R_A + R_B) C$
$t_L = 0.693 R_B C$

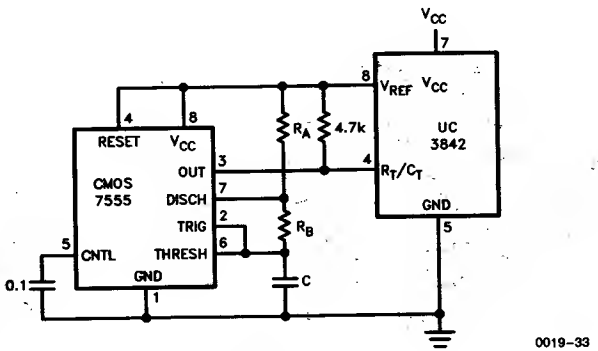


Figure 23

Synchronization to an External Clock

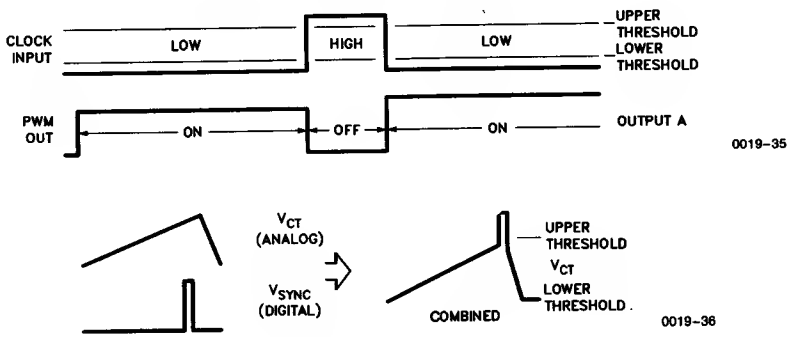


Figure 24

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 25 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave(s). The photos shown in Figures 26 and 27 depict the circuit waveforms of interest.

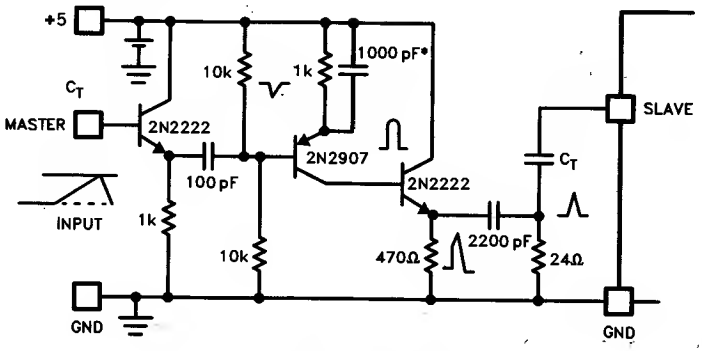
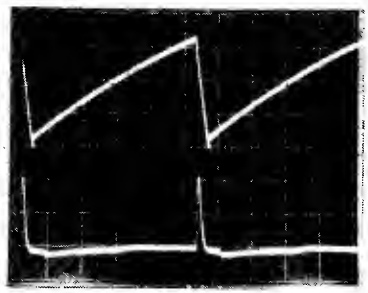


Figure 25. Sync Pulse Generator Circuit



Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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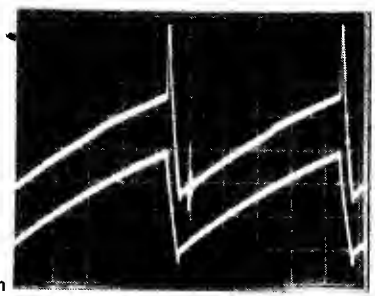
Figure 26. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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Figure 27. Master/Slave Sync Waveforms at C_T

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up
$V_O \approx 2 \times V_{IN}$

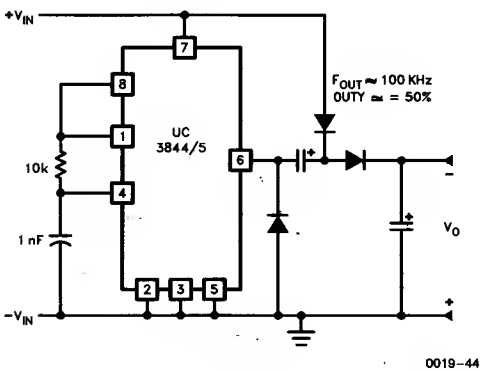

Figure 28

Inverting
$V_O \approx -V_{IN}$

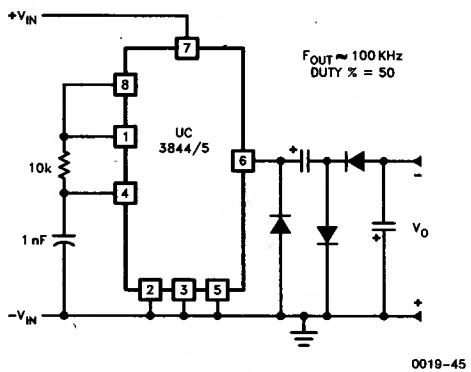

Figure 29

Low Power Buck Regulator—Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see "Closing The Feedback Loop", Buck Topology.

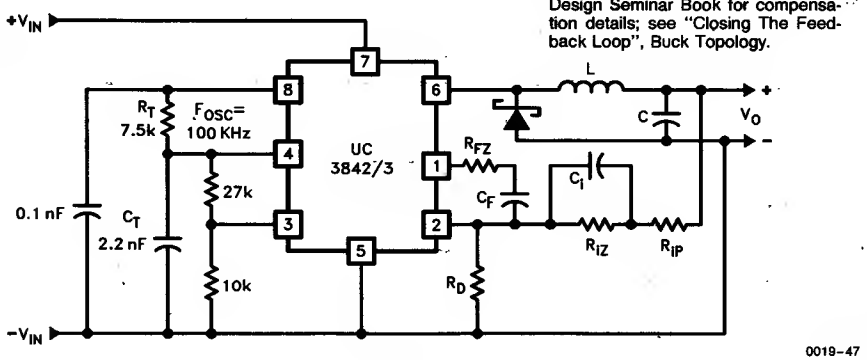

Figure 30

9

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 31 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

Also consult UNITRODE application note U-96 in the applications handbook.

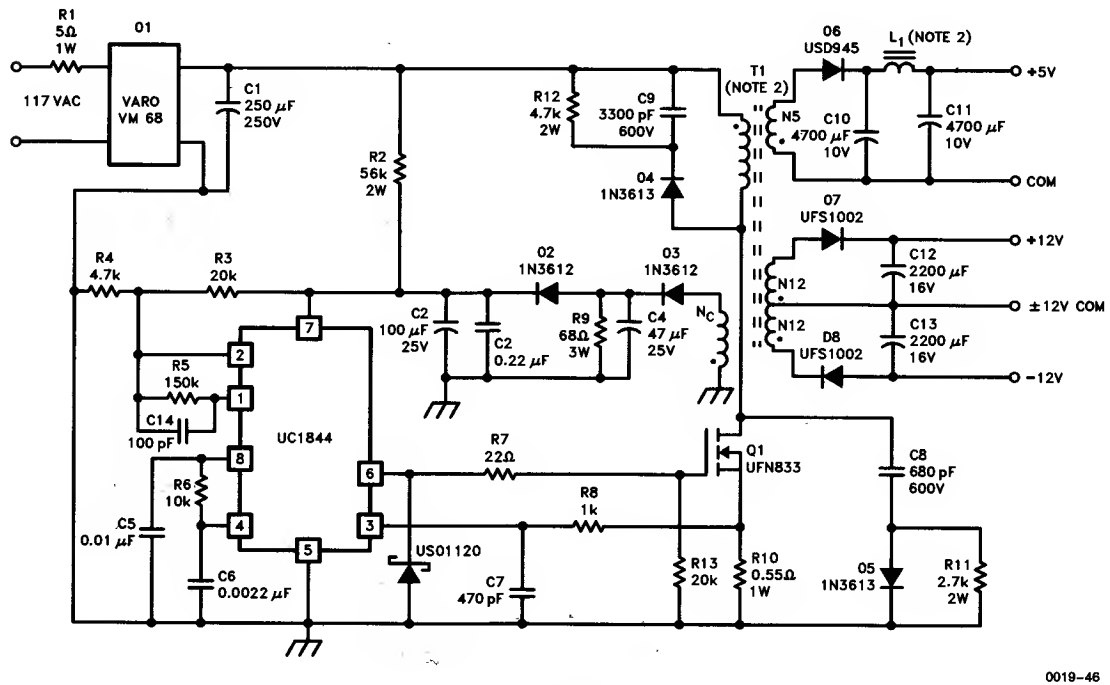

Figure 31

Power Supply Specifications

1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50 mV P-P Max.
   - B. +12V, ±3% 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.
   - C. −12V ±3%, 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.

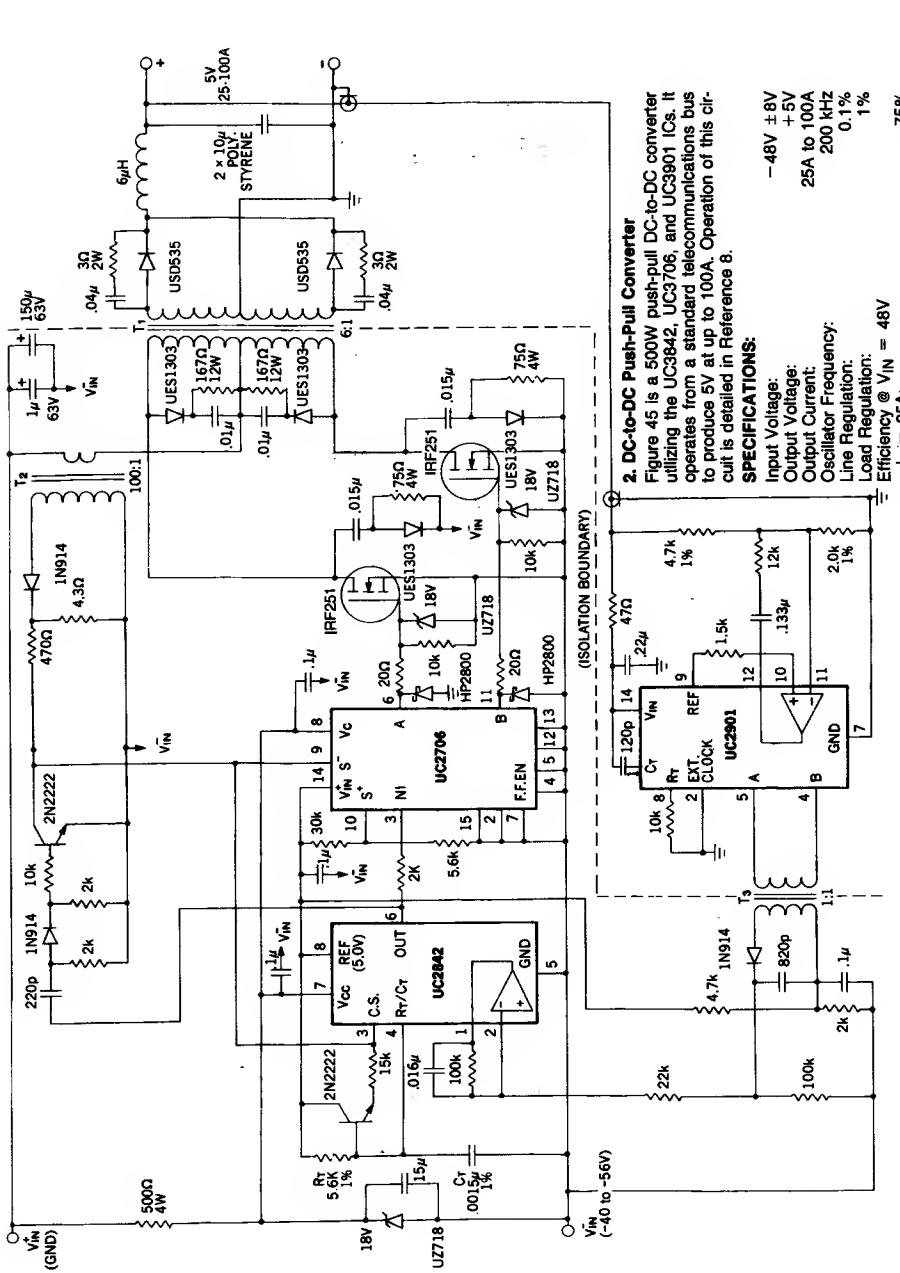

Figure 32. 500W Push-Pull DC-to-DC Converter

9

UC1637/2637/3637 SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

INTRODUCTION

There is an increasing demand today for motor control circuits, as a result of the incredible proliferation of automated position control equipment, which is itself made possible by recent developments in the field of digital computation.

The UC1637 Switched Mode Controller for DC motors is one of several integrated circuits offered by Unitrode for motor controls. This Application Note presents the general principles of its operation and the circuit details that optimize its use. As an illustration we will carry out an actual design, which will involve not only the UC1637, but also a power H-bridge using MOSFET transistors, and a modern DC motor tachometer. Using the tach output and UC1637's error amplifier, we will close the velocity control loop after a brief analysis of the factors that affect the feedback loop stability.

To achieve high efficiency power amplification, the UC1637 uses pulse width modulation, or PWM. This technique is employed today in many different circuits where power losses must be minimized, and is most suitable in applications involving inductive loads such as motors, voice coils, etc.

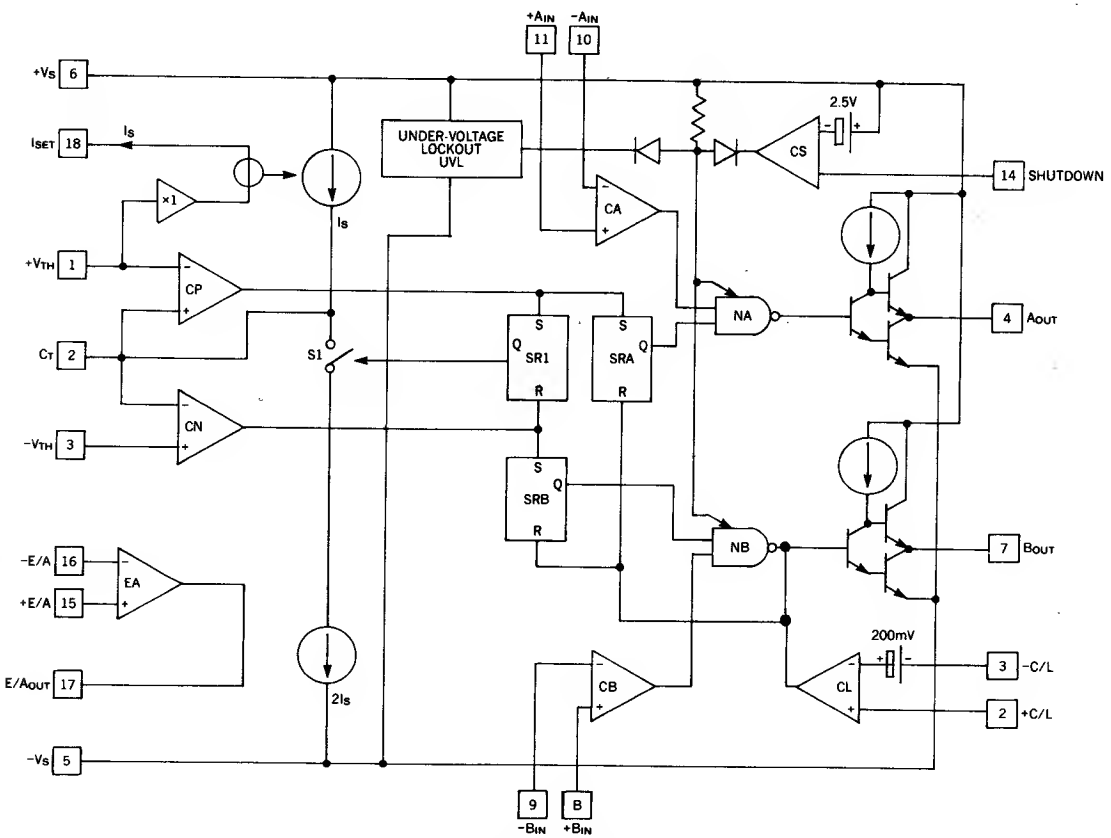

FIGURE 1. BLOCK DIAGRAM OF UC1637.

PULSE WIDTH MODULATION (PWM)

The function of a power amplifier is to regulate the flow of energy from a power supply to a load, under the control of an input signal. A linear amplifier does this by interposing a controlled voltage drop in series with the load, while carrying the full load current. The product of this voltage and current represents the amount of power that must be dissipated by the amplifier itself, and it is easy to see that the method is not very efficient. In fact, its usefulness diminishes rapidly as the amount of power to be controlled increases and, at some point, a more efficient method becomes imperative.

PWM is a switching technique in which the supply voltage is fully applied (switched) to the load and then removed, the "on" and "off" times being precisely controlled. The effect on the load is the same as if some lower voltage were continuously applied whose value depended on the duty-cycle, that is, the ratio of "on" time to the full switching period. Since supply current only flows during the "on" times, it is apparent that the efficiency should be much higher than in the linear amplifier, as in fact it is. Still, switching transistors have small but finite "on" voltages and transition times, all of which introduce losses, which limit practical PWM efficiencies to something between 75% and 90%.

THE UC1637

The diagram of Figure 1 shows in block form the internal organization of the device. The main functions are:

A) Triangular wave generator; CP, CN, S1, SR1
B) PWM comparators; CA, CB
C) Output control gates; NA, NB
D) Current limit; CL, SRA, SRB
E) Error amplifier; EA
F) Shutdown comparator; CS
G) Undervoltage lockout; UVL

The two output lines, A_{OUT} and B_{OUT}, are meant to drive the two legs of an H-bridge power amplifier, with the load driven in bipolar fashion. The A_{OUT} and B_{OUT} outputs themselves are rated at 500mA peak and 100mA continuous, which makes it easy to interface the device with most amplifiers.

In order to generate two PWM output signals, we first produce a triangular waveform, or linear ramp. This is done by charging a capacitor C_T (pin 2) with constant current I_S until the comparator CP, with a fixed threshold voltage of $+V_{TH}$, delivers a pulse to "set" the SR1 latch circuit. This forces Q high, which closes the switch S1 and adds a negative current, $2\times I_S$, to the node of pin 2. As a result, a net current equal to I_S now flows out of C_T, discharging it linearly until the comparator CN resets SR1, and the cycle restarts. Thus, the voltage at pin 2 ramps continuously between $-V_{TH}$ and $+V_{TH}$ at a frequency that depends on these two threshold voltages, on C_T, and on I_S.

The current I_S is programmed by means of a resistor connected to pin 18. The voltage at this pin is equal to $+V_{TH}$ and an internal current mirror forces the charging current I_S to be equal to the current flowing out of pin 18. If a resistor R_S is connected from pin 18 to $-V_S$ (pin 5) instead of to ground, the ramp frequency becomes independent of power supply voltage variations, since I_S will then change together with V_{TH}.

As Figure 2 shows, a triangular waveform can be compared with a reference voltage to generate a PWM signal. The UC1637 uses two separate comparators to generate the two output signals A_{OUT} and B_{OUT}. The way the signals are handled, and the results, are shown in Figure 3 where it can be seen that the difference between V_A and V_B is the cause of the time intervals during which both outputs are low.

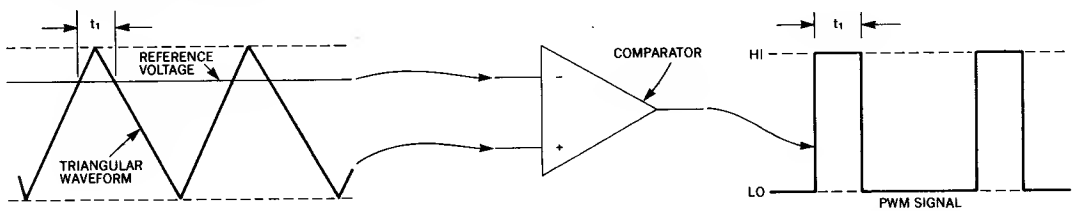

FIGURE 2. HOW A PWM SIGNAL IS GENERATED.

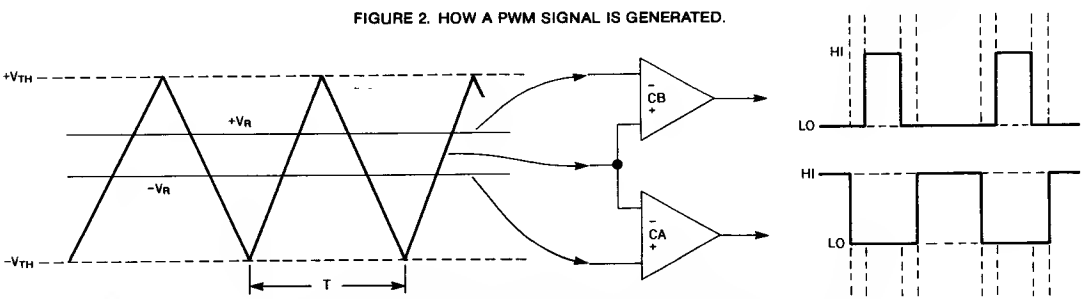

FIGURE 3. TWO PWM SIGNALS ARE GENERATED IN THE UC1637.

The two nand gates, NA and NB, will be enabled if the following two conditions are met:

A) supply voltage $+V_S$ is greater than +4.15 volts (typ)
B) the shut-down input line (pin 14) is at least 2.5 volts (typ) negative with respect to $+V_S$.

If these are satisfied, the A_{OUT} output line will be high if the CA output *and* Q of SRA are both high. Since SRA is set at each positive peak of the oscillator ramp, the output A_{OUT} can be controlled by CA singly — as long as a current-limit pulse from CL does not occur. The operation of the NB gate is similar.

The timing diagrams of Fig. 4 show the sequence of events before and after a current limit pulse occurs. Before time t_1 the PWM action is smoothly controlled by the ramp comparisons with V_A and V_B. The pulse from CL at time t_1 resets both SRA and SRB; the output lines are now disabled until SRA is set (at time t_2) and SRB is set (at time t_3).

The current limit comparator CL provides a means to protect both driver and motor from the consequences of very high currents. If the current delivered by the driver to the motor is made to flow through a low value resistor (for example, see R_S in Figure 7) the voltage drop across this resistor will be a measure of motor current. This voltage is applied between pins 12 and 13 of the UC1637, with pin 12 positive. A 200mV threshold is provided internally (see Figure 1) so that when the R_S voltage is equal to 200mV, the output of CA goes high, resetting both SRA and SRB and, consequently, terminating any active output pulse. This pulse-by-pulse method of current limiting is very fast and provides effective protection, not only for the driver components, but also for the motor, where the possibility of demagnetization due to excessive current is a matter of serious concern.

Finally, the UC1637 contains also an operational amplifier, EA, that can be used to provide gain and phase compensation, as will be seen later.

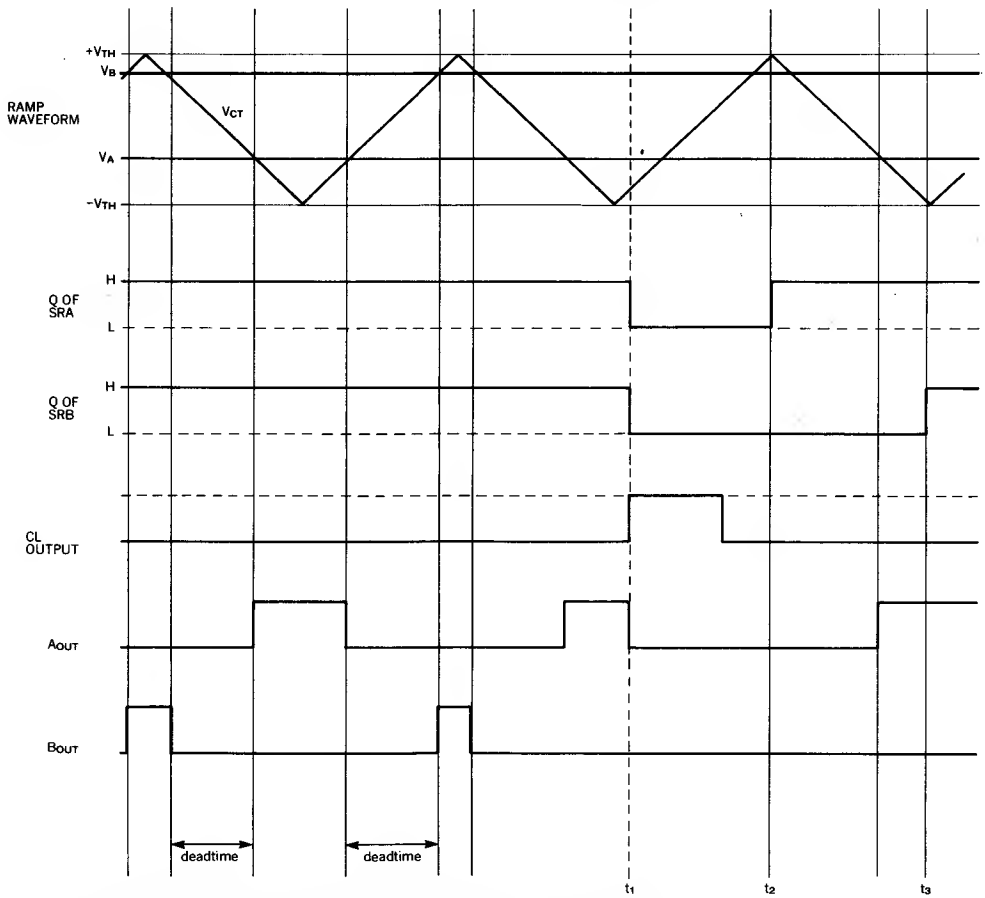

FIGURE 4. TIMING DIAGRAM SHOWING THE GENERATION OF PWM PULSES AT A_{OUT} AND B_{OUT}.
BEFORE TIME t_1, THE Q OUTPUTS OF SRA AND SRB ARE BOTH HIGH AND THE OUTPUT PULSES ARE CONTROLLED BY THE RAMP INTERSECTIONS WITH V_A AND V_B. AT TIME t_1, THE CURRENT LIMIT COMPARATOR HAS SENSED EXCESS CURRENT AND THE CL OUTPUT HAS GONE HIGH, RESETTING BOTH SRA AND SRB. THIS TERMINATES THE A_{OUT} PULSE THAT WAS ACTIVE AT THE TIME. A_{OUT} CAN RESUME ONLY AFTER SRA IS SET AT t_2; B_{OUT} CAN RESUME ONLY AFTER SRB IS SET AT t_3.

Figure 5 shows the connections needed to get the ramp generator and the two comparators ready to go. There is no great difficulty in calculating values for the various resistors, which are no more than two simple voltage dividers. Still, certain things should be considered before proceeding.

The input impedance R_{IN}, seen by the control voltage V_C will be

$$R_{IN} = \frac{R_3 + R_4}{2} \quad (1)$$

and this value may be specified or determined in advance. Also, it would be economical to have a minimum number of different values of resistors. If we make

$$R_1 = R_3 \quad (2)$$

we will have four resistors of equal value in the final circuit.

There is also the question of deciding on the separation V_G between the reference voltages $+V_R$ and $-V_R$. The voltage gain of the PWM amplifier will have one of the four characteristics depicted in Figure 6, depending on your choice of reference voltage separation. You can get a linear response by making $V_G = 0$, as in Curve #1, or by making $V_B - V_A = 2V_{TH}$, as in Curve #3. In Curve #2, there is a change in slope due to the contribution, near zero, of both V_A and V_B to the output changes, which in some systems may be undesirable, but which may be of interest due to the fact that it results in zero losses at null.

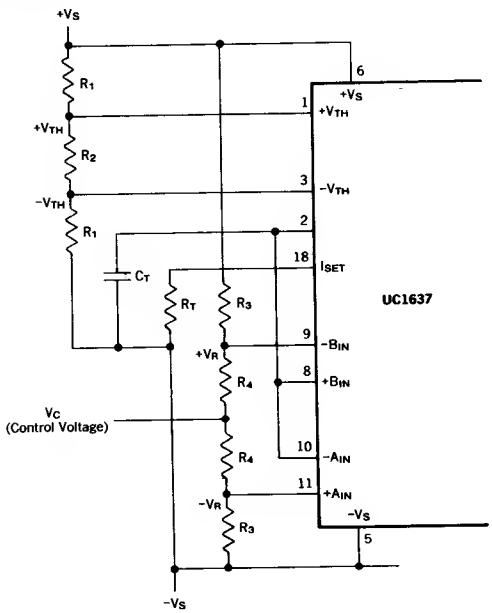

FIGURE 5. SETTING UP THE A AND B COMPARATOR INPUTS.

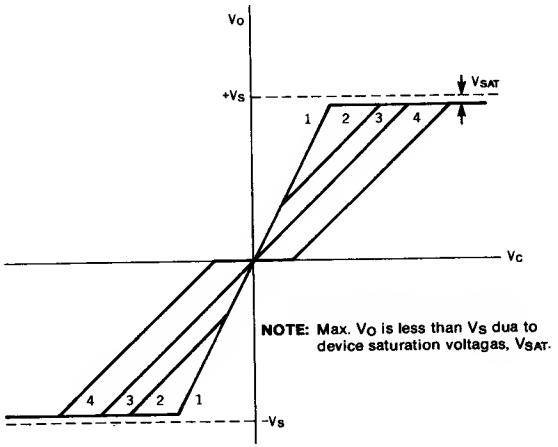

FIGURE 6. PWM VOLTAGE GAIN CHARACTERISTICS OBTAINABLE WITH VARIOUS VALUES OF REFERENCE VOLTAGE SEPARATION, OR GAP VOLTAGE 2 V_R.
1. LINEAR GAIN WITH $V_R = 0$ ($a = 0$).
2. NON-LINEAR GAIN WITH V_R GREATER THAN ZERO BUT LESS THAN V_{TH} ($0 < a < 1$).
3. LINEAR GAIN WITH $V_R = V_{TH}$ ($a = 1$).
4. NON-LINEAR GAIN WITH V_R GREATER THAN V_{TH} ($a > 1$).
NOTE: THE SLOPE OF LINE 1 IS TWICE THAT OF LINE 3.

At this point, this choice of PWM gain characteristic amounts only to the choice of the ratio between V_R and V_{TH}:

$$a = \frac{V_R}{V_{TH}} \quad (3)$$

The values of V_{TH} and V_R, as well as R_3 and R_4, depend on the following:

- $\pm V_S$: power supply voltages
- R_{IN}: desired control input resistance
- $V_C max$: peak value or input voltage V_C. This is the input voltage at which the output reaches 100% duty cycle
- a: ratio of V_R to V_{TH}

These values being known, the designer can proceed to calculate the following circuit values:

$$R_3 = \frac{2\,R_{IN}\,V_S\left(1 + \frac{1}{a}\right)}{V_C max + V_S\left(1 + \frac{1}{a}\right)} \quad (4)$$

$$R_4 = 2\,R_{IN} - R_3 \quad (5)$$

$$V_A = \frac{V_S R_4}{2 R_{IN}} \quad (6)$$

$$V_{TH} = \frac{V_R}{a} \quad (7)$$

$$R_2 = 2 R_3 \frac{V_{TH}}{V_S - V_{TH}} \quad (8)$$

and, from Eq. (2), $R_1 = R_3$.

Having chosen a frequency f_T for the PWM timing circuit, you can now calculate C_T and R_T. A suitable starting value for the charging current I_S is 0.5mA which gives

$$R_T = \frac{V_S + V_{TH}}{.0005} \quad (9)$$

$$C_T = \frac{.0005}{4 f_T V_{TH}} \quad (10)$$

You will probably need to make an adjustment here, so as to get a standard value for capacitor C_T, and it is best to keep I_S in the range from 0.3mA to 0.5mA when you do this.

It may be desirable, or even necessary in some conditions, to bypass the $+V_{TH}$ and $-V_{TH}$ inputs to ground, and for this, ceramic capacitors of 0.1μf should be adequate. Remember also that terminal 14, the shut-down line, must be held "low" (at least 2.5V below the positive rail) in order to enable the drive. With an external switch to ground, or to $-V_S$, and a pull-up resistor to $+V_S$, this line can be used to enable (low), and disable (high), the output. Both A_{OUT} and B_{OUT} will be low when the shut-down line is high.

The next step is to connect the UC1637 to a suitable power amplifier, and the amplifier to the motor. The UC1637 has provisions for current limiting, as discussed earlier, and you must make arrangements to develop a voltage proportional to motor current at the driver side. This can be done by adding to an H-bridge a low value resistor in series with rail connections. The current limit comparator has a common mode range that reaches all the way down to the negative rail (on the positive side the limit is 3V below the positive rail). A resistor R_S is then added at the bottom of the bridge, and its value is selected so as to give a voltage drop to 200mV when the desired limit current flows.

$$R_S = \frac{.2}{I_{MAX}} \text{ (ohms)} \quad (11)$$

where I_{MAX} is the maximum desired motor current in amperes. In a breadboard, a twisted pair of wires should be used to make the connection from this resistor to pins 12 and 13, and an RC filter should be added, as shown in Figure 7.

On a PC board, it is a good idea to keep R_S close to the UC1637 to minimize the length of the connecting traces. The RC filter should still be used.

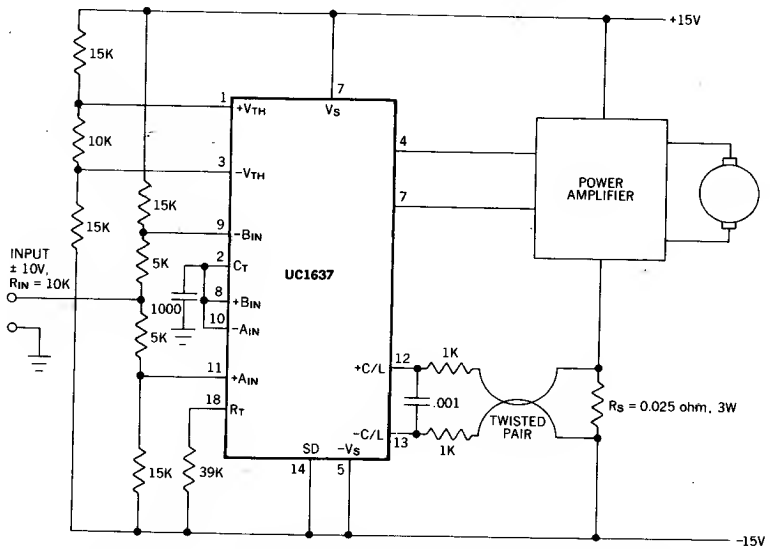

FIGURE 7. CIRCUIT DIAGRAM OF PWM VOLTAGE AMPLIFIER WITH GAIN OF 3.

AN EXAMPLE

We are ready now to design a current limited, PWM voltage amplifier to drive a small DC servomotor. Here are the requirements:

Supply voltages: ±15V
Input: ±10V max.; 10K input res.
PWM frequency: 30KHz
Motor current limited at 8A
Minimum power losses at idle

We have:
$V_S = 15V$
$V_C max = 10V$
$R_{IN} = 10^4$ ohm
$f_T = 3 \times 10^4$ Hz
and $I_{MAX} = 8A$

and also, from the last requirement, a = 1.

FROM EQUATIONS

(4) $$R_3 = \frac{2 \times 10^4 \times 15 \times 2}{10 + 15 \times 2} = 15K$$

(5) $$R_4 = 2 \times 10^4 - 15 \times 10^3 = 5K$$

(6) $$V_R = \frac{15 \times 5 \times 10^3}{2 \times 10^4} = 3.75V$$

(7) $$V_{TH} = 3.75V$$

(8) $$R_2 = (2 \times 15 \times 10^3) \times \frac{3.75}{15 - 3.75} = 10K$$

(9) $$R_T = \frac{15 + 3.75}{.0005} = 37.5K$$

and of course, $R_1 = R_3 = 15K$.

(10) $$C_T = \frac{.0005}{4 \times 30 \times 10^3 \times 3.75} = 1.11 \times 10^{-9} fd$$

If we settle for R_T = 39K, I_S becomes slightly less than 0.5mA and if we then pick C_T = 1000pf, the nominal frequency becomes 32KHz.
To limit the motor current at 8A, we need, from Eq. 11,

$$R_S = \frac{.2}{8} = 0.025 \text{ ohm}$$

The peak power in the resistor will be

$P_S = 8^2 \times .025 = 1.6$ watts.

Incidentally, the voltage gain of the amplifier can be determined from the fact that a 10V change at the input results in a 30V change at the output; therefore, the gain from input to motor terminals is 3. The above circuit is shown in Figure 7.

THE POWER AMPLIFIER

Where space is tight and motor current is less than five amperes, the Unitrode PIC900 offers a perfect solution to your power bridge design. This device comes in a DIL-18 package, requires only 5mA of input drive current, and is rated at 5A absolute maximum output current. It contains all you need for the output H-bridge — including the circulating diodes — and with only a few added parts, you are ready to go. A circuit diagram showing a velocity feedback loop using one UC1637 and one PIC900 appears in the UC1637 data sheet.

For higher currents, you will have to design your own amplifier, and for the purposes of this application note, a sample design is shown in Figure 8. Referring to that circuit, note that with $+V_S$ and $-V_S$ applied, if the inputs are left open, the power MOSFETs are all "off". If Drive A, for example, is driven to within 3.6V of either power rail, then the corresponding output is switched to that rail. Note that since the PNP and NPN junction transistors are by nature faster switching "on" than "off", while the MOSFETs are much faster than the junction transistors driving them, this connection provides a simple guarantee against cross-conduction. Also working toward this goal is the fact that the junction transistor can discharge the MOSFET's input capacitance faster than the 1K, 1W resistor can charge it. The arrangement shown in Figure 8 results in a transition time of about 1.5μS during which both MOSFETs in a given leg are off. This amount of time is a very small portion of the 33μS period toward which we are designing our example.

The power MOSFET transistors, in TO-220 package, are rated at 60V and 12A. The channel "on" resistance is quite low, 0.25 ohms at 8A, for the UFN533, resulting in low thermal losses. You can easily find other devices with even lower R_{DS} values, if needed, but as always, the price you pay is that you must pay the price.

Finally, a word about circulating diodes — conspicuous in Figure 8 by their absence. All power MOSFETs have an intrinsic rectifier, or body diode, a junction rectifier whose current rating is the same as that of the transistor. With the drive format provided by the UC1637, the two bottom MOSFETs (N-channel) are "on" during the time when motor current circulates, and as a result, the reversed diode carries only a small portion of the current; most of it flows from source to drain through the channel. In fact, the diode fully conducts only during the 1.5μS when both devices in one bridge leg are off. You can add fast recovery diodes in shunt with the MOSFETs if you find that they are essential. The intrinsic MOSFET diode is not particularly fast, and as your output current requirements increase, the need for fast external diodes will become more and more apparent.

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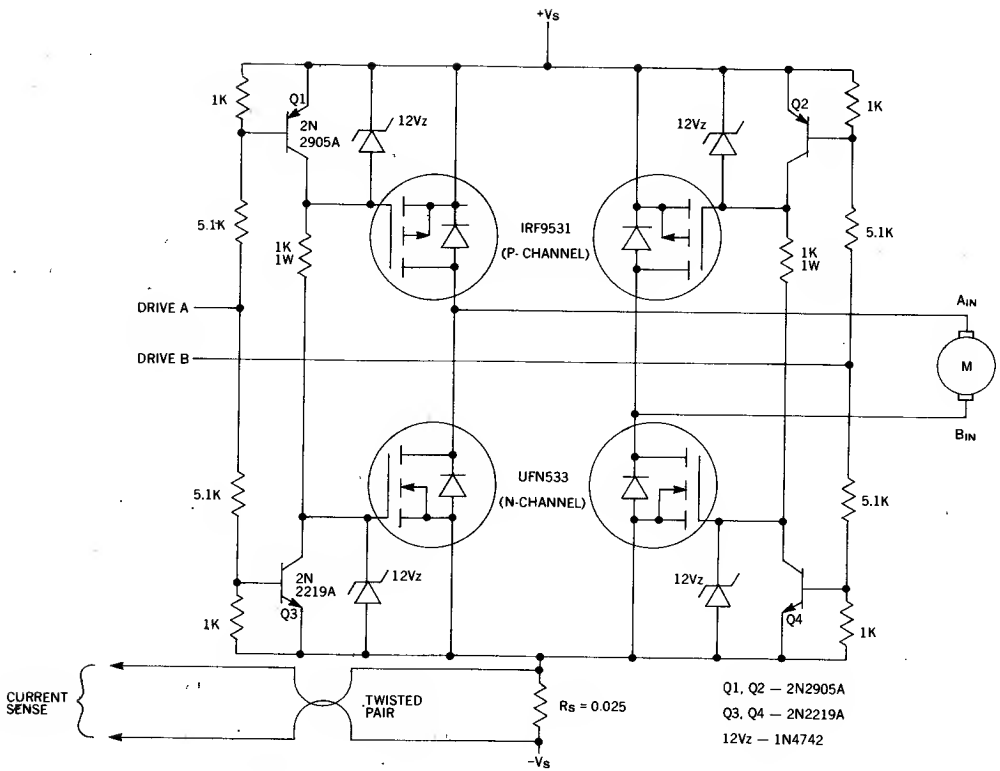

FIGURE 8. THIS 8A POWER AMPLIFIER IS SUITABLE FOR 30KHz OPERATION.

THE SERVOMOTOR

It is convenient to represent the DC servomotor by a simple equivalent circuit, and one such circuit is shown in Figure 9. Note that by expressing the moment of inertia J and the motor constant K in metric units (Nm sec^2 and Nm/A respectively), we avoid the need to include a multiplying constant in the expressions for C_M and e_o. Also, the motor constant K, in metric units, defines both the voltage constant in volt-sec/rad, and the torque constant in Nm/A, as one and the same number.

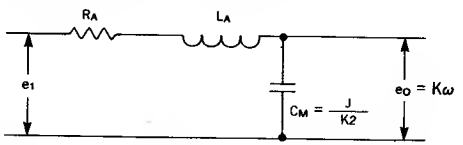

FIGURE 9. EQUIVALENT CIRCUIT OF MOTOR, WHERE J IS THE TOTAL MOMENT OF INERTIA OF ROTOR PLUS LOAD.

R_A = ermature resistance; ohms.
L_A = ermature inductence; henrys.
C_M = equivalant capacitenca; farads.
J = total momant of inartia; Nm sac^2.
K = motor constant; volt sac/rad, or Nm/A.
ω = rotor engular valocity; rad/sec.

TO CONVERT FROM	TO	MULTIPLY BY
oz in sec^2	Nm sec^2	7.06×10^{-3}
volts/KRPM	volt sec/rad	9.55×10^{-3}

The ratio J/K^2 has the dimensions of capacitance, with a value runnng to several thousand microfarads. The voltage across this capacitor is equal to $K\omega$ where ω is the angular velocity of the rotor in rad/sec. Consequently, this voltage is the analog of shaft velocity.

Our equivalent circuit, then, is a simple series connection of R_A, the armature resistance; L_A, the armature inductance; and C_M, the equivalent capacitance, equal to J/K^2. It should come as no surprise that such a circuit will have a natural resonant frequency ω_N, and a resonant Q as well. This is indeed the case, and we have for its transfer function,

$$\frac{e_{o(s)}}{e_{i(s)}} = \frac{1}{(s/\omega_N)^2 + s/Q\omega_N + 1} \quad (12)$$

where $$\omega_N = \frac{K}{\sqrt{L_A J}} \quad (13)$$

and $$Q = \frac{K}{R_A}\sqrt{\frac{L_A}{J}} \quad (14)$$

We can now use these sample results in our sample design. Here are some of the data given by a motor manufacturer:

EG & G TORQUE SYSTEMS
MODEL NO. MT-2605-102CE
(motor - tach assembly)

MOTOR: K_T = 4.7 oz in/amp
K_V = 3.5V/KRPM
R_A = 0.7 ohms
J_M = 0.0018 oz in sec^2
T_M = 8.6 ms (mech. time const.)
T_e = 1.6 ms (el. time const.)
TACH: J_T = 0.001 oz in sec^2
K_V = 3V/KRPM

The several motors in this series and size have the same electrical time constant T_E, and since we know R_A,

$L_A = T_E R_A = 0.016 \times 0.7$
L_A = 1.12 mH

The total moment of inertia is

$J = J_M + J_T = 0.0018 + 0.001$
J = 0.0028 oz in sec^2

In metric units,

$$J = \frac{0.0028}{141.612} \text{ (Nm sec}^2\text{)}$$

Putting K_T in metric units,

$$K = \frac{4.7}{141.612} \text{ (Nm/amp)}$$

The equivalent capacitance is

$$C_M = \frac{J}{K^2} = \frac{141.612 \times 0.0028}{(4.7)^2} = 18{,}000\mu f$$

For the equivalent circuit, then, the values are

R_A = 0.7 ohms
L_A = 1.12 mH
C_M = 18,000μf

The angular velocity will be proportional to the voltage e_o across C_M;

$$\omega = \frac{e_o}{K}$$

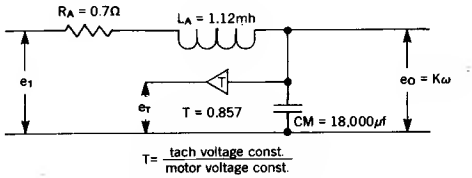

FIGURE 10. THE TACH VOLTAGE e_T IS PROPORTIONAL TO ω.

If the motor has a tachometer attached, we can include it in the equivalent circuit by deriving an equivalent tach voltage proportional to e_o. This is illustrated in Figure 10, where

$$T = \frac{\text{Tach. voltage constant}}{\text{Motor voltage constant}}$$

$$T = \frac{3\text{V/KRPM}}{3.5\text{V/KRPM}} = .857$$

From Eq. 13, ω_N = 222.7 rad/sec

From Eq. 14, Q = 0.356

(Note: Since $\zeta = \frac{1}{2Q}$, the damping factor here is 1.4)

From Eq. 12 and the above data, we can write the ratio of tach voltage to input as

$$\frac{e_T(s)}{e_i(s)} = \frac{.857}{\left(\frac{s}{222.7}\right)^2 + \frac{s}{79.3} + 1} \qquad (15)$$

THE VELOCITY LOOP

Our objective is to put together a feedback loop using our UC1637, H-bridge, and motor: the controlled variable is ω, the motor shaft's angular velocity. For high accuracy, we need a high loop gain, so that small velocity errors are magnified and corrected. The UC1637 internal ERROR amplifier is appropriate for this purpose, and will be used as a summing amplifier. But before proceeding, let us take a look at Figure 11, where a plot of the motor-tach transfer function (Eq. 17) is shown. The plot shows that as the frequency increases, the tach output decreases and the phase lag increases towards a maximum of 180°. This means that although we can introduce plenty of gain at very low frequencies, where the phase lag is low, the added gain must be reduced at the higher frequencies, where the 180° phase lag tends to make our loop a regenerative one. If we want the closed loop response to be "snappy", that is, if we want a bandwidth of several tens of hertz, then the loop gain must be

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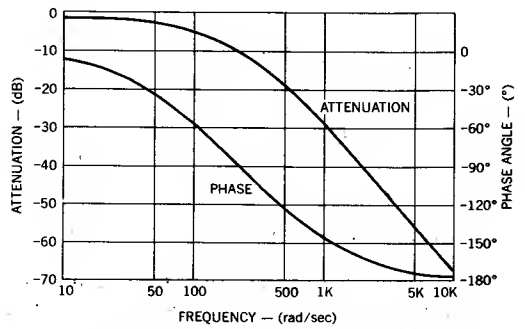
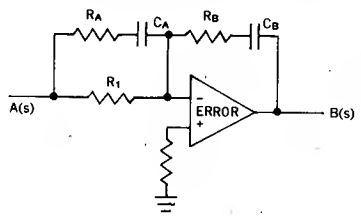


FIGURE 11. PLOT OF MAGNITUDE AND ANGLE OF EQ. 15, WHICH DESCRIBES PERFORMANCE DF OUR TEST MOTOR.

fairly high at all frequencies in the band; yet, for flat response and fast step response with no overshoot we must make certain that the overall phase shift is less than 180° at any frequency at which the gain is greater than unity.



$$\frac{A(s)}{B(s)} = \frac{(1 + sR_BC_B)\,[1 + s(R_1 + R_A)\,C_A]}{sR_1C_B\,(1 + sR_AC_A)}$$

FIGURE 12. ERROR AMPLIFIER WITH ITS FREQUENCY COMPENSATION NETWORK.
THE MAGNITUDE AND ARGUMENT OF THE TRANSFER FUNCTION CAN BE EASILY PLOTTED WITH THE AID OF A PROGRAMMABLE CALCULATOR.

The high gain ERROR amplifier of the UC1637, together with a few external components, is shown in Figure 12. Without R_A and C_A, the phase response of the circuit would go from −90° at low frequencies to 0° at high frequencies. This amount of phase correction is inadequate if we want a tight loop with good transient response. With R_A and C_A shunting R_1, it becomes possible to have a leading phase angle somewhere at midrange, even though the high frequency asymptote is still at zero degrees (R_A and C_A introduce both a zero and a pole). The transfer function of the circuit shown in Figure 12 is plotted in Figure 13 for the following component values:

R_1 = 9.1K
R_A = 1K
C_A = .22μf
R_B = 470K
C_B = .0047μf

The break frequencies are:

$$\frac{1}{R_BC_B} = \frac{1}{(R_1 + R_A)\,C_A} = 450 \text{ rad/sec}$$

$$\frac{1}{R_1C_B} = 23{,}400 \text{ rad/sec}$$

$$\frac{1}{R_AC_A} = 4{,}500 \text{ rad/sec}$$

The plot shown in Figure 14 shows the result of cascading the compensation amplifier, PWM amplifier, and motor-tach. All gain contributions have been simply added together, and all phase contributions have also been added. The result, shown in Figure 14, shows the open loop frequency response of the complete velocity control system.

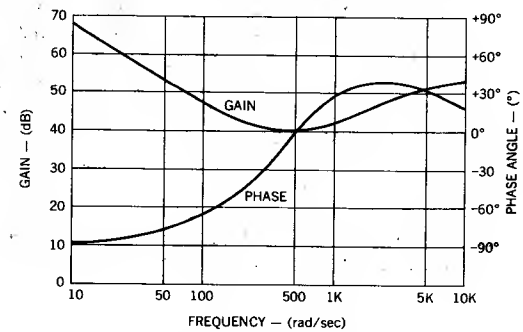


FIGURE 13. MAGNITUDE AND ANGLE DF COMPENSATION AMPLIFIER OF FIGURE 12.

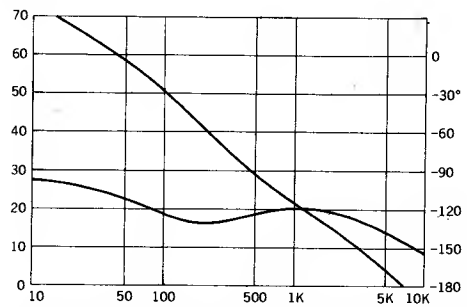


FIGURE 14. OVERALL OPEN-LOOP RESPONSE, INCLUDING +8dB DUE TO PWM AMPLIFIER GAIN AND MOTOR-TACH DC GAIN.

The inclusion of the ERROR amplifier with its compensation components has had the effect of introducing a large amount of gain at the lower frequencies, and also of reducing the phase lag at the higher frequencies. The loop gain is 0dB at about 7KHz, and the phase margin is about 40°. Moreover, since the phase never exceeds 180°, we have the needed indication of *relative stability*, and can proceed to close the loop as shown in Figure 15 and make measurements. Note that a noise filter has been added at the output of the tachometer. Such a filter is usually necessary, especially in PWM control loops of relatively wide bandwidth, because of the inevitable AC coupling between the motor signal and the tach output. In our filter, the 3dB cut-off point is at 21KHz, which is high enough not to affect the loop behavior.

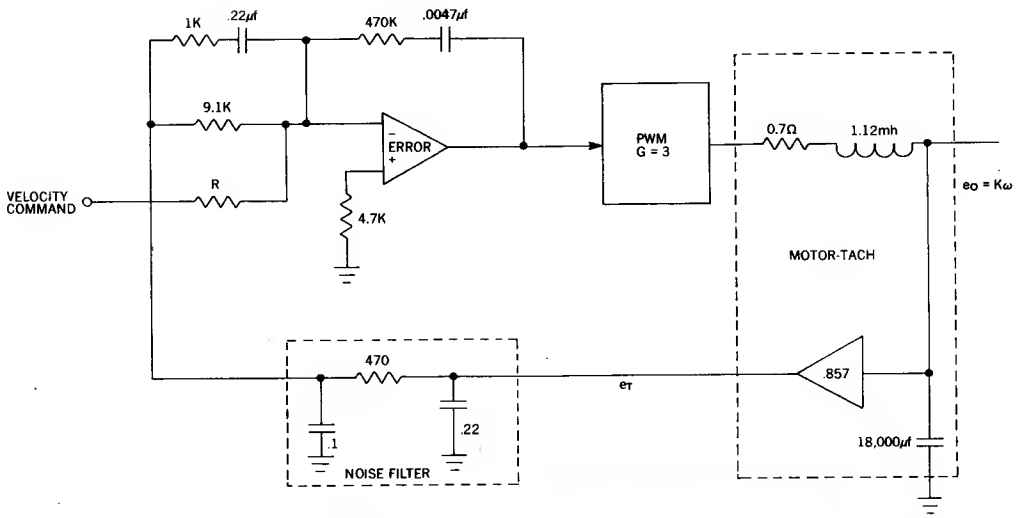


FIGURE 15. THE COMPLETE VELOCITY LOOP.

The oscilloscope trace shown in Figure 16 reveals that the step response of our loop is very well behaved. The motor shaft reaches full speed in less than 10mS, and there is no noticeable overshoot. The net velocity change in Figure 16 amounts to 133 RPM, and the current trace shows that the current does not quite reach the chosen limit of 8A. With larger input steps, the motor accelerates at constant 8A current, and the acceleration rate is approximately 100RPM per millisecond. The 3dB bandwidth of the loop measured about 80Hz.

Top trace: 5A/cm
Bottom trace: 100mV/cm
Horizontal: 5 msec/cm

FIGURE 16. STEP RESPONSE OF THE VELOCITY CONTROL LOOP OF FIGURE 15. THE UPPER TRACE SHOWS THE MOTOR CURRENT; THE LOWER TRACE SHOWS THE TACH OUTPUT VOLTAGE, I.E., MOTOR VELOCITY.

CONCLUSIONS

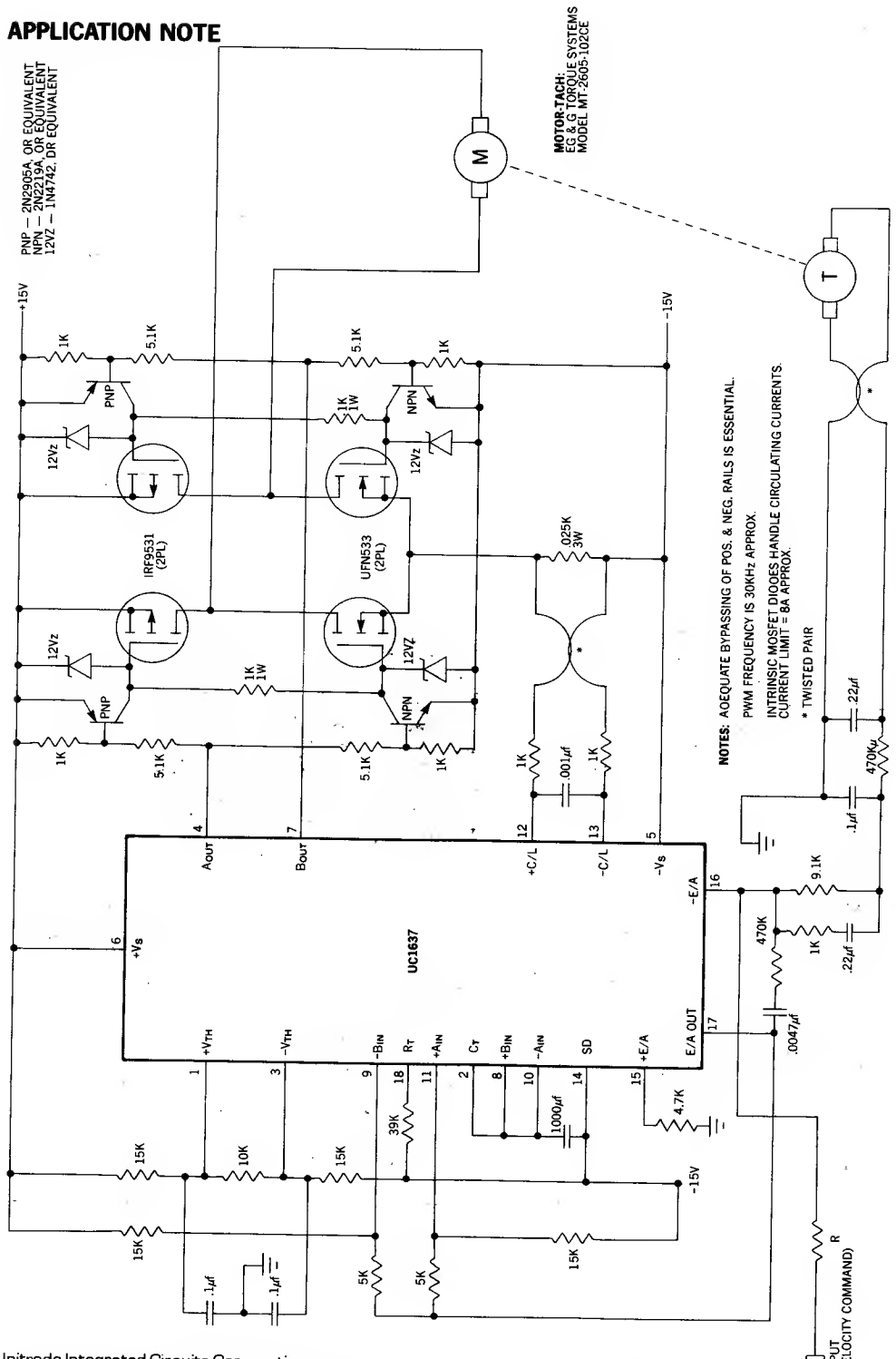
We have discussed in some detail the characteristics of Unitrode's UC1637 and have presented in detail a design approach which illustrates those points. The sample design was built and tested, with the measured results as presented above. These results show that excellent performance can be obtained with few components, and that the design technique is quite simple. Our velocity loop would perform well as an inner loop in a position control system, for example, although a different response might perhaps be desirable. However that may be, using the UC1637 a sizable portion to the job is completed beforehand.

See Figure 17.

ACKNOWLEDGMENTS

We are grateful to EG & G Torque Systems for providing the motor-tachometer used in the sample design.

The Electro-Craft Corporation generously supplied a copy of their engineering handbook on DC Motors, 5th Edition. This book is highly recommended.



NOTES: ADEQUATE BYPASSING OF POS. & NEG. RAILS IS ESSENTIAL.
PWM FREQUENCY IS 30KHz APPROX.
INTRINSIC MOSFET DIODES HANDLE CIRCULATING CURRENTS.
CURRENT LIMIT = 8A APPROX.
* TWISTED PAIR

SELECT VALUE OF R FOR DESIRED GAIN.
WITH R = 9.1K, GAIN WILL BE 333.3 RPM PER VOLT.

FIGURE 17. COMPLETE VELOCITY CONTROL LOOP OF SAMPLE DESIGN.

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IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

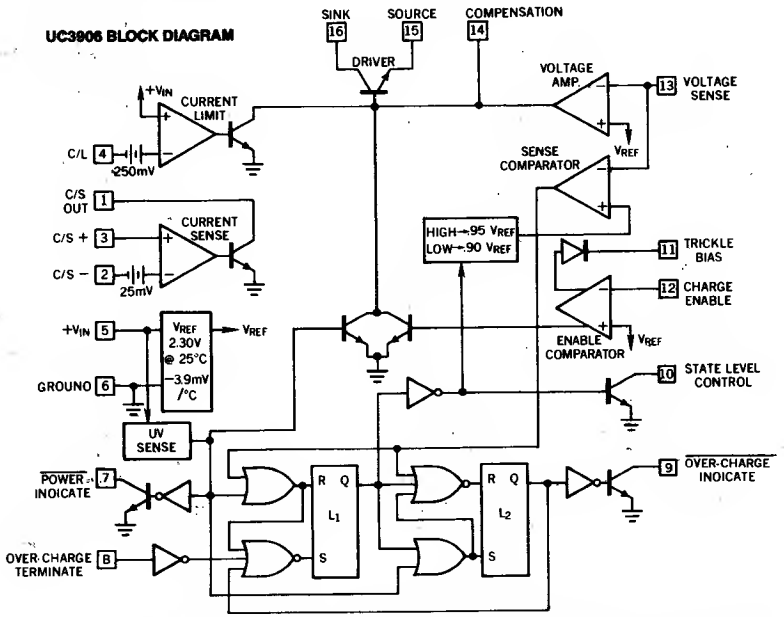


FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger. The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, –40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.

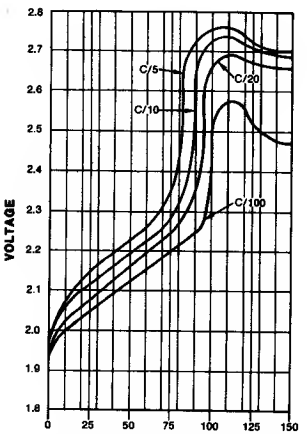


FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products, Inc.)

Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately −4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

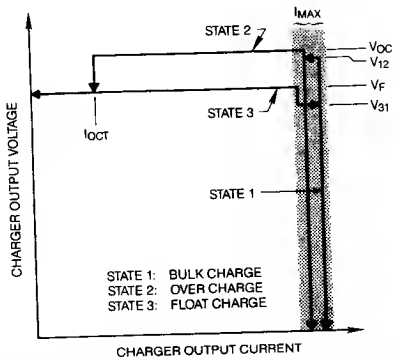


FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger. Internally, the starting of the over-charge state arms the set input of the first latch — assuming no reset signal is present — so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, ($25mV/R_S$), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

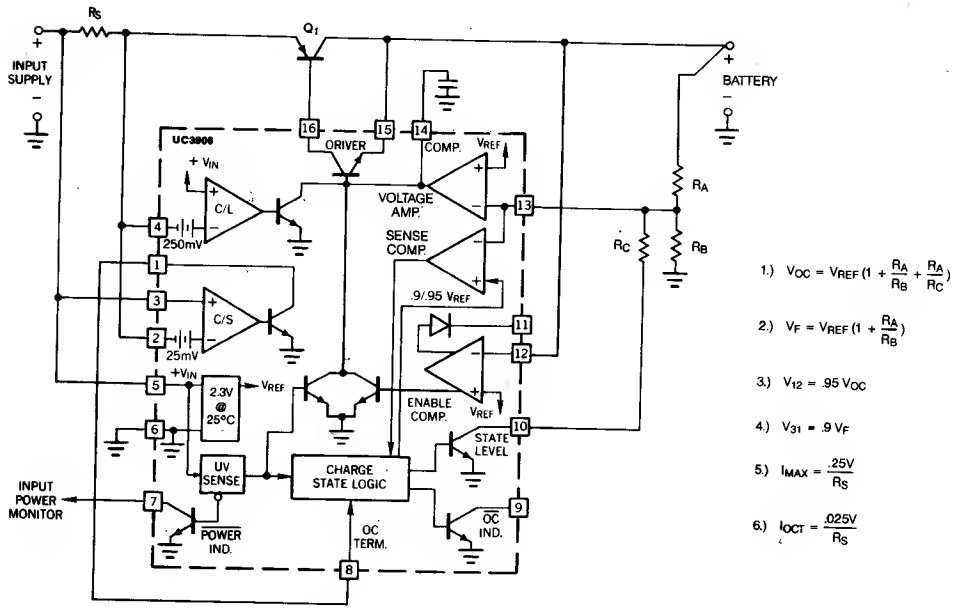


FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

-3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

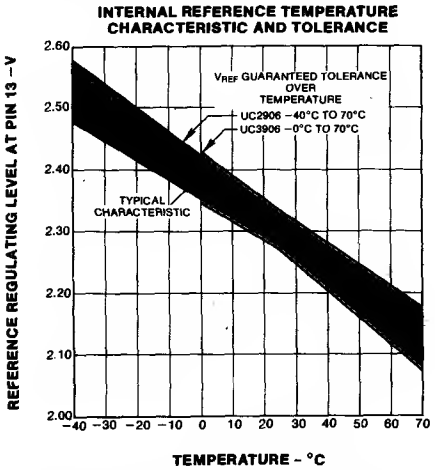


FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C, (-40 to 70°C for the UC2906), to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

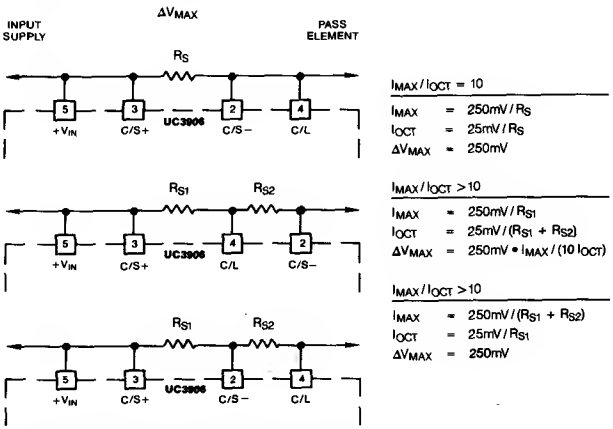


FIGURE 6. Although the ratio of input offset voltages on the current limit end current sense stages is fixed at 10, other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater then 10 is increased voltage drop across the sensing network at I_{MAX}.

9

of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element. As shown in figure 7, the enable comparator input taps off the battery sensing divider. When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-

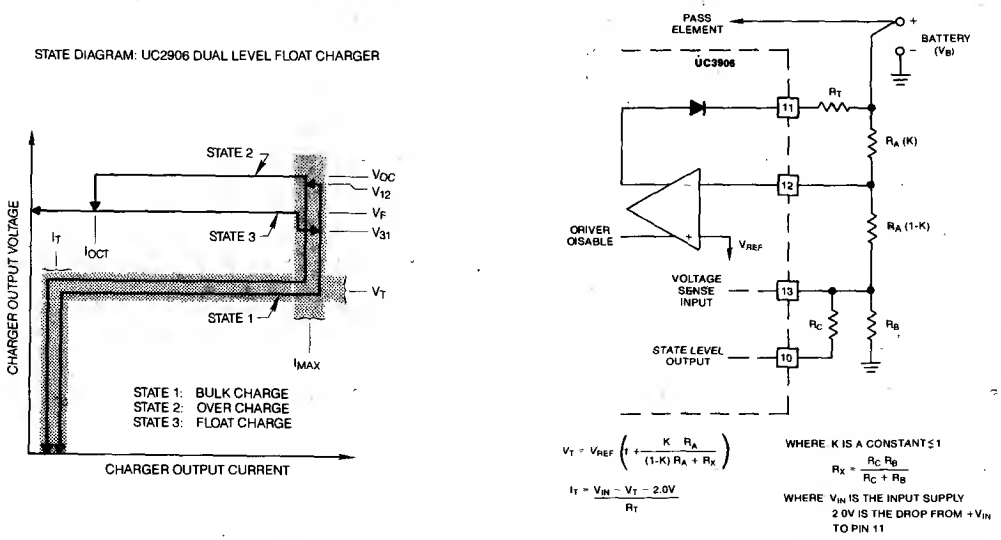


FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor C1 supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

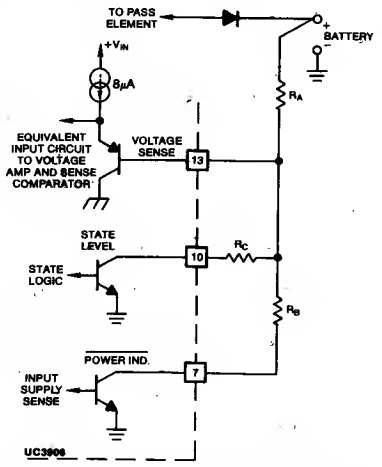


FIGURE 8. By using a diode in series with the pass element, end referencing the divider string to the power indicate pin, pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, I_H, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

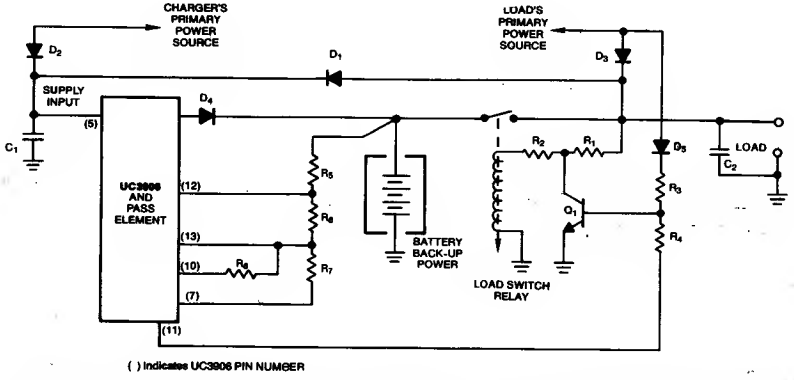


FIGURE 9. Using the enable comparetor to monitor the battery voltege e precise discharge cut-off voltege can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (>25mA), then an external buffering element may be required at the output of the current sense comparator.

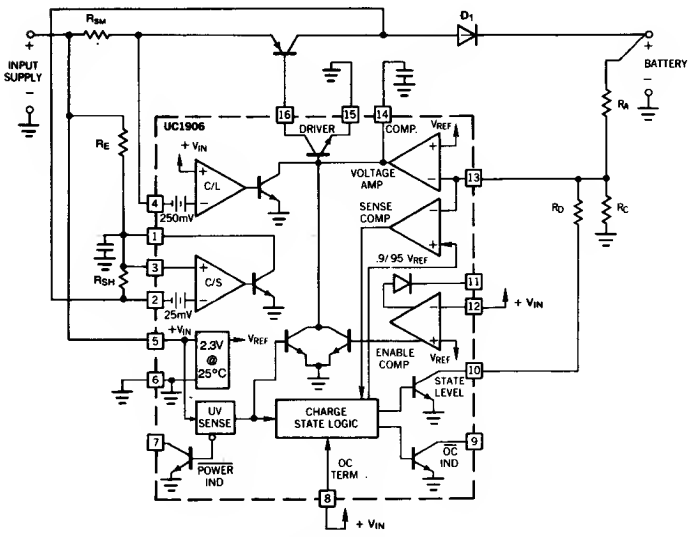
The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

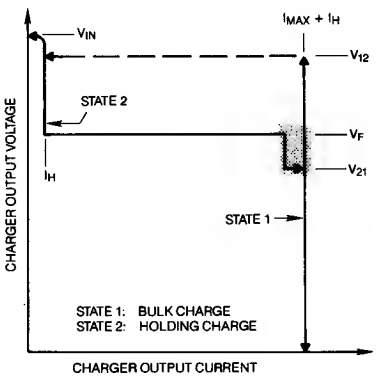
PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.





1.) $V_{12} = .95\ V_{REF}\left(1 + \frac{R_A}{R_C} + \frac{R_A}{R_D}\right)$

2.) $V_F = V_{REF}\left(1 + \frac{R_A}{R_C}\right)$

3.) $V_{21} = .9\ V_F$

4.) $I_{MAX} = \frac{.25V}{R_{SM}}$

5.) $I_H = \frac{.025V}{R_{SH}}$

FIGURE 10. A duel step current charger hes some advantages when large series strings must be charged. This type of charger maintains constant current during normel cherging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to

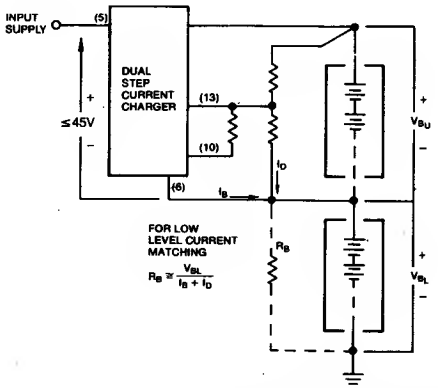


FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bias end divider currents.

the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
TOPOLOGY	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER
CURRENT RANGE	25mA <I <1000mA	25mA <I <1000mA	600mA <I <15A	25mA <I <1000mA
MINIMUM ΔV	ΔV >0.5V	ΔV >2.0V	ΔV >1.2V	ΔV >2.7V
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\beta_{Q2}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \cdot \beta_{Q1\,MIN}\,\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. = IMPEDANCE AT CHARGER OUTPUT.

FIGURE 12. There are a large number of possible driver/pass element configurations, e few are summarized here. The trade-offs are between current gain, input to output differential, and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by edding a resistor in series with the UC3906 driver.

(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by -3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage . . . . . 9.0V to 13V
Operating temperature range . . . . . 0°C to 70°C
Start-up trickle current (I_T) . . . . . 10mA (V_{IN} = 10V)
Start-up voltage (V_T) 5.1V
Bulk charge rate (I_{MAX}) 500mA (C/5)
Bulk to OC transition voltage (V_{12}) . . 7.125V
OC voltage (V_{OC}) 7.5V
OC terminate current (I_{OCT}) 50mA (C/50)
Float voltage (V_F) 7.0V
Float to Bulk transition voltage (V_{31}) 6.3V
Temperature coefficient on voltage levels . . . . . -12mV/°C
Reverse current at charger output with the input supply at 0.0V . . . . $\leq 5\mu A$

In order to achieve the low input to output differential, (1.5V), the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

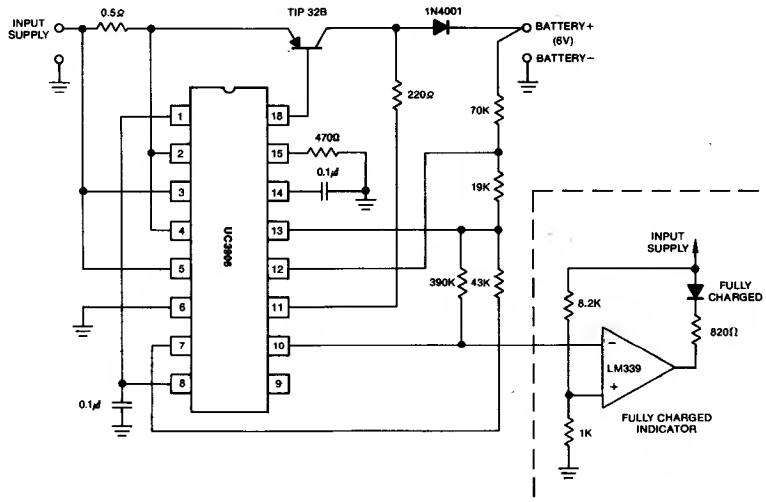


FIGURE 13. This dual level float chargar was designed for a 6V (threa 2V cells) 2.5AH battary. A separate "fully charged" indicator was added for visual indication of charge completion.

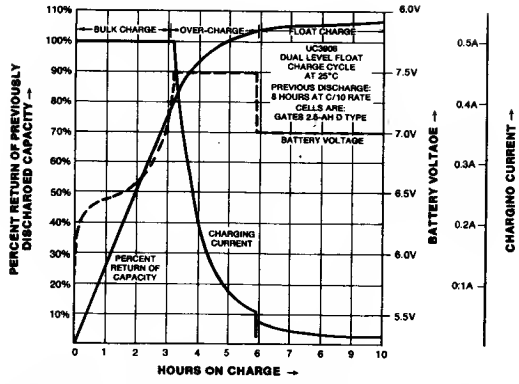


FIGURE 14. The neerly ideal characteristics of the dual level float charger are illustreted in these curves. The over-cherge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

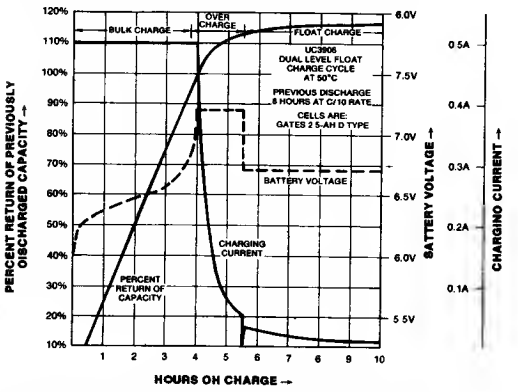


FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge ecceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

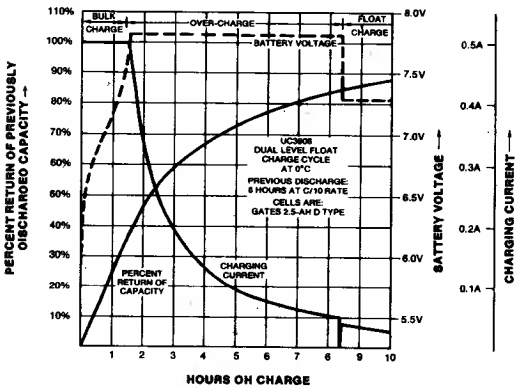


FIGURE 16. At lower temperatures the cepacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

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UC3620
BRUSHLESS DC MOTORS GET A CONTROLLER IC THAT REPLACES COMPLEX CIRCUITS

A COMMUTATOR AND DRIVER CHIP, COMPLETE WITH THERMAL AND UNDER-VOLTAGE PROTECTION AND TRANSIENT SUPPRESSION, RADICALLY SIMPLIFIES THE CONTROL OF BRUSHLESS DC MOTORS

INTRODUCTION

The popularity of the three-phase, brushless DC motor is on the rise for a number of good reasons: There are no brushes to wear out or to arc over; heat dissipation is better because the windings are on the stator, and good torque control is both possible and relatively easy to achieve with the availability of electronic circuits. The motor's main drawback has been the need to design and assemble a complex circuit consisting of six output power transistors with transient suppression diodes, a switching current control circuit, and a Hall logic decoder, plus loop control and protection circuitry.

The advent of the UC3620 controller chip greatly simplifies the designer's problem, for it integrates all these elements. This chip easily and safely controls motors requiring up to 2A of continuous current, and has a peak rating of 3A. The device has a maximum V_{CC} rating of 40V and is available in a 15-pin package rated at 25W. Only a half dozen external components are needed to get a motor running.

A three-phase brushless DC motor has two, four, or more permanent magnet poles mounted on its rotor. The required rotating field is produced by the stator's stationary windings, whose three phases must be commutated in the proper sequence. This sequence is governed by the rotor's angular position, and consequently, some means must be provided both to sense this position and to use that information to control the commutation sequence.

The sensing is accomplished by three Hall-effect devices mounted on the stator close to the rotor magnets, at the correct rotational angles. An electronic circuit decodes the Hall device signals and controls the direction of the currents applied to the three motor phases. This power switching is done by power transistors.

Another function must be added to the driving electronics, namely, that of controlling the motor current and maintaining it at the correct value. At high speed, the electric motor's back emf limits the phase currents. But at low speeds, the back emf is low (it is zero at stall), and therefore if the current is to be kept constant, the applied voltage must be reduced. This is done by sensing the motor current and using its value to regulate the duty cycle of the applied voltage, thereby controlling the average motor voltage. In this way, a constant-current source of motor power is obtained.

HOW IT WORKS

In the controller chip, each of the three output stages is a totem-pole pair (Figure 1) capable of sourcing and sinking the motor's full rated current. Inductive transients from the load are clamped to V_{CC} by Schottky diodes and to ground by the intrinsic substrate diodes, thus obviating the need for external clamping devices.

The power output stages have two functions. The first is to commutate the three motor phases in the proper sequence, producing unidirectional torque in the rotor. The second is to switch the applied motor voltage in the manner selected and programmed by the user, maintaining the output current at the desired level. This switching control of current is accomplished in a fixed-off-time, two-quadrant mode, providing the automatic peak current limiting and low ripple current essential to high electrical efficiency at the motor windings.

The emitters of the three bottom transistors of the totem-pole output stages are connected to Pin 1, through which all the motor current flows. If a low-value resistor is placed between this pin and ground, a usable voltage proportional to motor current is derived without appreciable I^2R losses.

This current-sensing voltage serves as a feedback signal for the switching current control loop. It is applied to the I_{SENSE} input through an RC filter, which prevents false triggering due to noise spikes in the current waveform.

An internal voltage comparator determines whether the voltage $V_{I\ SENSE}$ is equal to V_{REF}, a positive variable reference voltage dependent on the output of the chip's error amplifier. If Q of the monostable multivibrator (that follows the comparator) is high, the chip's output stages are enabled, the output current increases, and $V_{I\ SENSE}$ also increases until it becomes positive with respect to V_{REF}.

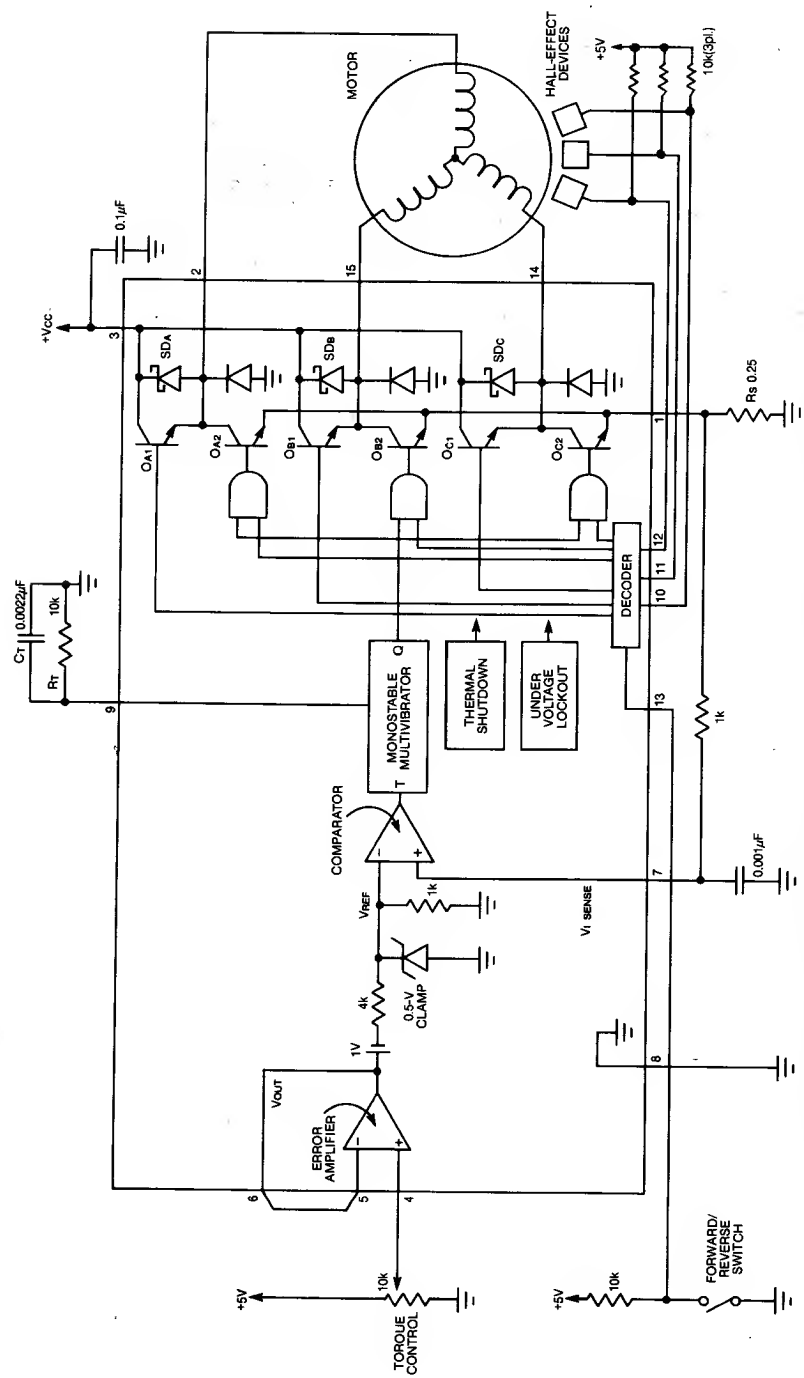

FIGURE 1. THE UC3620 CHIP PROVIDES FULL CONTROL OF MOTOR CURRENTS UP TO 2A, WITH ROTATION IN BOTH DIRECTIONS. HALL-EFFECT DEVICES INTERNAL TO THE MOTOR PROVIDE POSITION INFORMATION THROUGH A DECODER TO THREE TOTEM-POLE DRIVERS. COMPARING THE CHANGING VOLTAGE ACROSS R_S WITH THE ERROR AMPLIFIER OUTPUT HELPS KEEP THE CURRENT CONSTANT.

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At this point the comparator resets the monostable, forcing Q low and disabling the output stages. The motor current now circulates through one of the Schottky diodes and the conducting upper transistor because of the stored inductive energy, until the monostable off-time has elapsed (Figure 2). Q then returns to the high state and the cycle is repeated.

The switching off-time is fixed, since it is determined by the user's choice of timing components R_T and C_T. At the start of the off-time, capacitor C_T is charged to +5V, and the monostable outputs are held in the off state until this voltage decays exponentially to a level of 2V. Since resistor R_T supplies the only path for the discharging current, it is possible to calculate the time required, t_{OFF}, in seconds:

$$\exp\left(\frac{-t_{OFF}}{R_TC_T}\right) = \frac{2}{5}$$

or:

$$\frac{-t_{OFF}}{R_TC_T} = \ln(2/5) = -0.916$$

$$t_{OFF} = 0.916R_TC_T$$

When the 2 volt level is reached, the monostable is set again, and the cycle repeats.

The reference voltage, V_{REF}, then, is the controlling voltage of what is in effect a transconductance amplifier of which the controlled output is the motor current through resistor R_S. To repeat, the circuit controls the peak value of the current. If the switching frequency is high (low current ripple), the assumption may be made that the average value of motor current, I_M, is approximately equal to the peak, and so:

$$V_{REF} = I_MR_S$$

$$G_T = \frac{I_M}{V_{REF}} = \frac{1}{R_S} \text{ Siemens}$$

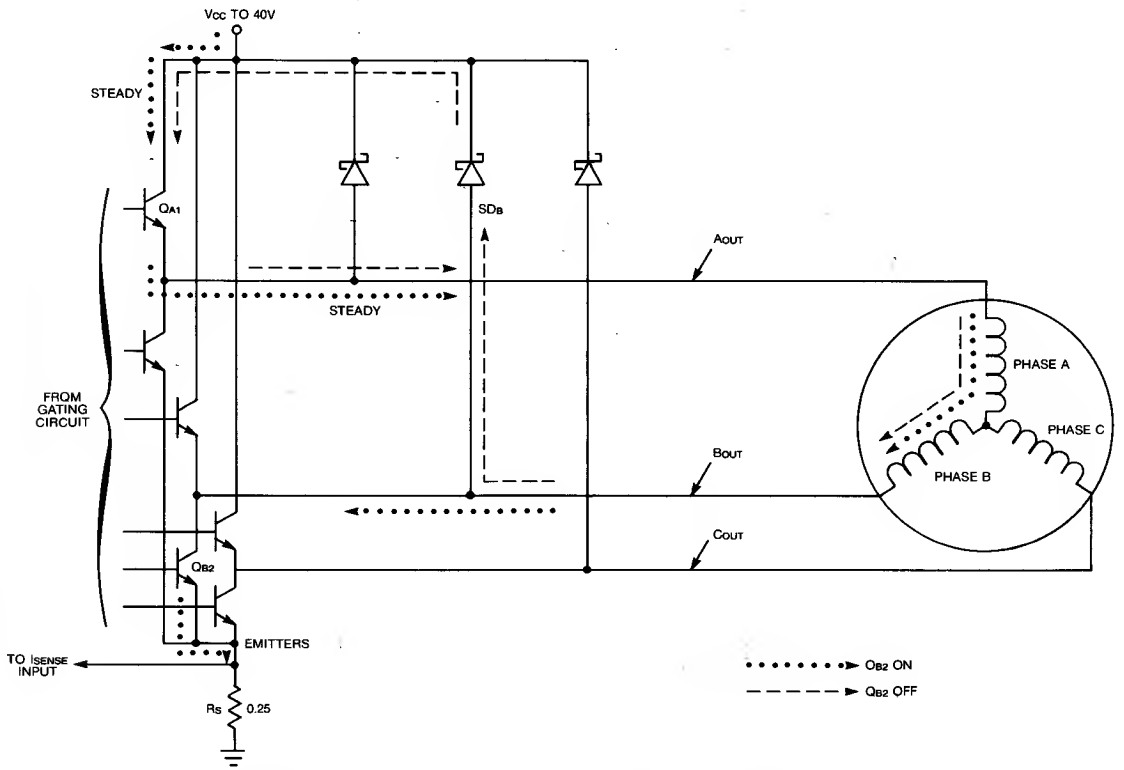

FIGURE 2. WHEN Q_{B2} IS ON, CURRENT FLOWS THROUGH Q_{A1} AND TWO MOTOR WINDINGS TO GROUND (DOTTED ARROWS). DURING THE TIME THAT Q_{B2} IS OFF, THE STORED ENERGY IN THE WINDING INDUCTANCE FLOWS THROUGH SCHOTTKY DIODE SO_B, TRANSISTOR Q_{A1}, AND BACK THROUGH THE WINDINGS (DASHED ARROWS).

The maximum value of V_{REF} is limited to 0.5V by a zener diode (Figure 1 again). This value sets a limit to the maximum motor current as well, since:

$$I_{MAX} = \frac{0.5}{R_S} \text{ amperes}$$

Consequently, the proper selection of R_S protects both the motor and the chip from excess current.

The motor is connected to the chip's three outputs A_{OUT}, B_{OUT}, and C_{OUT}. The motor windings are Y-connected, and the driver energizes two phases at a time, the third one being off. Thus each driver output will be in one of three states: high (V_{CC}), off (high impedance), or low (0V), generating six possible combinations (Table 1).

Table 1. Terminal Conditions for Different Driver Output States

OUTPUT STATE	TERMINAL A	TERMINAL B	TERMINAL C
$A\bar{B}Z$	High	Low	High Z
$AZ\bar{C}$	High	High Z	Low
$ZB\bar{C}$	High Z	High	Low
$\bar{A}BZ$	Low	High	High Z
$\bar{A}ZC$	Low	High Z	High
$Z\bar{B}C$	High Z	Low	High

SIX STATES

In each of the six possible states, one of the upper transistors is on, together with one of the bottom transistors. In any of the states, it is the bottom transistor that controls switching, while the upper device remains conducting. For example, in state $A\bar{B}Z$, current flows continually through upper transistor Q_{A1}, but switches between lower transistor Q_{B2} and Schottky diode SD_B (Figure 2 again). This switching action results in low current ripple through the motor and is known as two-quadrant operation, in which the power supply current flows only in one direction, namely, into the driver (Figure 3). One advantage of this unidirectionality is that a shunt regulator is not necessary to prevent an overvoltage at the V_{CC} bus during motor deceleration.

A more significant advantage is that it results in the least current ripple for a given switching rate. More precisely, the current waveform's form factor (the ratio of its rms to its average value) is closer to unity. Since the amount of I^2R heating depends on the rms value of I, whereas torque depends on the average value, a form factor approaching unity results in greater motor efficiency.

The current reference voltage V_{REF} at the inverting input of the chip's comparator depends on the output voltage, V_{OUT}, of the error amplifier. The relationship between the two is:

$$V_{REF} = \frac{V_{OUT} - 1}{5}$$

The offset of 1V between V_{OUT} and the 5:1 voltage divider ensures that the error amplifier can always achieve zero current at the motor. The amplifier itself has a high gain of 80dB minimum, an f_t of 0.8MHz; and is internally compensated for stable operation.

In a feedback speed control application, even with a reduction in gain of 14dB due to the 5:1 resistive attenuator between the amplifier and the comparator, there is still a minimum DC gain of 66dB, which is more than adequate for most requirements. The same consideration applies to the 1V offset, which is overshadowed by the high-gain loop as well.

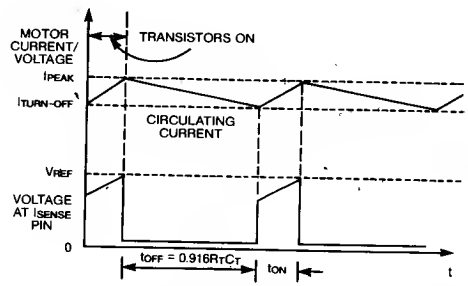

FIGURE 3. THE CHIP'S SWITCHING CIRCUIT CONTROLS MOTOR CURRENT ON A PULSE-BY-PULSE BASIS. WHEN THE BOTTOM TRANSISTOR OF AN OUTPUT STAGE IS ON, THE CURRENT AT FIRST RISES RAPIDLY ANO THEN DECAYS SLOWLY AS IT CIRCULATES THROUGH THE TRANSISTOR'S ASSOCIATED DIODE. THE FORM FACTOR OF THE WAVEFORM IS THEREFORE CLOSE TO UNITY, SO THAT HEATING OF THE COILS IS REDUCED.

The chip also includes two protection circuits to help make it more reliable. The under-voltage lockout prevents the output stages from being energized unless the supply voltage can provide sufficient base current to the drive transistors. The maximum V_{CC} start-up threshold is set at 8V and has a built-in hysteresis of 0.5V.

A thermal shutdown circuit affords protection against excessive junction temperatures. This circuit disables the drive transistors when the chip's temperature is between 150°C and 180°C. When the temperature returns to a safe value, normal operation is automatically restored.

When the power source for a motor is DC, a commutator is needed to, in a sense, alternate the power applied to the windings. A brushless DC motor uses an external power commutator. As a rule, however, the motor has an electronic device internal to it that generates information relative to angular position for use in controlling the commutator.

CONTROLLING BRUSHLESS MOTORS TO 2A

The control chip was designed to drive any three-phase brushless DC motor of up to 2A and is particularly suited for motors with integral Hall-effect devices. H_A, H_B, and H_C (Figure 1 again) are TTL-compatible inputs that, together with the Forward-Reverse input (FWD/REV), determine the output states (Table 2).

The commutation logic built into the UC3620 is intended for use with motors with 120 electrical degree Hall codes. Motors that use the alternative 60 electrical degree code can be easily accomodated with the addition of an inverter to reverse polarity of one of the Hall signals.

When used as described, the device operates in a current feedback mode and acts as a current controller, or rather as a transconductance amplifier. This closed-loop circuit can be made part of another feedback loop to control the motor speed. Controlled speed loops are of interest in many applications, some of which require a very high degree of control accuracy. For example, a crystal-referenced phase-locked loop is needed to control the spindle speed of magnetic disk drives.

Table 2. Hall Device Logic Coding

HALL DEVICE INPUTS			FORWARD/ REVERSE LINE	DRIVER OUTPUT
H_A	H_B	H_C		
1	0	1	1	$A\bar{B}Z$
1	0	0	1	$AZ\bar{C}$
1	1	0	1	$ZB\bar{C}$
0	1	0	1	$\bar{A}BZ$
0	1	1	1	$\bar{A}ZC$
0	0	1	1	$Z\bar{B}C$

Note: A change of state in the Forward/Reverse line inverts the output states, thus reversing the direction.

NEW PULSE WIDTH MODULATOR CHIP CONTROLS 1 MHz SWITCHERS

ABSTRACT

Controversy prevails as to the benefits of pushing switched mode pulse widtb modulated power supplies higher and higher in frequency. Two facts are undisputed tbough: the industry is pushing switching frequencies up daily and no PWM control IC has been available to optimally control circuits running above several bundred kilohertz. A new IC, the UC3825, has been developed with the top end of the PWM frequency spectrum in mind to simplify high speed control problems. This chip, suitable to eitber voltage or current mode control, addresses the speed critical parameters that have been glossed over in the past: error amp bandwidth, output drive capability, oscillator frequency range, and propagation delay. A one megahertz, 50 watt supply bas been built to demonstrate the chip.

PWM CONTROLLER REVIEW

Briefly reviewing popular control IC's on the market today should serve to illustrate one source of the headaches belonging to designers of high frequency switching power supplies. The snaggle-toothed appearance of the table illustrates the fact that high speed parameters have generally been ignored. The entries in this table represent the tried and true first and second generation standbys (1524, 1525, 494), dedicated off line control (1840), and current mode (1846). All these architectural approaches have certainly proven sufficient for numerous converter designs, but all lack the processing speed required to keep track of a 1 MHz switcber, or even 200 kHz for that matter. Many specifications in the table are missing completely, some are only typical, and the few guaranteed limits leave much room for improvement.

Of prime importance here is the delay time between fault detection and turning off the power switch – the speed critical path. When a fault occurs, either the on chip over-current sense section or an off chip fault detector plus the shutdown section of the cbip must work fast enougb to turn off the power switch before destructive current levels introduce an automatic (and permanent) power down feature to the supply. This feature, of course, is manifested in blown power devices. The problem is aggravated at tbe onset of core saturation, since switch currents then rise at much faster rates.

Also important is the drive capability of the output stage of the control chip chosen. Rise and fall times must be consistent with switching speeds or else an output buffer will have to be added. This, of course, adds delay to the speed critical path placing tighter demands on the delays through the chip or forcing the designer to over-specify the power elements to insure fault survival. Over-specifying, however, adds cost, weight and volume as transistors, heat-sinks, and transformers are beefed-up. These consequences are in direct opposition to tbe very motives for going to higher frequencies in the first place – reduced volume and lower cost.

On-chip error amplifiers have also been a design obstacle in the past. Why build a high frequency switcher and then over compensate tbe loop due to lack of error amp bandwidth? Designers bave been forced to conser-

SPEED COMPARISON OF PWM CONTROLLER IC'S

	SHUT DOWN DELAY (ns)		OVER-CURRENT SENSE DELAY (ns)		ERROR AMP BANDWIDTH (MHz)		ERROR AMP SLEW RATE (V/ s)		OUTPUT RISE/FALL TIME (ns)	
	TYP	MAX	TYP	MAX	TYP	MIN	TYP	MIN	TYP	MAX
SG3524	–	–	–	–	3	–	–	–	200	–
UC3524A	200	–	600	–	3	–	–	–	200	–
UC3525A	200	500	–	–	2	1	–	–	100	600
TL494	–	–	–	–	0.8	–	–	–	200	400
UC3840	–	–	200	400	2	1	0.8	–	–	–
UC3846	300	600	200	500	1	0.7	–	–	50	300
UC3825	50	80	50	80	5.5	3	12	6	30	60

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vatively use the bandwidth available simply due to a lack of guaranteed specifications in many cases. Also, some characteristics which would prove useful haven't been specified at all. Slew rate is such a specification that has great bearing on the large signal response of the supply.

By comparison, the 3825 specifically addresses the speed critical parameters. Maximum propagation delays of 80 ns nearly belong in the "order of magnitude" improvement catagory. Slicing delays yielded a hefty output stage capable of 1.5 Amp peak currents. The guaranteed rise time is, in fact, more a function of internal slew rates than external loading in the 1000 pF range. The error amp guaranteed to 3 MHz and 6 V/μs promises ease of use when controlling wide-band loops.

UC3825 BLOCK DIAGRAM

The design philosophy for the 3825 was to build a chip faster than any other available and tailor it to fit neatly into high frequency converter designs. It includes a dual totem-pole output stage capable of driving most power mosfet gates stand-alone, and the versatility to be useful for DC to DC, off-line, bridge, flyback, push-pull, and even resonant mode converter topologies. The member of a family covering the conventional temperature ranges, the UC3825 is specified for zero to 70 degrees centigrade while the UC2825 spans −25 to 85, and the UC1825, −55 to 125.

The block diagram of the 3825 (figure 1) is architecturally similar in many respects to a number of previous PWM controllers. It includes an oscillator, under-voltage-lock-out circuit, trimmed bandgap voltage reference, wideband error amplifier, PWM comparator PWM latch, toggle flip-flop, soft start section, comparators for over-current sensing and reinitializing soft start, and dual totem-pole outputs. The input to the PWM comparator is brougbt out to a separate pin so that it can be connected either to the timing capacitor for conventional PWM designs or a current sensing network for current mode control schemes.

In normal operation, the oscillator establishes a fixed clock frequency issuing blanking pulses to terminate one period and begin the next. These pulses serve to reset the PWM comparator while blanking the outputs off. After the blanking pulse, one output turns on until the ramp input (level shifted 1.25 Volts) exceeds the error amp output voltage. This sets the PWM latch which turns the output off and triggers the toggle flip-flop, selecting the other output for the next period.

THE SPEED CRITICAL PATH

The blocks that set the 3825 aside as the controller best suited for frequencies over several hundred kilohertz are those in the speed critical path (high-lighted blocks in figure 1.): the PWM comparator and current limit comparator in the front end; the PWM latch and associated internal logic; and the ouput stage. Signal

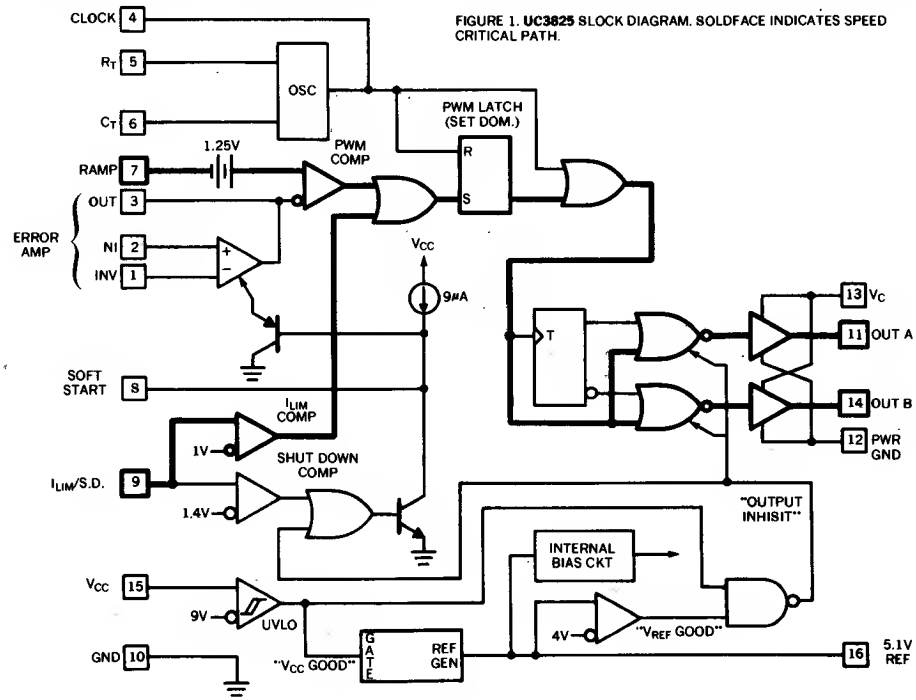


FIGURE 1. UC3825 SLOCK DIAGRAM. SOLDFACE INDICATES SPEED CRITICAL PATH.

propagation through these subcircuits makes or breaks a design during a fault condition. In the 3825, the propagation delay from either the Ramp input or the Current-limit sense input to the output pins is typically 50ns, very much faster than any chip available today.

Comparators

The PWM comparator is basically an npn differential pair with an emitter follower output (figure 2a). The pair is biased so that the output swing is one Vbe. This guarantees none of the transistors in the comparator will saturate while providing output voltage levels compatible witb the internal logic. In order to assure that the input common mode range of the comparator is not exceeded (the range of an npn input pair cannot go below approximately one Volt), a 1.25 Volt level shift is included between the non-inverting input of the comparator and the input pin of the chip. This allows the ramp input to swing from zero to approximately three Volts. The inverting input is tied directly to the output of the error amplifier.

The benefit of this approach is ease of use both in current mode and conventional PWM applications. For the older PWM circuit approach, the ramp input pin can be tied directly to the oscillator Ct pin while current mode users can simply tie a ground referenced current sense network directly to the Ramp pin.

The current limit comparator is very similar in design to the PWM comparator. Its inverting input is referenced internally to a one Volt level derived from the 5.1 Volt reference allowing the non-inverting input to be brought directly to the current limit pin. Functionally, when a fault causes the Current-limit pin to exceed one Volt, it acts just like the PWM comparator, setting the PWM latch and causing the outputs to remain off for the duration of the clock cycle.

The current-limit comparator can also be combined with the 3825 outputs and a few external components to form a constant volt-second product clamp (figure 2b). This clamp is useful in current mode systems to prevent core saturation during load transients. When either output turns on (goes high), capacitor, C, is charged from Vin through resistor, R. Normal circuit operation would turn off the outputs causing C to be discharged before it reaches one Volt. If, however, it does reach one Volt, the current-limit comparator terminates the output pulse. Since tbe charge rate is proportional to Vin (assuming Vin is much greater than one Volt), then a constant Volt-second product clamp of one Volt times RC is achieved.

Logic

All of the speed critical logic, including the PWM latcb, the toggle flip-flop, and various gates are a cross between emitter coupled logic and emitter function logic. In either case, their speed relies on emitter coupled pairs and emitter follower buffers biased to insure that no transistor saturates. Although two OR's, a NOR and the PWM latch are directly in the critical path between the input comparators and the output drivers, they account for only twenty percent of the total delay, the remainder being shared between the comparators and the output stage.

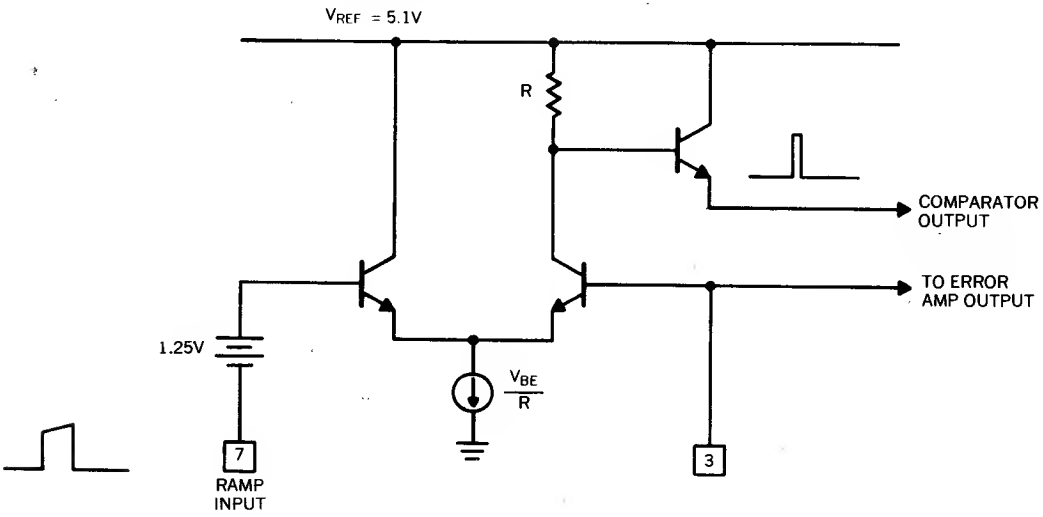


FIGURE 2a. PWM COMPARATOR SCHEMATIC.

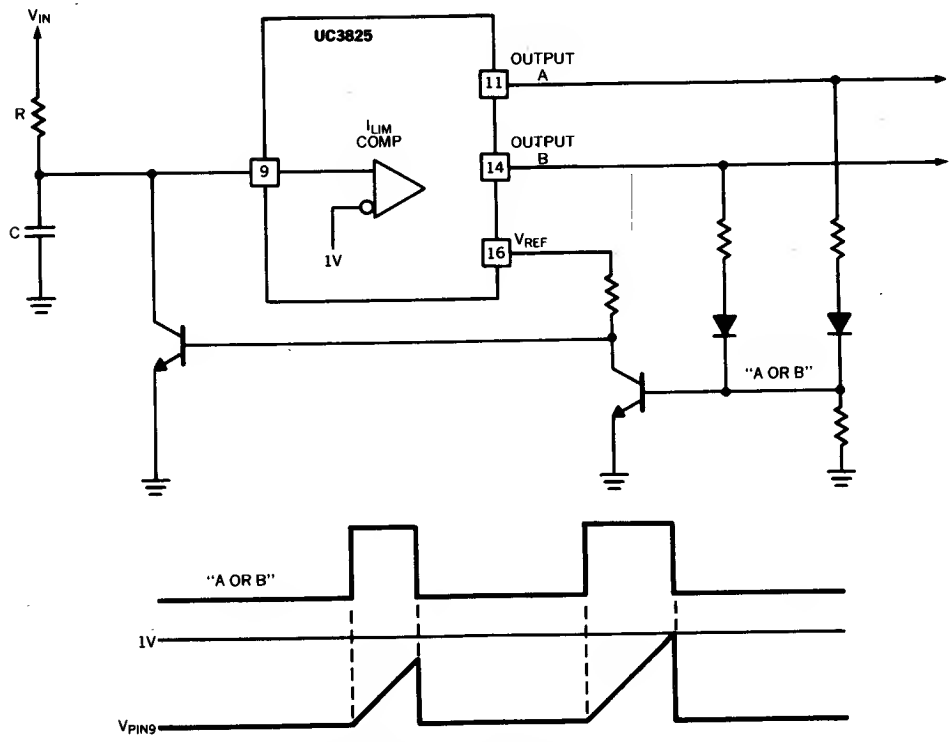


FIGURE 2b. CONSTANT VOLT-SECOND PRODUCT CLAMP IMPLEMENTED USING THE CURRENT LIMIT COMPARATOR.

Outputs

Speed from one pin to another does little or no good unless the signal coming out of the chip has the strength to do its job. The dual totem-pole drivers of the 3825 are capable of driving 1000 picofarads from one rail to the other in a mere 30 nanoseconds. In fact the peak current avilable is in excess of 1.5 Amps. This kind of brute strength is sufficient for driving a wide range of power mosfet's in a variety of applications.

Some older PWM controllers with totem-pole output stages are plagued with hefty amounts of cross conducted charge during output transitions. This can result in major self heating problems especially at higher clock rates. The 3825 output stage (figure 3a) has been modeled after the successful designs of the UC3846 and UC3842. The differences are in bias values and the addition of Schottky diodes. This circuit guarantees the output transistors, Q1 and Q2, are driven with complementary signals to keep cross conducted charge under control. This approach necessarily involves a compromise since speed is of the utmost concern. Delays could be inserted to guarantee zero cross conducted charge, but that would be contrary to the required propagation delays for high speed operation. The outputs have been adjusted to yield these rise and fall times at a penalty of only 20 nanocoulombs of cross conducted charge per transition. At a clock frequency of 500 kHz, this only adds an additional 10 mA to the supply current.

Rather than dwell on cross conducted charge, which is measured with no load on the outputs, it is more appropriate to examine the performance with typical loads. The most anticipated load is a power mosfet. The impedence presented by the gate of the fet is application dependent, but is primarily capacitive. Therefore, consider the requirements of driving a capacitor with a square wave voltage. The charge required for one cycle is equal to the capacitance times the voltage. The average current taken from the supply is that charge times the switching frequency. This determines the power required from the supply to drive the cap. Since the cap is an energy storage element, all the power

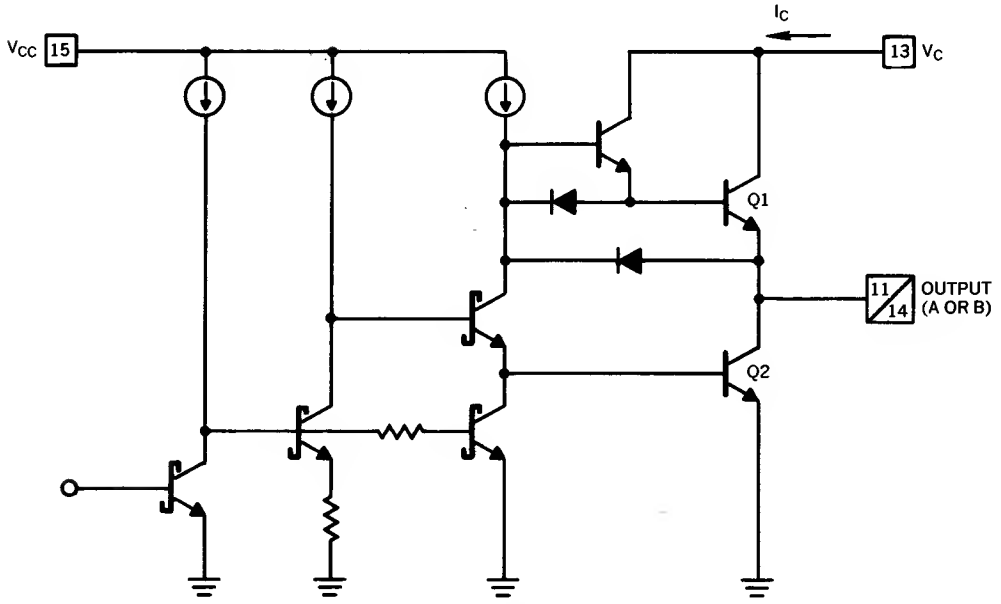
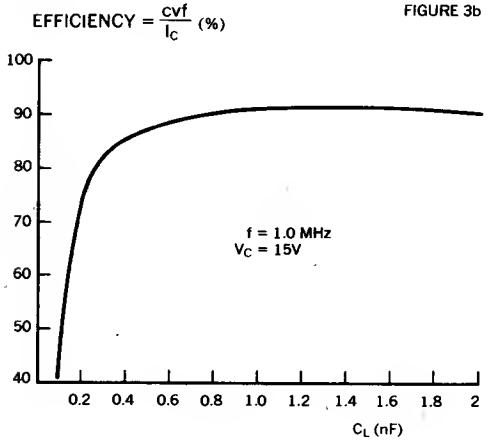


FIGURE 3a. OUTPUT STAGE SIMPLIFIED SCHEMATIC.

taken from the supply is dissipated by the chip. An efficiency figure for the chip can be defined as the ratio of the theoretical power dissipation to the actual power dissipated by the chip. This can be determined for a given frequency and supply voltage by measuring the average supply current into the Vc pin (assuming the peak output voltage is approximately equal to the supply voltage). The figure of efficiency, then, is: (CVf)/Ic. The graph of figure 3b shows the 3825 optimized to drive capacitances above 200pF. Care should always be taken when driving high capacitive loads to make sure the maximum power dissipation level of the chip is not exceeded.

FIGURE 3b



Another side effect of the output stage should be considered. Any node in a circuit capable of driving large capacitances at these rates begins quickly to resemble an LC tank. Transmission lines, even one inch in length, can become troublesome. The trouble occurs when, on the falling edge at an output, the load rings and actually pulls the output pin below ground. For years IC manufacturers have been warning users not to allow certain pins to go below ground and the 3825 output pins carry the same warning. The collector of the pull down transistor becomes a parasitic npn emitter when pulled below the chip's substrate, which is grounded (figure 4). The collector, or collectors as the case is, are every other npn collector and pnp base on the chip. The ones that are closer to the parasitic emitter collect proportionally more current than ones further away. Physical size of the parasitic collectors also plays a similar role. The results of this phenomenon can range from nonobservable to severe. Resembling leakage current internally, reference voltages can be altered, oscillator frequency can jitter, or chip temperature can be elevated. Dummy collectors tied to ground are inserted into the 3825 chip which help to attenuate this problem but the designer still needs to be aware of it. The problem's potential is not a horror story, though. Among the easiest of solutions is some form of damping in the load circuit (for example ten ohms series resistance) and a good high speed diode, Schottky if possible, to clamp the output pin's negative going excursion.

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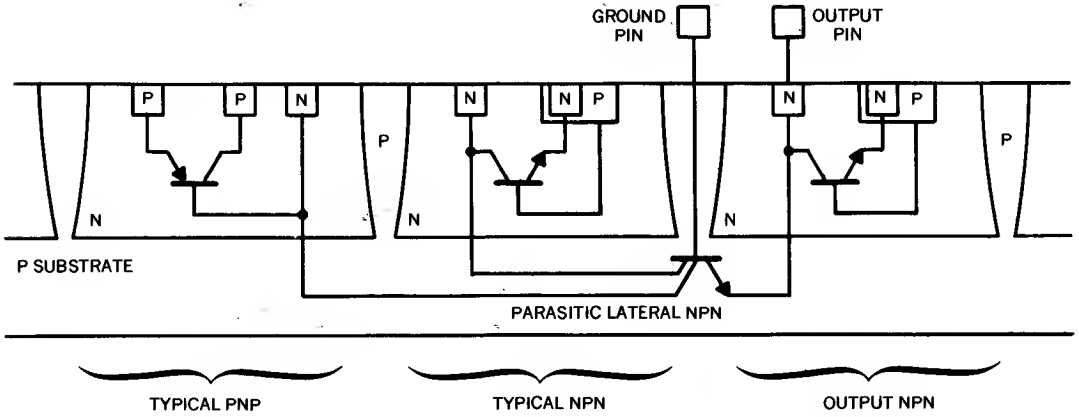

FIGURE 4. PARASITIC NPN TURNS ON WHEN SUBSTRATE – EPI JUNCTION IS FORWARD BIASED.

HIGH SPEED COMPLEMENTARY BLOCKS

An integrated circuit controller with delays of 50ns through its speed critical path is certainly a leading candidate for high frequency switcher applications. There are a few blocks just off the race path that need also to be fast in order to fully qualify the chip for such applications. The oscillator and error amplifier are two such blocks.

Oscillator

From the users point of view, the oscillator looks identical to many that have gone before it (figure 5a). Composed of an all npn comparator, this oscillator has dual thresholds – the upper at 2.8 Volts and the lower at one Volt. Charging current for the timing capacitor, Ct, is mirrored from the timing resistor, Rt. The Rt pin is held at a temperature stable 3 Volts. Temperature stability of the oscillator, then, is achieved by maintaining stable thresholds at the comparator. When Ct has charged to the upper threshold, Q3 turns on to sink a controlled current of approximately 10 mA. The effect of this action is that the discharge of Ct is done in an orderly manner allowing the comparator to reliably catch it when crossing the lower threshold. This also prevents Q3 from saturating, reducing delays in the oscillator and enabling it to operate at higher frequencies. The 3825 oscillator is nominally specified at 400kHz with an initial guaranteed accuracy of 10%. Temperature stability is typically better than 5% while voltage stability (frequency shift over supply voltage) is 0.2%. Oscillator dead time, which effects controller dynamic range, can typically be held to 100ns at 1MHz, allowing 90% duty cycles.

In applications where two 3825's are used in close proximity and synchronization is desired (figure 5b), the oscillator in one chip can be disabled by tying Rt to the reference Voltage. That chip, then, must be clocked by joining the clock pins of both chips. Multiple 3825's also can be synchronized from a master 3825 or other external sync signal. The slave chips are programmed to run at a frequency somewhat lower than the master chip. The master then inserts a sync pulse forcing each slave's Ct over the top threshold and causing discharge action to occur. This way, each chip generates its own clock pulses synchronized to a master clock.

Error Amplifier

The 3825 error amplifier is a voltage gain amp with premium bandwidth and slew rate. Again using only npn's in the signal path, a compensated unity gain bandwidth of 5.5 MHz is achieved. The simplified schematic (figure 6) shows the signal path of the amplifier. Note that while the compensation scheme is not extremely complex or brand new in nature, neither is it the simple dominant pole approach. Included are two zeros located beyond the unity gain frequency to enhance phase margin. One is created by a capacitor across the emitter degeneration resistors in the first stage and the second is formed by a resistor in series with the dominant pole capacitor.

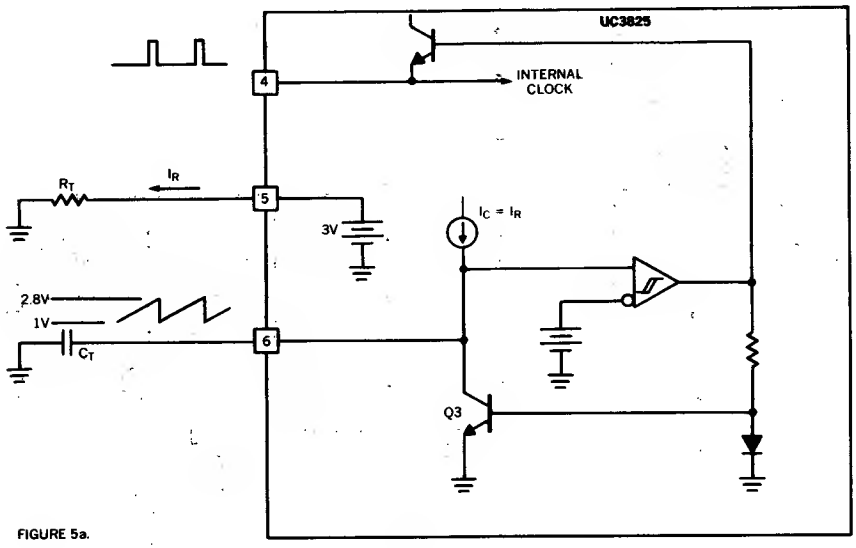

FIGURE 5a.

FIGURE 5b.

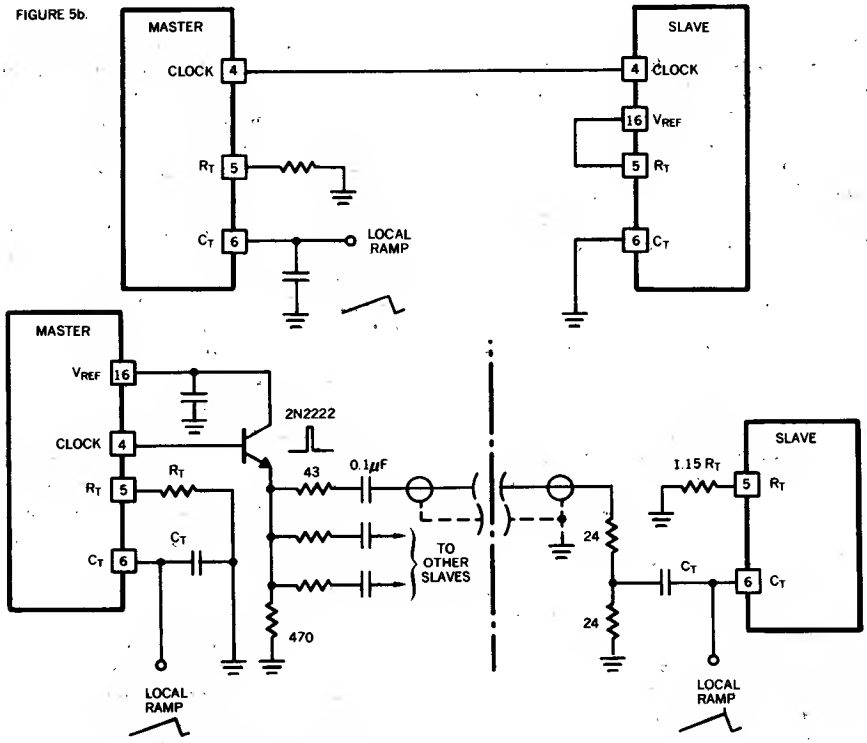

FIGURE 5. OSCILLATOR SIMPLIFIED SCHEMATIC (a) AND TWO SYNCHRONIZATION METHODS (b).

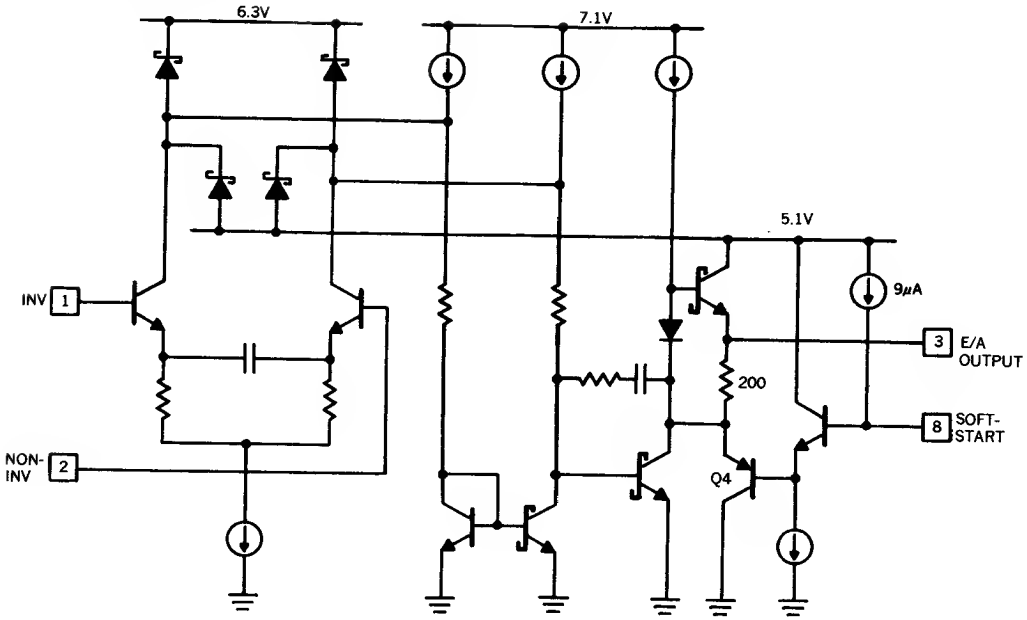

FIGURE 6. SIMPLIFIED SCHEMATIC OF WIDE BAND ERROR AMPLIFIER SHOWING SOFT START CLAMP SCHEME.

By degenerating Gm, the emitter resistors allow an increased first stage bias current level. This contributes to a 12 V/μs typical slew rate. High slew rate, while desirable for good large signal transient response, is not enough to guarantee minimal response time. Often an amplifier may have high slew rates yet exhibit long delay times coming out of saturation when it has been driven to a rail. To defeat this problem, all critical nodes within the amp have been Schottky clamped.

GLUE BLOCKS

The remaining blocks, while not speed critical, mold the 3825 into a more complete PWM controller. The reference, a time proven design, is trimmed to guarantee 5.1 Volts at better than one percent tolerance. This voltage is then held over conditions of line, load, and temperature changes to a two percent total spread.

Soft-start is very simply implemented by a pnp clamp transistor merged into the output stage of the error amp (figure 6). During soft start, while the 9 μA current source is charging the external capacitance on pin 8, Q4 actively forces pin 3 to follow pin 8. In this manner a controlled slow start can be achieved for either voltage or current mode systems. When the error amp comes into regulation, Q4's emitter-base junction is reverse biased and offers no further interference to the normal operation of the amp.

In addition to slow starts, the soft-start pin can be used to other ends. Clamping the maximum voltage this pin is allowed to rise to will then effectively clamp the maximum swing of the error amplifier. In a conventional PWM scheme this results in a duty cycle clamp while in a current mode application, it establishes the maximum peak current level.

Fault conditions are sensed by the 3825 at pin 9 which is shared by the inputs of the current limit comparator and the shut down comparator. When this pin exceeds one Volt, the current limit comparator sets the PWM latch, terminating the output for the remainder of that cycle. As with normal operation, setting the PWM latch causes the toggle flip-flop to switch states. If the pin is further raised to exceed 1.4 Volts, the shut-down comparator forces the soft-start pin to sink a guaranteed minimum of one milliampere rather than sourcing 9 microamperes. Thus the shut down comparator causes the soft start capacitor to be discharged rapidly. After the fault signal is removed the 3825 will then execute a normal soft-start sequence.

One method of combining current-limit and shut-down signals is shown in figure 7. Here, in a current mode control example, a current sense transformer is used to translate switch current to proper voltage analogs for optimal control at both the Ramp and Current-limit sense pins while the shut-down signal is inserted with a resistive summing technique.

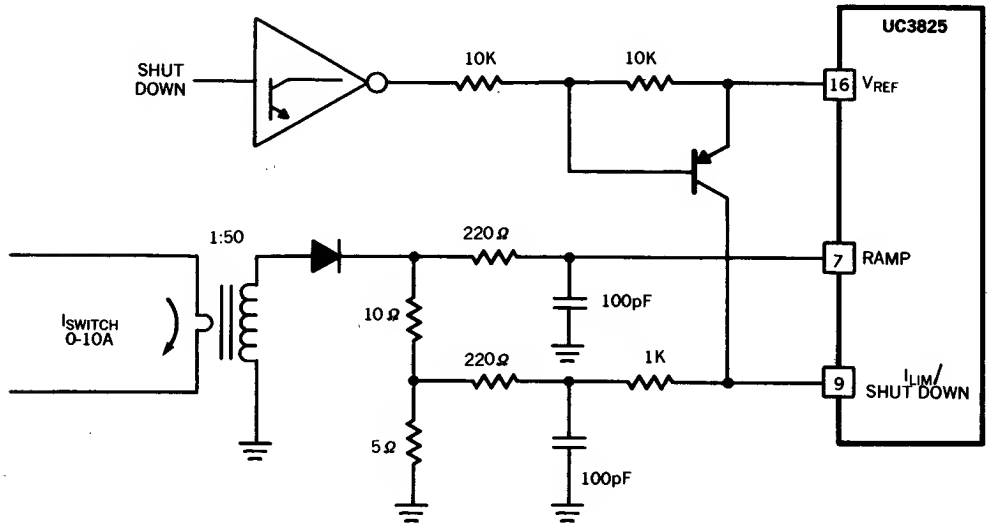

FIGURE 7. CURRENT LIMIT SENSE AND SHUT DOWN SIGNALS ARE COMBINED AT PIN 9 IN THIS CURRENT MODE EXAMPLE.

Starting the 3825 involves the Under-voltage lockout portion of the chip. This block acts like a comparator with it's inverting input biased to 9 Volts and having 0.8 Volts of hysteresis. If Vcc is below the UVLO threshold, the reference generator and the internal hias are turned off, Keeping Icc at a typical 1.1 mA and the outputs in a high impedence state. When Vcc exceeds the UVLO threshold, the reference is turned on and the chip comes alive. Bedlam is avoided, however, as a second comparator monitors the reference voltage and inhihits the outputs until the reference is high enough to ensure intelligent operation. This inhihit signal also holds the soft start pin at a low voltage. After the reference is sufficiently high, the chip begins a soft start sequence.

50 WATT DC-DC PUSH-PULL CONVERTER

A 48 to 5 Volt, 50 Watt converter has been built as a test vehicle for the chip (U-110). Designed around a push pull, current mode controlled topology, the circuit runs from a 1.5 MHz clock. In the interest of simplicity, the ramp input and current limit pins were tied together underutilizing the availahle dynamic range of the Ramp pin hy a factor of 3. A ground plane, judicious bypass capacitors and tight layout technique yielded a circuit that could be easily interrogated without significant noise interference prohlems.

In this simple application, the 3825 performs all the tasks required to regulate the 50 W power stage. The gate drive for the two power mosfets comes directly from the chip. Current loop slope compensation is resistively summed with the current sense signal at pin 7. Overall loop compensation is implemented with two resistors and a capacitor on the error amplifier. Taking advantage of the 1.5 MHz switching frequency and the wide bandwidth characteristics of the error amp, the control loop was compensated to zero dB at 300kHz.

CONCLUSION

Presenting an easy to use PWM architecture, the UC3825 possesses the necessary high speed characteristics to control switchers in the higher frequency ranges. This fills a void that has hindered high frequency applications in the past. A simple example running at 1.5 MHz points to a future of faster switching supplies.

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USING AN INTEGRATED CONTROLLER IN THE DESIGN OF MAG-AMP OUTPUT REGULATORS

By
Robert A. Mammano, Unitrode IC Corp.
Charles E. Mullett, Mullet Associates, Inc.

Magnetic amplifier technology dates back considerably further than transistors but its wide-spread use has been slow in developing. While many factors may have been responsible for this, at least one — the high cost of tape-wound magnetic cores — has been alleviated with significant recent price reductions and the introduction of less expensive materials. And now, another one — the problems in designing effective control loops utilizing mag amps as voltage regulators — has fallen with the introduction of an IC dedicated to mag amp control — the UC1838.

While there are many types of power supply applications where mag amps may effectively be used, one of the most popular current uses is as a secondary regulator in multiple output power supplies configured as shown in Figure 1. The problem with multiple outputs stems from the fact that the open-loop output impedance of each winding, rectifier, and filter is not zero. Thus, if one assumes that the overall feedback loop holds the output of V_{o1} constant, then increasing the loading on V_{o1} will cause the other outputs to rise as the primary circuit compensates; similarly; increasing the loading on any of the other outputs will cause that output to droop as the feedback is not sensing those outputs. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated and auxiliary, or secondary regulators are the usual solution. A side benefit of secondary regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratio may not match the ratio of output voltages. Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. Mag amps are a hands down winner in both areas.

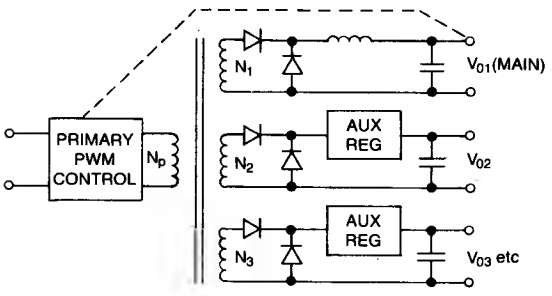

Figure 1. A typical multiple output power supply architecture with overall control from one output.

MAG AMP VOLTAGE REGULATORS

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only subtract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed. As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplied as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

MAG AMP OPERATION

Figure 2 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that N_S is a secondary winding driven from a square wave such that it provides a ± 10 volt waveform at v_i. At time $t = 0$, v_i switches negative. Since the mag amp, L1, had been saturated, it had been delivering $+10$V to v_3 prior to $t = 0$ (ignoring diode drops). If we assume $v_c = -6$V, as defined by the control circuitry, when v_i goes to -10V, the mag amp now has four volts across it and reset current from v_c flows through D1 and the mag amp for the 10 μS that v_i is negative. This net four volts for 10 μS drives the mag amp core out of saturation and resets it by an amount equal to 40V-μS.

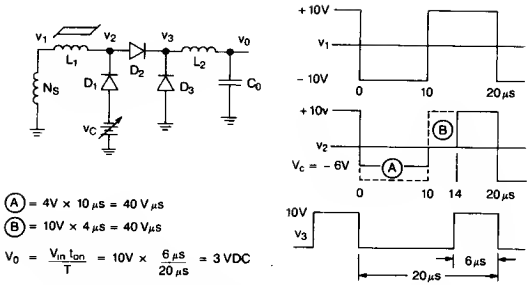

Figure 2. A simplified mag amp regulator and characteristic waveforms.

When t = 10 μS and v_1 switches back to +10V, the mag amp now acts as an inductor and prevents current from flowing, holding v_2 at 0V. This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same 40 volt-μS that was put into the core during reset.

When the core saturates, its impedance drops to zero and v_1 is applied to v_2 delivering an output pulse but with the leading edge delayed by 4 μS.

Figure 3 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

N = mag amp coil turns
Ae = core cross-section area, cm²
ℓe = core magnetic path length, cm
B = flux density, gauss
H = magnetizing force, oersteads

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I^2R loss — each term very close to zero relative to the output power.

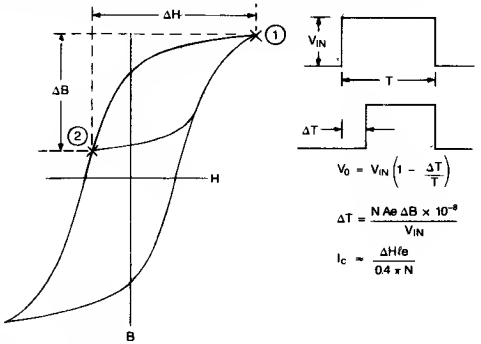

Figure 3. Operating on the B-H curve of the magnetic core.

Figure 4 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

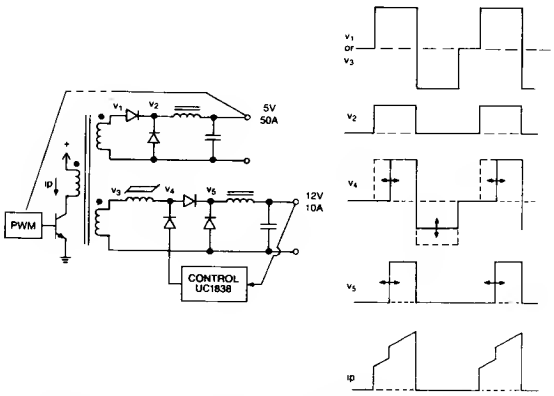

Figure 4. Control waveforms for a typical two-output, secondary regulated, forward converter.

THE UC1838 MAG AMP CONTROLLER

While bringing no major breakthroughs in either integrated circuit or power supply technology, the UC1838 provides a low-cost, easy-to-use, single-chip solution to mag amp control. The block diagrams of this device, as shown in Figure 5, includes three basic functions:

1. An independent, precise, 2.5V reference
2. Two identical, high-gain operational amplifiers
3. A high-voltage PNP reset current driver.

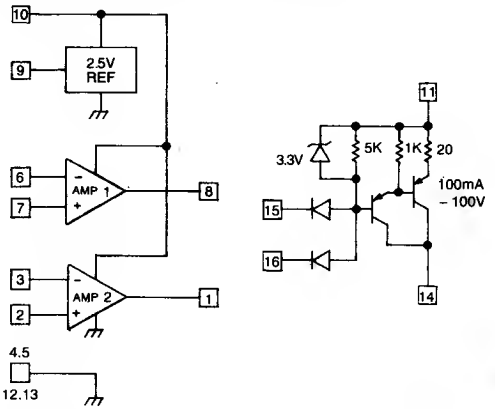

Figure 5. The block diagram of the UC1838 mag-amp control integrated circuit.

The reference is a common band-gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The two op amps are identical with a structure as shown simplified in Figure 6. These amplifiers have PNP inputs for a common mode input range down to slightly below ground and have class A outputs with a 1.5 MA current sink pull down. The open loop voltage gain response, as shown in Figure 7, has a nominal 120 dB of gain at DC with a single pole roll-off to unity at 800 KHz. These amplifiers are unity-gain stable and have a slew rate of 0.3 V/μS.

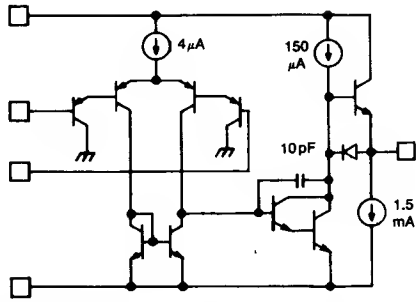

Figure 6. Simplified schematic of each of the operational amplifiers contained within the UC1838.

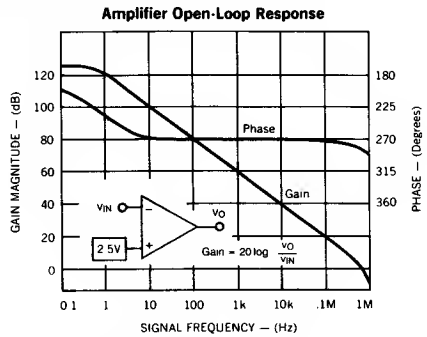

Figure 7. Open-loop gain and phase response for the UC1838 op amps.

Two op amps are included to provide several design options. For example, if one is used to close the voltage feedback loop, the other could be dedicated to some protective function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 MA of reset current with a collector voltage swing of as much as 80 volts negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR" ed to turn on the driver, turning off the supply output.

With internal emitter degeneration, this reset driver operates as a transconductance amplifier providing a reset current as a function of input voltage as shown in Figure 8. The frequency response of this circuit is plotted in Figure 9 showing flat performance out to one megahertz.

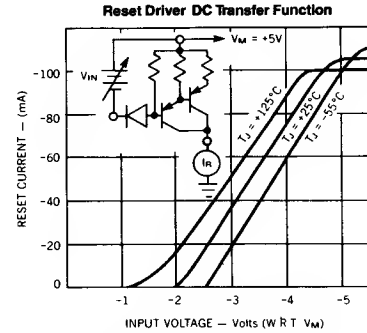

Figure 8. Transconductance characteristics of the UC1838 reset current generator.

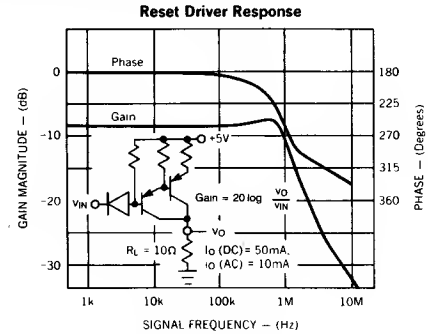

Figure 9. Reset driver frequency response.

Current limiting to protect the output driver is achieved by means of the 3.5 V Zener clamp (which is temperature compensated to match two VBE's) in conjunction with the 20Ω emitter resistor. It should be noted that thermal shutdown is purposely not included since protecting the driver by turning it off would mean losing control of the power supply output. Pin 11 — the emitter of the driver — can be connected to any convenient voltage source from 5VDC to the level used to supply the op amps. Note that the op amp supply must be at least 2 volts higher than the DC level on the inputs, a point to remember when selecting a location for current sensing. One possible configuration for a complete secondary regulator with shutdown control is shown in Figure 10.

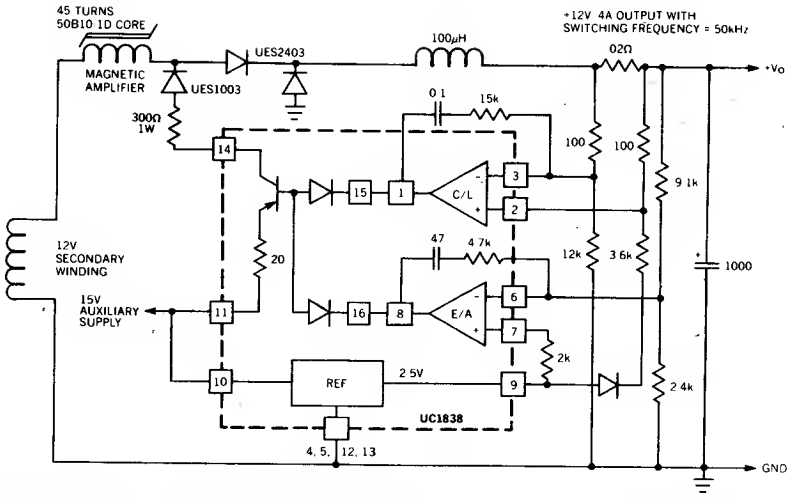

Figure 10. Using the UC1838 to provide both voltage control and over-current shutdown in a typical 12V, 4A regulator.

MAG AMP DESIGN PRINCIPLES

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 11. Some considerations affecting the choices could be:

1. A lower Bmax requires more turns — less important at higher frequencies since fewer turns are required.
2. Higher squareness ratios make better switches
3. Higher I_M requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely

MATERIALS

Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.

Trade Name	Composition	Bmax (kG)	Core Loss @ Bmax	Squareness Ratio	Turns Req'd	I_M (A)
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonol	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.8W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

Figure 11. A comparison of several types of core materials available for mag amp usage.

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the "withstand area," Λ — which the mag amp will be expected to support

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 amp/cm² is a common design rule.
2. Determine core size based upon the area product:

$$AwAe = \frac{Ax \times \Lambda \times 10^8}{\Delta B \times K} \quad \text{where}$$

Aw = Window area, cm²
Ae = Effective core area, cm²
Ax = Wire area, (one conductor) cm²
Λ = Required withstand area, V-sec
ΔB = Flux excursion, gauss
K = Fill factors ≈ 0.1 to 0.3

3. Calculate number of turns from

$$N = \frac{\Lambda \times 10^8}{\Delta B \times Ae}$$

4. Estimate control current from

$$Ic \approx \frac{Hle}{0.4\,\pi\,N} \quad \text{where}$$

l_e = core path length, cm
H is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\Delta T \approx \frac{P \text{ watts}^{0.8}}{A \text{ (surface) cm}^2} \times 444\,^{\circ}C$$

6. Once the mag amp is defined, it can be used in the power supply to verify I_C and to determine the modulator gain so that the control requirements may be determined.

9

COMPENSATING THE MAG AMP CONTROL LOOP

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency.

Figure 12 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

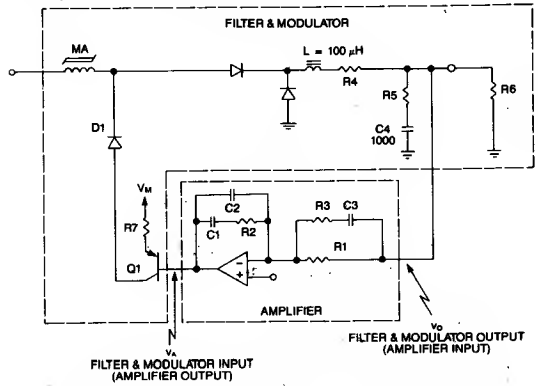

Figure 12. Schematic diagram of a typical regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4) and their parasitic resistances R4 and R5. For this discussion, a 20 KHz, 10 Volt, 10 Amp regulator is used. The output inductor has been chosen to be 100 μH, the capacitor is 1000 μF and each has .01 ohms of parasitic resistance. The load resistor (R6) of 1 ohm is included since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 13 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is $1/(2\pi\sqrt{LC})$, or 316 Hz, and that the magnitude of the response "rolls off" at the slope of -40 dB per decade above the corner frequency. Note also that the phase lag asymptomatically approaches 180 degrees above the corner frequency.

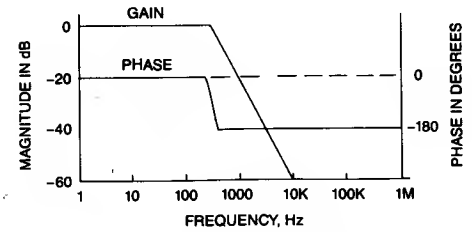

Figure 13. Output filter response.

To include the effects of the mag amp modulator, we must consider the additional phase shift inherent in its transfer function. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the "backswing" of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\varnothing m = -(2D + \alpha)\frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time
α = resetting impedance factor: = 0 for a current source; = 1 when resetting from a low-impedance source; and somewhere in between for an imperfect current source.
ω_S = $2\pi f_S$, where f_S = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 14 illustrates this point. With $\alpha = 0$, we insert no phase delay, and with $\alpha = 1$ we insert maximum phase delay, which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

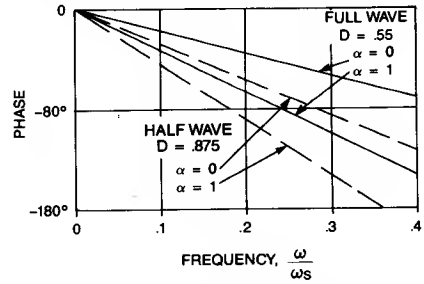

Figure 14. Mag amp phase shift.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the

filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator's phase shift.

Using this technique, the Bode plot for the modulator and output filter of this example has been calculated assuming $\alpha = 0.2$ and $D = 0.6$ yielding the graph of Figure 15.

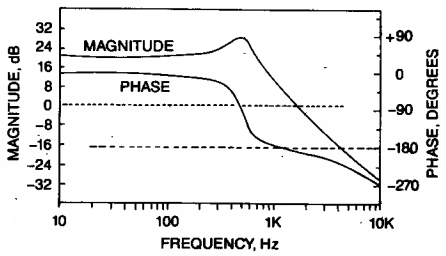

Figure 15. Filter-modulator response including the effects of mag amp phase delay.

If we now close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called "dominant pole" compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 12 allows us to do a much better job, by adding a few inexpensive passive parts. It has the simplified response shown in Figure 16. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.

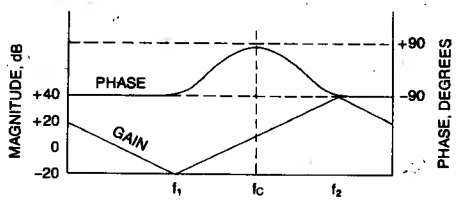

Figure 16. Compensated amplifier frequency and phase response.

The important point is that this circuit provides a phase "bump" — it can have nearly 90° of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies, f1 and f2. This benefit is not free, however. As we ask for more boost (by increasing the separation between f1 and f2) we demand more gain-bandwidth of the amplifier.

DESIGN EXAMPLE

An 8V, 8A Output Derived from a 12V Output — 20 KHz Push-Pull Converter

This example uses the UC1838 to control a full-wave mag amp output regulator, with independent shutdown current limiting. Capsule specifications are as follows:

INPUT: PWM quasi-square wave which, without the magamp, produces 12 Vdc.

OUTPUT: 8.0 Vdc ±1% at load currents from 1 to 8A.

OUTPUT RIPPLE: Less than 50 mV p-p.

TRANSIENT RESPONSE: For load changes of 6 to 8 and 8 to 6A, peak excursion of the output shall be less than ±2% and settle to within 1% of the final value within 500 μS.

OUTPUT PROTECTION: The 8V output shall have independent current limiting, so as not to shut down the 12V output when the 8V output is overloaded or short-circuited. It shall recover from the overload automatically when the overload is removed.

Figure 17 shows the proposed circuit approach. A current transformer has been used to sense the overload, simply to illustrate this approach. A simple series resistor of perhaps .01 or .02 ohms would do as well here, but the current transformer is preferred for high-current outputs.

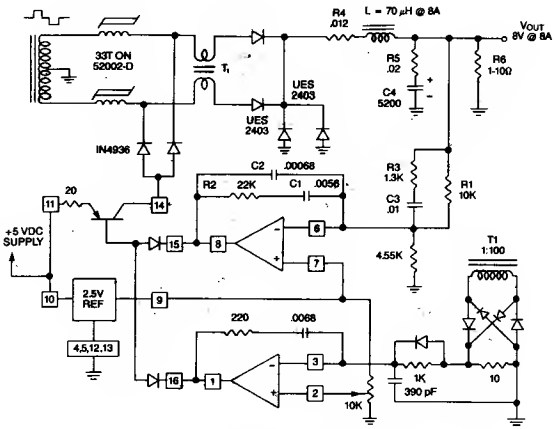

Figure 17. Control and current limiting for a 8V, 8 amp, 20 KHz push-pull converter.

DESIGN APPROACH

With the input waveform already set by the converter design, and the above specifications to define the desired output, the new output circuit will be approached as follows:

1. Draw the preliminary schematic.
2. Design the mag amp.
3. Design the feedback loop.
4. Design the current limiter.
5. Build the breadboard and test it.

PRELIMINARY SCHEMATIC

Figure 17 shows the preliminary circuit diagram. Parasitic resistance of the output filter inductor and capacitor (R4 and R5) are shown, along with the expected feedback com-

pensation elements (R1, R2, R3, C1, C2, and C3). These will be referenced in the mag amp design.

MAG AMP DESIGN

The information necessary to the design is as follows:

1. Input pulse: nominally 32V × 9 μS, = 288 volt-microseconds.
2. Duty ratio of the "off" time: nominally (25 - 9 μS)/ 25 μS = .76, since the frequency at the output is 40 KHz.
3. Output current: 8A.
4. Regulation only, or complete shutdown required? Shutdown.

Comments on the output filter

Design of the output filter is not complicated by the presence of the mag amp. In this case, it was designed with output ripple specs, and capacitor ripple current in mind. Although this design has adequate inductance for continuous conduction of the inductor at minimum load, this is not mandatory. The mag amp, when designed for shutdown, is capable of regulating the output in the discontinuous conduction mode.

Mag amp core selection

1. Wire size: The current waveform in the magamp can be analyzed as follows: During the power pulse, the current is approximately 8A (inaccurate only due to the "tilt" of the top of the current pulse); the duty ratio of this pulse is half the ratio of the output voltage to the pulse height, or .5 × 8/30 = .12. During the dead time between pulses, the inductor current is shared by the rectifier diodes and the "catch" diode. The duty ratio is 1 - 2 × .12 = .76, and the current during this interval is 8/3A. During the remaining interval the current is zero, because the entire 8A is flowing in the other mag amp.

   The rms value of the current can now be computed:

   $$Irms = \sqrt{8^2 \times .12 + (8/3)^2 \times .76} = 3.62 \text{ A.}$$

   At 400 Amp/cm², a wire area of approx. .0091 cm² is required. 16 gauge wire has an area of .0131 and is chosen for the mag amp.

2. Core selection: An appropriate material at this frequency is square-loop 80% nickel (Square Permalloy 80 or eq.) with a tape thickness of 1 mil. The saturation flux density if this material is 7000 gauss. A fill factor of 0.2 is chosen for the winding. The required area product is:

   $$AwAe = \frac{Ax \times \Lambda \times 10^4}{\Delta B \times K} = \frac{.0131 \times 288 \times 10^{-6} \times 10^4}{2 \times 7000 \times 0.2} = .135 \text{ cm}^4$$

   which can be divided by 5.07 × 10^{-6} cm²/C.M. in order to refer to core manufacturer's tables.

   An appropriate core is the Magnetics 52002-10, which (with 1 mil tape thickness) has an area product of .026 × 10^6 C.M. cm². The core area of this core is 0.076 cm².

3. Determine the number of turns: The mag amp must be able to withstand the entire area of the input pulse, which is 288 volt-microseconds.

   $$N = \frac{\Lambda \times 10^8}{2 \times Bm \times Ac} = \frac{288 \times 10^{-6} \times 10^8}{2 \times 7000 \times .076} = 27 \text{ turns.}$$

   Allowing an extra 20% for variations in Bm, pulse dimensions, etc., the winding is chosen to be 33 turns.

FEEDBACK LOOP DESIGN

The key steps in the design of the feedback loop are as follows:

1. Determine the modulator's dc transfer function.
2. Plot the transfer function of the modulator and filter, to determine the gain and phase boost required of the feedback amplifier.
3. Design the feedback amplifier.
4. Plot the results in the form of the closed-loop transfer function.

Plotting the modulator's transfer function can be easily done experimentally with the UC1838 by opening the feedback loop at the input to the Reset Driver and driving this point (pin 15 or 16) directly. For interest, the reset current is also measured with the help of a 1 ohm resistor placed in series with the emitter of the reset transistor (pin 11 of the UC1838). The results are shown in Figure 18, with load resistors of 1 ohm and 10 ohms.

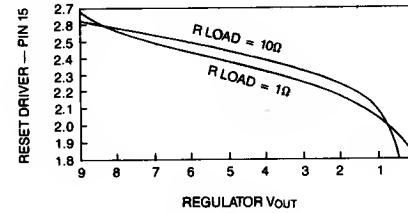

Figure 18. DC gain of the mag amp modulator.

Note that the results are practically the same at both load values. This is to be expected, since the output inductor is still in the continuous conduction mode at the minimum load.

In the region of the desired output (8V and 8A load), the modulator dc gain is approximately 12.5, or 22 dB. In addition to the phase shift of the filter, the modulator contributes additional phase lag! Assuming that we will not attempt to cross unity-gain at a frequency above one-tenth the switching frequency, we can neglect the phase lag due to the impedance of the core and the reset circuit. But we cannot neglect the phase lag resulting from the delay between the time of resetting the core and the time when the core delivers its output:

$$\varnothing_M = 2D \frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time (.76 in this example)
ω_S = 2 D f_a, where f_a = the switching frequency (40 KHz)

We can use any one of the common circuit analysis programs for analyzing the filter-modulator, neglecting the modulator phase lag when running the program, and then adding it later. Or, the lag may be included in a more sophisticated analysis program. The resultant response prediction is shown in Figure 19.

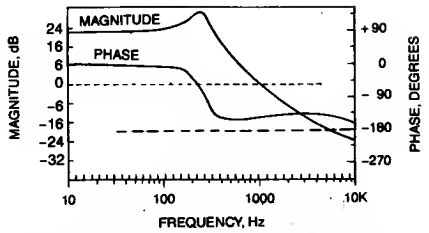

Figure 19. Calculated response plot for the modulator and filter.

Note the shape of the phase response. In the region of 2 KHz the phase lag is decreasing, due to the ESR of the output capacitor. Above 6 KHz the modulator's phase lag becomes important, and the phase lag increases.

Choosing one-tenth the switching frequency for the unity-gain crossover frequency (4 KHz), we can determine the desired gain and phase boost of the feedback amplifier. At 4 KHz, the gain of the modulator is -15 dB (a factor of .179) and the phase shift is -135 degrees. It is generally recommended that there be at least 60 degrees of phase margin at the crossover frequency. This will require reduction of the phase lag to -120 degrees.

In accordance with the design procedure of Venable[2], the required boost is:

Bc = M - P - 90, where

M = desired phase margin, and P = filter & modulator phase shift.

In this case, Bc = 60 - (-135) -90 = 105 degrees. This is comfortably within the theoretical limit of 180 degrees, inherent in the amplifier configuration shown in Figure 17. The gain required at the crossover frequency is the reciprocal of the modulator's gain, or +15dB = a gain of 5.6.

Continuing with the procedure, we can now compute the amplifier components:

$K = (\text{Tan}\ [\ (Bc/4) + 45]\ )^2 = 8.65$

$C2 = 1/(2\pi f G R1) = .00071\ \mu F$

$C1 = C2\ (K - 1) = .0055\ \mu F$

$R2 = \sqrt{K}/(2\pi f C1) = 21{,}485$ ohms

$R3 = R1/(K - 1) = 1{,}302$ ohms

$C3 = 1/(2\pi f \sqrt{K} R3) = .01\ \mu F$

where f = crossover frequency in Hz, G = amplifier gain at crossover (expressed as a ratio, not as dB), and K is a factor which describes the required separation of double poles and zeroes to accomplish the desired phase boost. These frequencies are:

$f1 = f/\sqrt{K}$ (double zero), and $f2 = f\sqrt{K}$ (double pole),

In this example, f1 = 1361 Hz and f2 = 11.76 KHz. With this information at hand, it is wise to check the gain-bandwidth required of the feedback amplifier to see that the circuit's needs can be met with one of the amplifers in the UC1838. Knowing that the amplifier rolloff is 20 dB per decade, we can simply calculate the required gain-bandwidth at f2 and see that it is well below the gain-bandwidth of the amplifier.

The gain at f2 is:

$Gf_2 = \sqrt{K}\ G$, and hence the required gain-bandwidth is:

$GBW = \sqrt{K}\ G\ f2 = K\ G\ f$, where G is the desired gain at crossover.

In this example, GBW = 8.65 × 5.6 × 4000 = 194 KHz. This is comfortably below the gain-bandwidth of the amplifier, which is 800 KHz.

For interest, the response of the amplifier is plotted in Figure 20. Note that the gain reaches a minimum at 1.3 KHz, and that the phase boost peaks at 4 KHz, as intended.

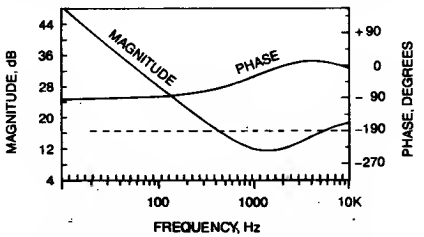

Figure 20. Compensated amplifier response.

Figure 21 shows the overall response, combining the filter-modulator's response with that of the feedback amplifier. Note the 60 degrees of phase margin at the crossover frequency.

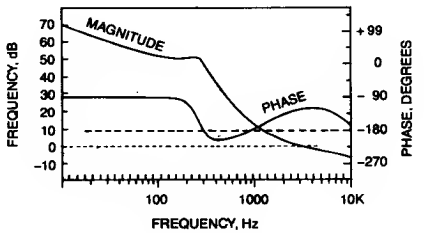

Figure 21. Total loop response with 60 degrees of phase margin at crossover.

CURRENT LIMITER DESIGN

Although a series sensing resistor might have been acceptable at this level of output current, a current transformer, T1 in Figure 17, has been used for the sake of interest. The secondary has 100 turns, and each primary winding is simply one pass through the toroid.

The amplifier performs as an integrator rather than as a comparator, the form found in many primary current limiters of switched-mode controllers. This is not an arbitrary choice. Since the current pulse occurs during the time that the core is obviously not being reset, the circuit must have "memory" — it must apply a shutdown command to the reset transistor during the next reset interval. Although many sophisticated schemes can be devised, the integrator is attractive because of its simplicity.

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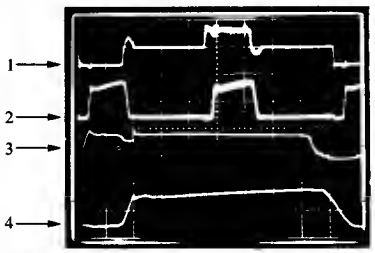
A diode is placed across the input resistor of the integrator, to force its output down quickly when receiving the narrow pulses which occur when the circuit is in current limit. The circuit of this example was developed experimentally. A future goal is to explore this in detail and develop a more rigorous approach. The performance of this circuit is illustrated with waveform photos later in the paper.

BREADBOARD TEST RESULTS

Figure 22 shows the waveform of the input voltage which is applied to the mag amp core, and the current of the two mag amps combined (by placing a current probe on the return leg of the secondary of the converter's transformer). The lower two traces are expanded versions of the top ones, and one can see clearly the effect of the transformer's leakage inductance: the voltage pulse has a "dent" in it during the rise of the current in the mag amp.

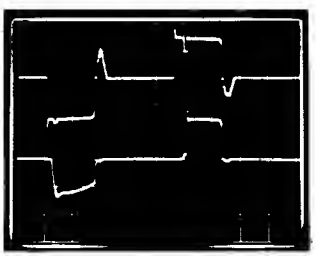


1. Secondary voltage, 50V, 5 μs/div.
2. Current in return (center tap) of secondary. 5A, 5 μs/div.
3. Secondary voltage, 50V, 1 μs/div.
4. Current in return (center tap) of secondary. 5A, 5 μs/div.

Figure 22. Input voltage and current to the mag amp.

Also note the "backswing" at the end of each voltage pulse. This is the discharge of the energy stored in the saturated inductance of the mag amp core. Finally, note the rate of rise of the current pulse, which is determined by the saturated inductance of the mag amp, in series with the leakage inductance of the transformer.

Figure 23 illustrates the operation of the mag amp in more detail. The upper trace is the input voltage of the mag amp, and the lower trace is its output. The reset volt-second product is the difference between the negative pulses of the two traces. The shape of the negative pulse in the lower trace is due to the changing impedance of the mag amp core during reset.

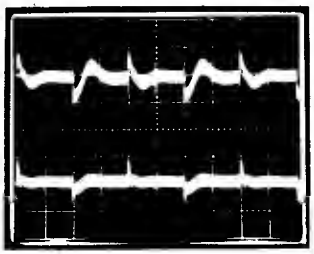


Top: Secondary voltage (into mag amp), 20V × 5 μs/div.
Bot: V_{OUT} of mag amp, 20V × 5 μs/div.

Figure 23. Mag amp operation.

Control loop transient response

To test the response of the regulator to step changes in load, an electronic load was square-wave modulated at 500 Hz, between the values of 6A and 8A. The results are shown in Figure 24. The upper trace is the regulator's output voltage, showing peak excursions of less than 50 mV, and recovery time of .5 ms. The lower trace is the reset current, measured with a current probe at the collector of the reset transistor in the IC.

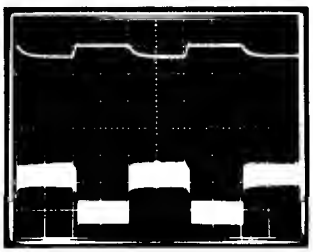


Output transient response 6-8A ΔI_{LOAD}
Top: Output voltage, 50mV × .5 ms/div.
Bot: Reset current, 20mA × .5 ms/div.
(Measured at collector of UC1838 transistor)

Figure 24. Dynamic regulator response to step change in load between 6 and 8 amps.

Response of the current limiter

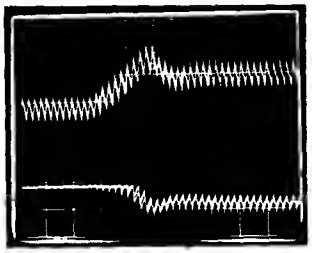
To illustrate the dynamic operation of the limiter, the current limit was set at 7A, and then the electronic load was modulated between 5.7A and 8.7A at a rate of approximately 25 Hz. Figure 25 shows the output voltage in the top trace. The lower trace is the current in the output inductor. Note that the output voltage is well-behaved and that there is no overshoot of the inductor current.



Top: V_{OUT}, 2V × 20 ms/div.
Bot: Inductor current, 2A × 20 ms/div.

Figure 25. Response of current limiter with load switched between 5.7 and 8.5A; with current limit set at 7.5A.

Finally, Figure 26 shows the operation of the current-limiting amplifier. The upper trace is the inductor current, and the lower trace is the output voltage of the current-detecting amplifier. Note the output waveform of the amplifier. Although the amplifier performs as an integrator, it slews fast enough to keep up with the rate of rise of the inductor current, thus adequately protecting the converter and output rectifiers.



Top: Inductor current, 2A × .1 ms/div.
Bot: V_{OUT} of C.L. amp (pin 1), 2V × .1 ms/div.

Figure 26. Response time of current limit amplifier.

APPLICATIONS AT HIGHER SWITCHING FREQUENCIES

As mag amp output regulators are applied at higher and higher switching frequencies, the second-order effects, of course, become more significant.[3] Leakage inductance of the transformer and saturated inductance of the mag amp rob the circuit of its control range, since these produce additional dead time at the leading edge of the output pulse. Even without the mag amp output regulator, this can be a problem in high-frequency switched-mode converters.

Diode storage time has the same result. If the output side of the mag amp "sticks" at ground (during reverse recovery of the rectifier) while its input voltage swings negative, some unwanted reset will be applied to the mag amp. There are techniques to deal with this problem, by providing a shunt recovery path around the mag amp to remove the stored charge in the diode.[4]

The control circuit of the mag amp regulator is not involved in the cycle-by-cycle operation of the circuit; hence, the control IC is not a major barrier to raising the operating frequency. It does affect the situation in an indirect way, however. Its gain-bandwidth may limit the speed of transient response such that the loop crossover frequency cannot be raised in proportion to the switching frequency. In most applications this will not be objectionable. If it is, an outboard op amp can provide the additional gain-bandwidth. If the regulator is not required to have its own current limiter, then the second amplifier can be used in cascade with the first, to provide additional gain-bandwidth.

The integration of the circuit blocks required to implement mag amp output regulators is an important contribution. It is especially beneficial to have the reset transistor included, as this can even eliminate a small heat sink. Finally, it is helpful not only in the design process but also in production to have a single component which encompasses all of the active control functions. As more and more designers are working with the same component, the development of the technology will be more focused, and this will be universally beneficial.

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4. C. E. Mullett and R. Hiramatsu, "An Improved Parallel Control Circuit for Saturable Reactor Output Regulators in High-Frequency Switched-Mode Converters," Proceedings of The IEEE Applied Power Electronics Conference and Exposition, April, 1986, pp. 99-106.
5. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, FL in the development of the UC1838.

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1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

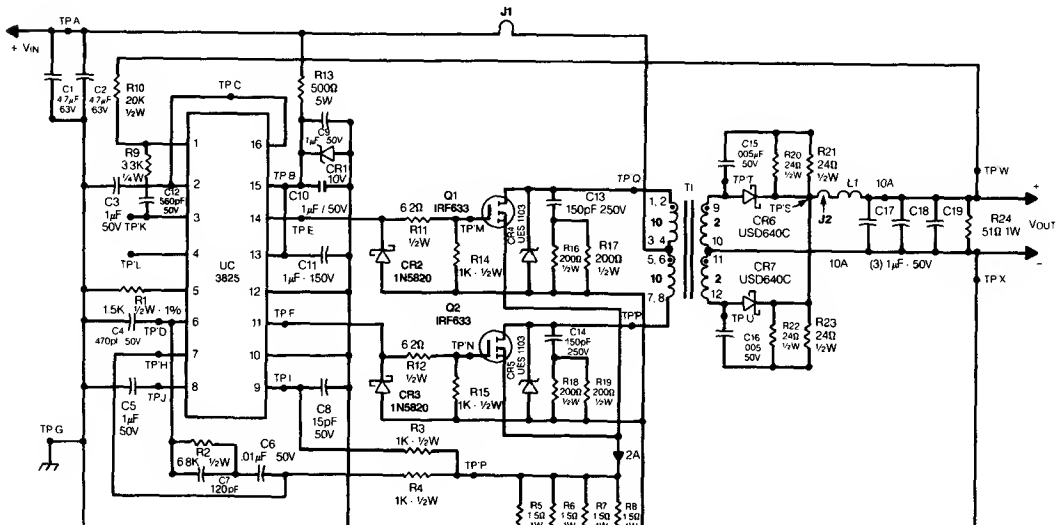
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825. Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.[1]

Figure 1. Schematic Diagram



II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2–10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

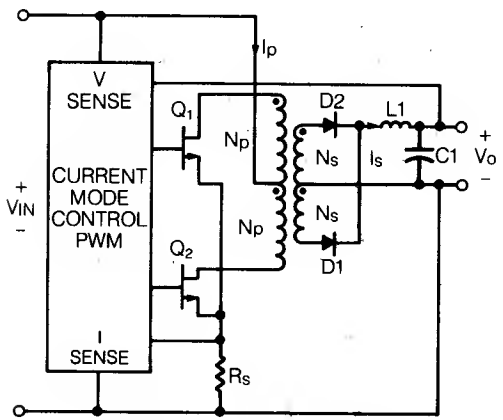


Figure 2. Basic Diagram — Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_s. Simultaneously, diode D1 conducts current $I_p \times N_p/N_s$ in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

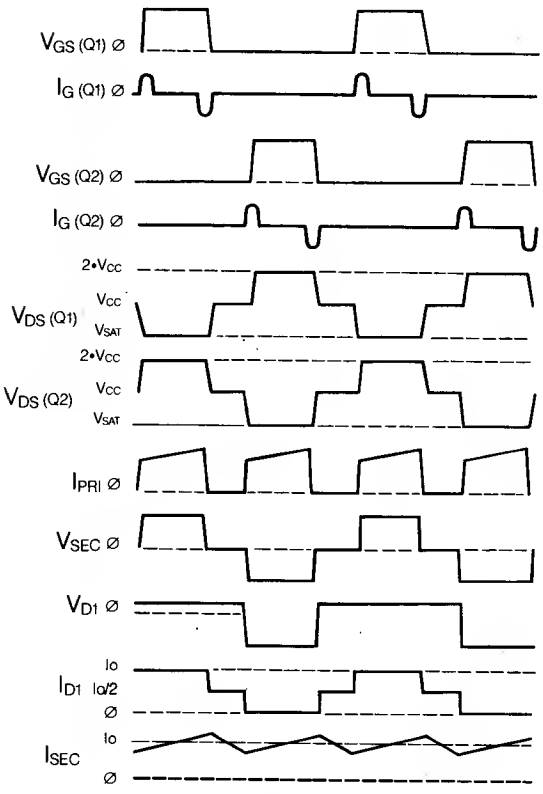


Figure 3. Basic Push-Pull Waveforms

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IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{cc} and V_c (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures are used for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} = \frac{68\text{ watts}}{42\text{ volts}} = 1.62\text{ A}$$

The primary current during the transistor on time is:

$$\text{I (p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \le \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload; V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

P dc = I dc² Rds max • duty
= 2² • 0.8 • 0.85/2 = 1.35 watts

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 -150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) – V xtor (max) – V (Rs) max
V p (min) = 42 v – 2.0 v – 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)
V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \bullet Duty\ (max) \bullet 10^4}{2 \bullet Freq. \bullet N\ (p) \bullet \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared[2] and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \bullet Np = \frac{V\ pri \bullet D\ max \bullet 10^4}{2 \bullet F \bullet \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \bullet 0.85 \bullet 10^4}{2 \bullet 750{,}000 \bullet 10 \bullet 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise[3]

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

$$d\ pen = 7.5 / (frequency^{0.5})\ (cm)$$

At 750 kHz, this corresponds to $8.66 \bullet 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

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For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm²

Primary area (Axp) = 1.24A / 450A / cm² = $2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$I\,rms\,(sec) = \frac{I\,sec^2\,(duty\ on) + \frac{I\,sec^2}{2}(2 \cdot duty\ off)}{2}$$

$$I\,rms\,(sec) = \frac{10^2\,(.425) + \frac{5^2}{2}(2 \cdot .075)}{2}$$

$I\,rms\,(sec) = 4.81A$

Secondary Area (Axs) = 4.81A / 450A / cm²
= $1.07 \cdot 10^{-2}$ cm²

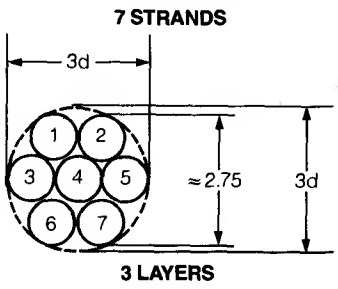

Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\#\,\text{conductors}} = \frac{Axp}{7} = \frac{2.75 \cdot 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ \text{cm}^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07 \cdot 10^{-2}\ \text{cm}}{1.40\ \text{cm}} = 7.64 \cdot 10^{-3}\ \text{cm}$$

This corresponds to 0.003″ thick foil, a standard value. In practice, slightly thicker foil (0.004″ to 0.005″) may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

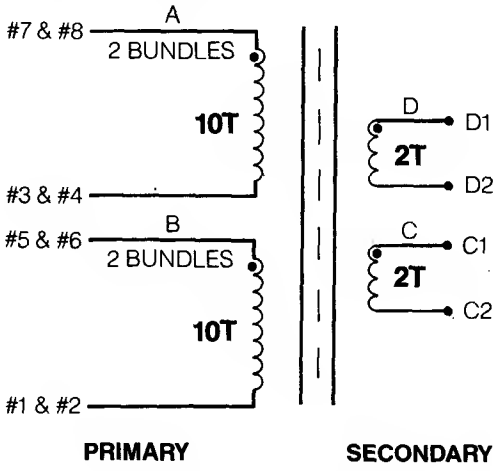

Figure 5. Transformer Schematic

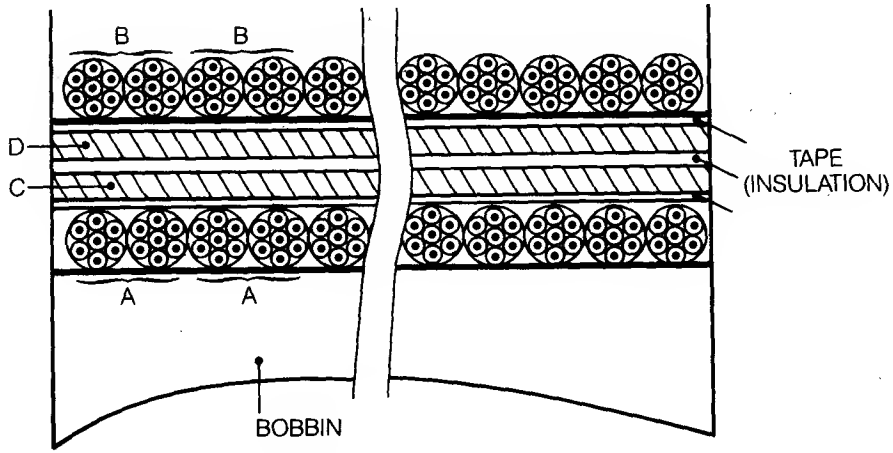

Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of $1.82 \cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$Rpri = \frac{R\ wire \cdot M.L.T. \cdot \#\ turns}{\#\ wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586\ ohm$$

Voltage drop and power loss in each half winding can be also calculated:

$$V\ (R\ pri) = Ipri \cdot Rpri = 2.0 \cdot 0.58 = 0.116\ volt\ (negligible)$$

$$P\ (Rpri) = R\ pri \cdot I\ pri^2 \cdot duty = 0.0586 \cdot 4 \cdot 0.425 = 0.0996\ watts$$

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec $= 1.58 \cdot 10^{-4}$ ohms/cm.

$$Rsec = R\ foil \cdot M.L.T. \cdot \#\ turns = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2 = 0.00143\ ohm$$

$$V\ (Rsec) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143\ volt\ (negligible)$$

$$P\ (Rsec) = R\ sec\ ((Idc^2 \cdot D\ on) + ((Idc/2)^2 \cdot 2 \cdot D\ off))$$

$$P\ (Rsec) = 0.00143\ ((10^2 \cdot 0.425) + (5^2 \cdot 0.15) = 0.066\ watts$$

Transformer Power Losses

The total copper losses for two windings are then:

$$P\ cu = P\ (Rpri) + P\ (Rsec) = 2 \cdot (0.066 + 0.0996) = 0.332\ watts$$

Estimated eddy current losses are approximately 50% of the copper losses. Pcu ≈ 0.50 watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$$P\ core = 3.327 \cdot 0.15 = 0.50\ watt$$

The total power lost is a summation of the copper and ferrite losses:

$$P\ xfmr = P\ cu + P\ core = 0.50 + 0.50 = 1.00\ watts$$

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\ di}{dt} : L = \frac{V\ dt}{di} = \frac{5.9\ v\ (350)\ 10^{-9}\ s}{3.0\ A} = 690\ nanohenries$$

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Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \cdot N^2 \cdot D\ (in)$, $N = (L/F \cdot D)^{1/2}$ (turns)

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690 / 0.0173 \cdot 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns, the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \cdot 10^2 \cdot 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \cdot \frac{T\ period}{2} \cdot \frac{I}{2}, \text{ Delta } Q = I\ p\text{-}p / 8 \cdot F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p / 8 \cdot F \cdot dV = 3 / 8 \cdot 1.5 \cdot 10^6 \cdot 0.10 \approx 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit / Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section — slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information. Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability[5]

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7), that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

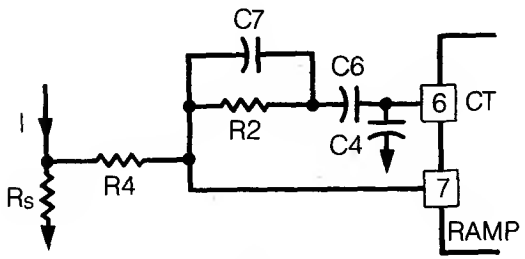


Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

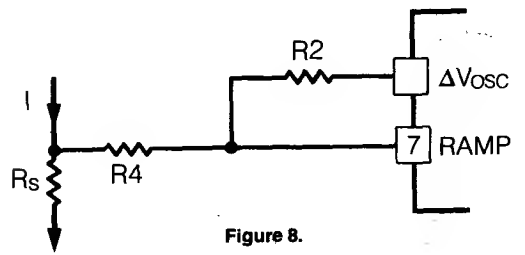


Figure 8.

STEP 1. Calculate Inductor Downslope
$S(L) = di/dt = V\,sec / L = 5.9\,V / .740\,\mu H = 8.0\,A/\mu s$ (1)

STEP 2. Calculate Reflected Downslope to Primary
$S(L)' = S(L) / N\,(turns\ ratio) = 8.0/5 = 1.6\,A/\mu S$ (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage
$V\,S(L)' = S(L)' \cdot Rsense = 1.6 \cdot 0.375 = 0.600\,V/\mu s$ (3)

STEP 4. Calculate Oscillator Slope
$V\,S\,(osc) = d\,(V\,osc) / T\,on = 1.8\,V / 570\,ns = 3.15\,V/\mu s$ (4)

STEP 5. Generate the Ramp Equations
Using superposition, the circuit can be configured as:

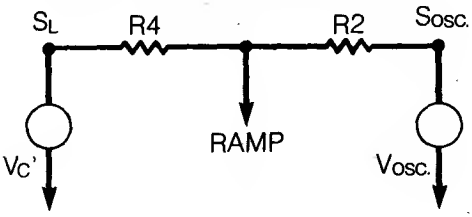


Figure 9.

$$V\,(ramp) = \frac{V\,S\,(L)' \cdot R2}{R2 + R4} = \frac{V\,S\,(osc) \cdot R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,
$V\,(ramp) = V\,S\,(L)'' + V\,S\,(comp)$ (6)

WHERE

$$V\,S\,(comp) = \frac{V\,S\,(osc) \cdot R4}{R2 + R4}; \quad V\,S\,(L)'' = \frac{V\,S\,(L)' \cdot R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation
$V\,S\,(comp) = m \cdot S(L)''$ (7)

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S\,(osc) \cdot R4}{R2 + R4} = \frac{m \cdot V\,S(L)' \cdot R2}{R2 + R4}$$

SOLVING FOR R2:

$$R2 = R4 \cdot \frac{V\,S\,(osc)}{V\,S\,(L)' \cdot m} = R4 \cdot \frac{3.15}{0.600 \cdot 0.75} \quad (9)$$

USING CIRCUIT VALUES,
$R2 = 7.05 \cdot R4$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

9

CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency.[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\,\pi\,R\,(load)\,C\,(output)$

$F_z = 1/2\,\pi\,R\,(esr)\,C\,(output)$

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min - 0.300 max

For three capacitors in parallel, ESR = 0.016 - 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

$F_p\,(2A) = 1/(2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

$F_p\,(10A) = 1/(2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

$F_z\,(high) = 1/(2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

$F_z\,(low) = 1/(2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V\,(output)}{V\,(control)} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V\,(control)} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76 \cdot 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of -16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = 1 / (2 • π • R9 • C12)

therefore, C12 = 1 / (2 • π • R9 • F zero)

C12 = 1 / (2 • 3.14 • 3300 • 100.000) = 480 pF (use 560 pF)

R10 / R9 = approx -16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

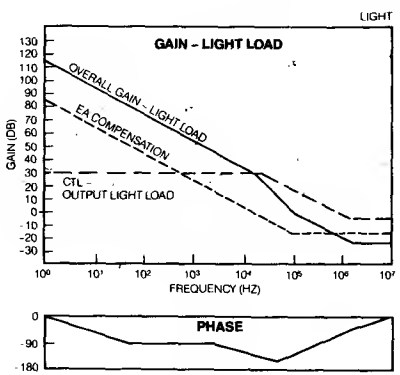


Figure 11.

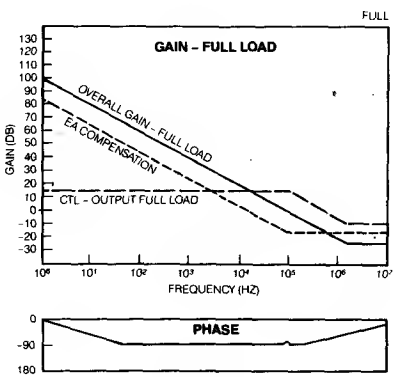


Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13, 14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2, 3	USD1140	40 V, 1 Amp Schottky
CR4, 5	UES1105	150 V, 2.5 Amp Ultrafast
CR6, 7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1, 2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1 K, 1/2 W, 5%	
R5-8	1.5 R, 1 W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5 W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink—Mosfets (AAALL #5786B)	
H2	Heatsink—Diodes (AAALL #5299B)	

Efficiency Measurements

V (In)	I (In)	P (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

V (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg. MV
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses

Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 W
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

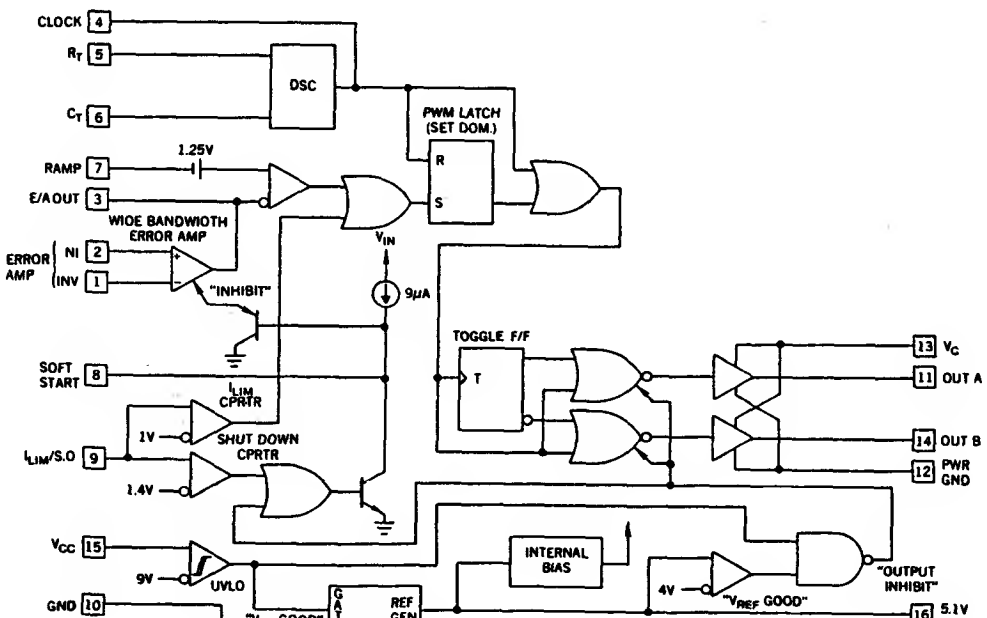
Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

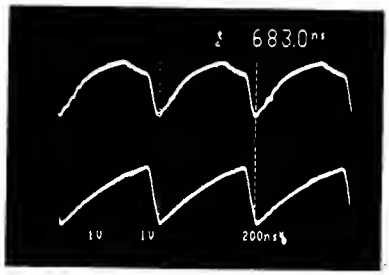
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section C1 — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



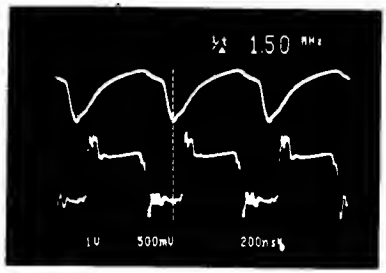
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H', 1 v/cm

Bottom Trace
CT Waveform,
TP 'D', 1 v/cm

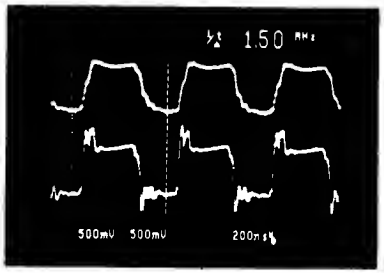
RAMP VOLTAGE



Top Trace
Filtered Ip with
Slope Compensation
TP 'H', 1 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

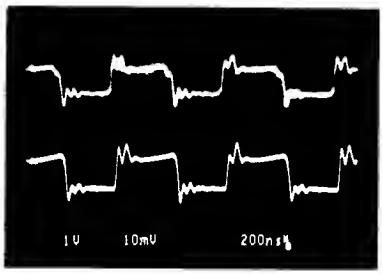
PRIMARY CURRENT



Top Trace
Filtered Ip
TP 'I', .5 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

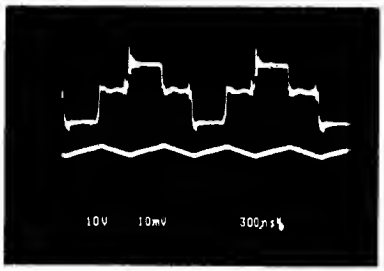
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P', 1 v/cm

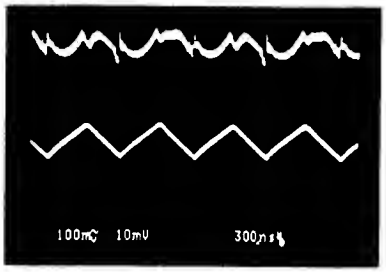
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T', 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W', 100 mv/cm

Bottom Trace
AC Output Current
J2, 2 A/cm

9

PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant V_{OUT} L_{SEC}.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current I1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

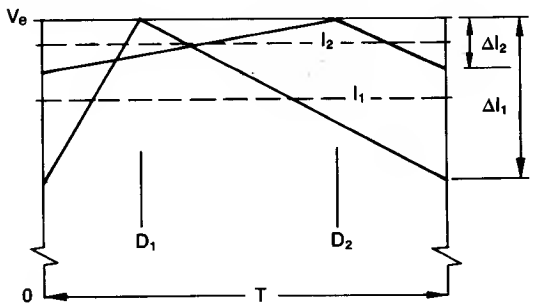


Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

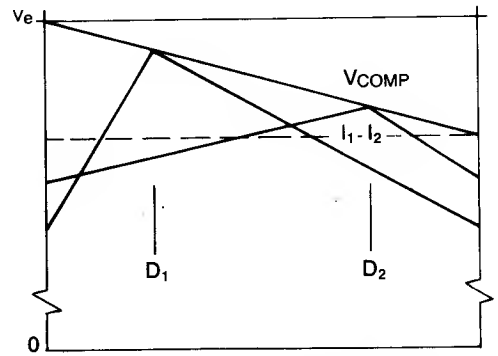


Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator
	ΔV Oscillator (PK-PK Ramp Amplitude)
	I Sense Threshold (Max)
Output	V Secondary (Min)
	L Output
	I AC Secondary (Secondary Ripple Current)
General	R Sense (Current Sensing Resistor)
	M (Amount of Slope Compensation)
	N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

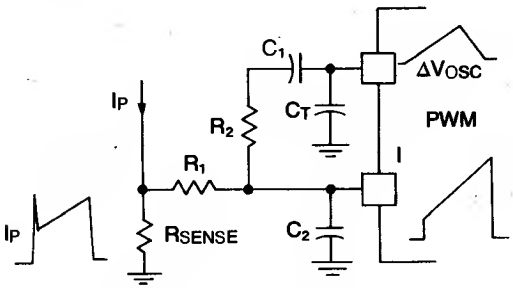


Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

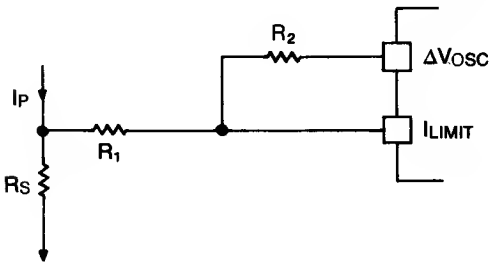


Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d\,(V_{OSC}) / T\ on$ (Volts/Second)

Step 5. Generate the Ramp Equations
Using superposition, the circuit can be illustrated as:

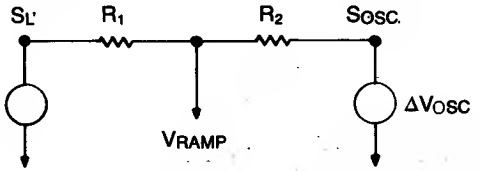


Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$ simplifying,

$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)}$ where

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$, and $$V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation
$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

Equating $$\frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

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Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of downslope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

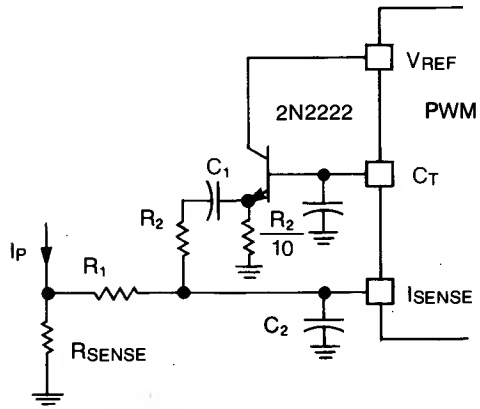


Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 μS
T Deadtime: 500 ns, T on Max = 4.5 μS
Turns Ratio: 15 / 1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<10% I DC)
L Output: 5.16 μh

1. Calculate the Inductor Downslope on the Secondary Side

$S(L) = di/dt = V_{SEC}/L_{SEC} = 6\ v/5.16\ \mu h = 1.16\ A/\mu s$

2. Calculate the Transformed Inductor Slope to the Primary Side

$S(L)' = S(L) \bullet Ns/Np = 1.16 \bullet 1/15 = 0.0775\ A/\mu S$

3. Calculate the Transformed Slope Voltage at Sense Resistor

$V\,S(L)' = S(L)' \bullet Rsense = 7.72 \bullet 10^{-2} \bullet 0.250 = 1.94 \bullet 10^{-2}\ V/\mu S$

4. Calculate the Oscillator Slope at the Timing Capacitor

$S_{(OSC)} = d\,V\ osc/T\ on\ max = 1.8/4.5 = 0.400\ V/\mu S$

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}\ ;\ R2 = \frac{1K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

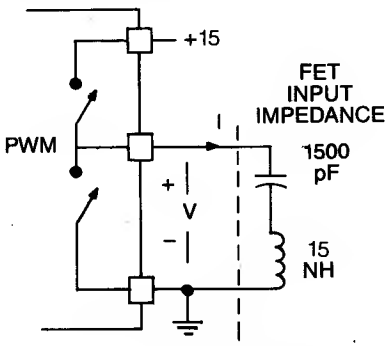


Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

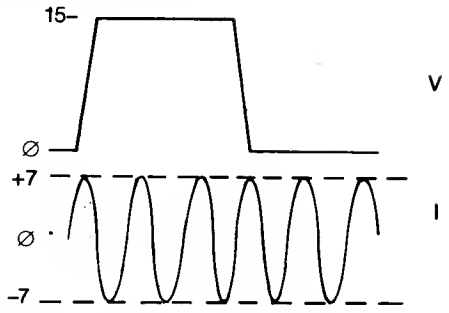


Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (V_C) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

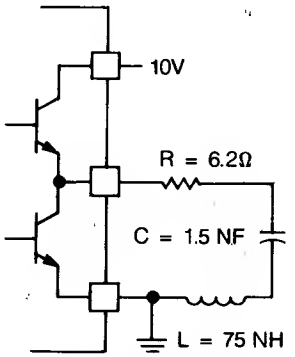


Figure 9. Circuit Parameters

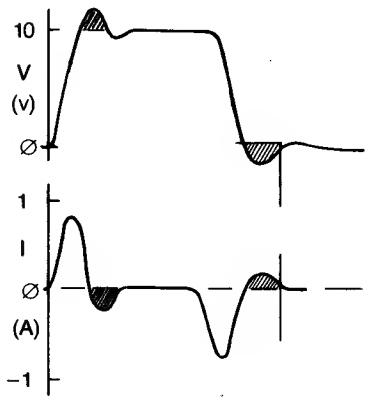


Figure 10. Circuit Response

The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

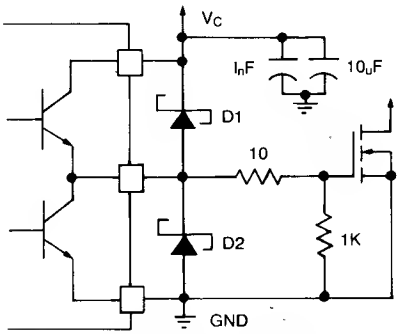
$$R(\text{gate}) \geq 2 \bullet \sqrt{L/C}$$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS — highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

9

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure xx when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

Power MOSFET Drive Circuit

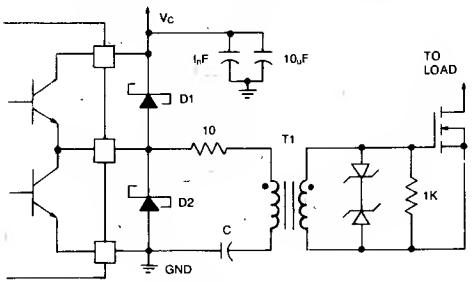


D1,D2: UC3611 Schottky Diodes

Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Transformer Coupled MOSFET Drive Circuit



D1,D2: UC3611 Schottky Diode Array

Figure 12.

Transformer Coupled Push-Pull MOSFET Drive Circuit

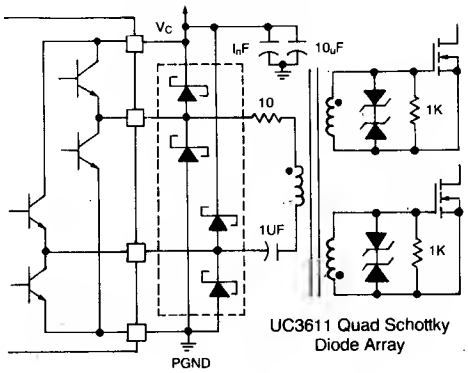


Figure 13.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm}\right] + [Crss(VDD - Vgth)]\right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{(10 \bullet Ciss) + (Crss \bullet V\,drain)\}$$

$$Ton = \frac{2}{I\,pk} \bullet \{(10 \bullet Ciss) + (Crss \bullet Vdrain)\}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1.0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET, high speed applications.

SEE APPLICATION NOTE U-118

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resultng in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator. Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

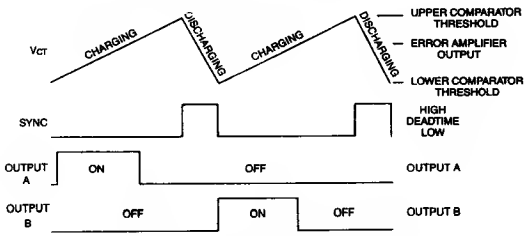


Figure 14. Voltage Mode Control – Normal Operation

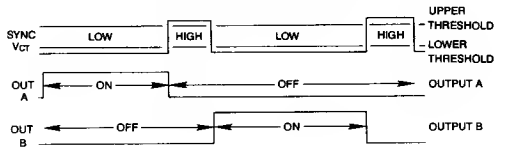


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocesso software controlled routine.

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Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator. In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

— Sync any PWM to/from any other PWM
— Sync any PWM to/from any number of other PWMs
— Sync from digital levels for simple system integration
— Bidirectional sync signal
— Any PWM can be master or slave with no modifications
— Each control circuit will start and run independently of sync if sync signal is not present
— Localized ramp at Ct for slope compensation
— No critical frequency settings on each module
— High speed — minimum delays
— High noise immunity
— Low power requirements
— Remote off capability
— Minimal effect on frequency, duty cycle, and dead time
— Low cost and component count
— Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

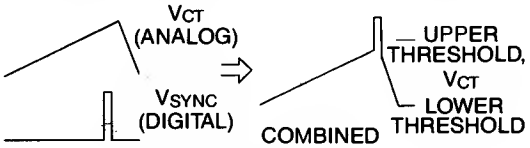

Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor. Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

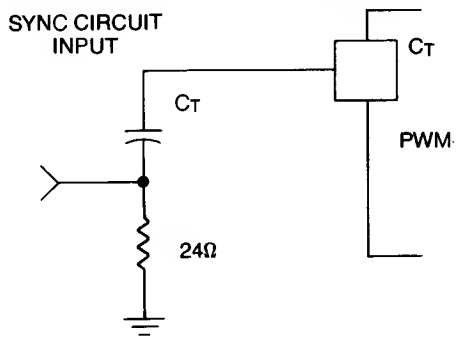

Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail.)

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

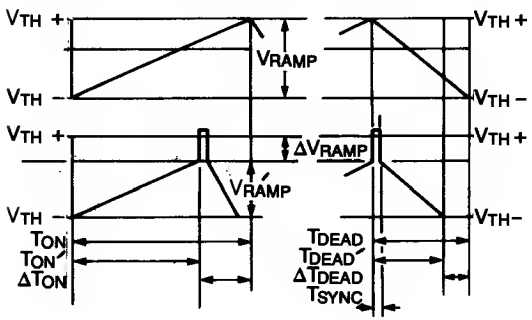

Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\,osc = \frac{1}{Ct}\left[\int I\,chg\,dT = \frac{I\,chg}{Ct}\right]_0^t T$$

$$T\,chg = \{\Delta V\,osc \bullet Ct\} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\,osc = Vth\ upper - Vth\ lower$$

$$\Delta V\,osc' = \Delta V\,osc \frac{(tchg')}{t\,chg(o)} - V\,(24\ ohm)$$

$$V\,(24\ ohm) = I\,chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator. Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\,chg'}{T\,chg(o)} = \frac{T\,sync}{T\,orig} = \frac{F\,orig}{F\,sync} = P \text{ "relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\,(sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\,orig.$$

$$T\,chg' = T\,chg(o) \bullet P = 0.85\ T\,chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta[Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\,[Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) – ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\,dschg' = [\Delta Vdchg(o) \bullet P] - V\,(24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\,dchg' = T\,dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\,dchg(o) \bullet [\Delta V\,dchg' / \Delta Vosc(o)]$$

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The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

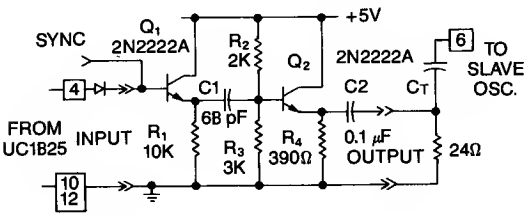

Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor C1, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master. This high speed pulse amplifier circuit adds a minimum of delay (≈50 ns) between the master to slave timing relationship.

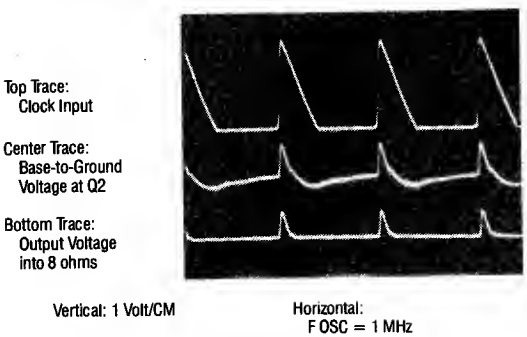

Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.

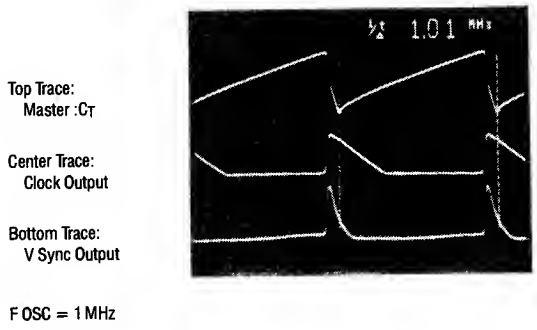

Figure 21. Circuit Timing Waveforms

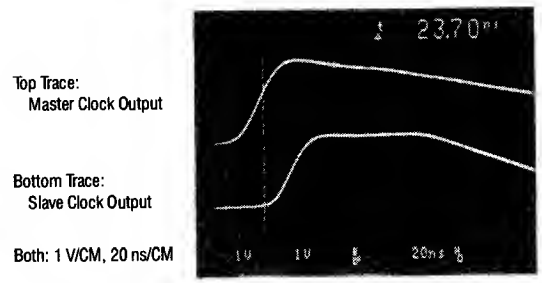

Figure 22. Sync Circuit Delay; input to Output

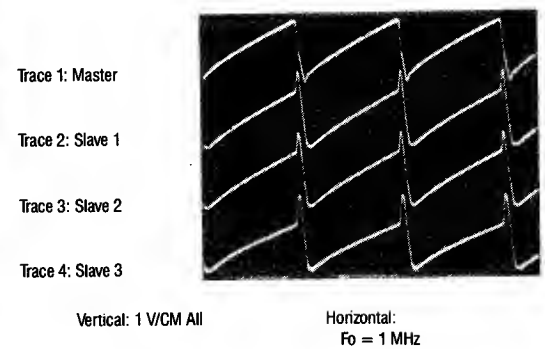

Figure 23. Oscillator Waveforms: Master and Slaves

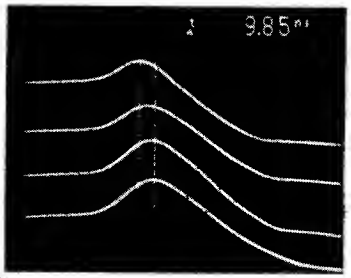

Figure 24. Typical Sync Delay at C_T Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator. In this instance, the sync pulse forces synchronization at alternate cycles to the master.

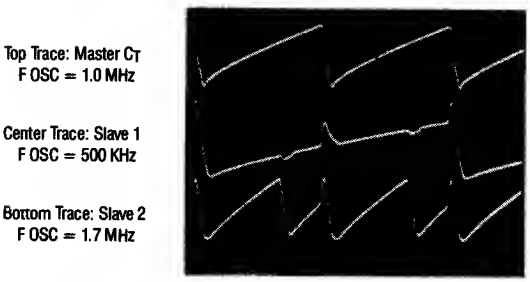

Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

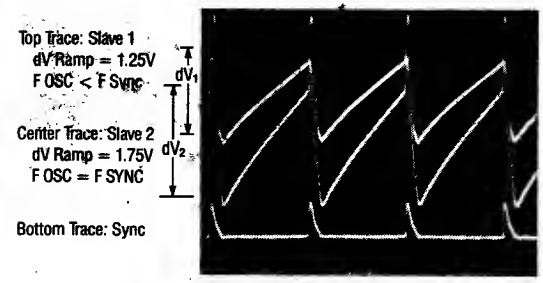

Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

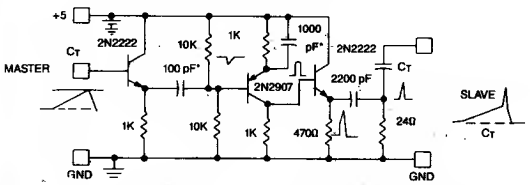

Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit. the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

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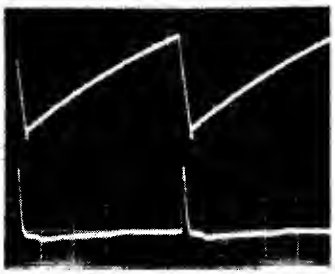


Figure 28. Operating Waveforms at 500 KHz

Figure 29. Master/Slave Sync Waveforms at C_T

IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full-functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.

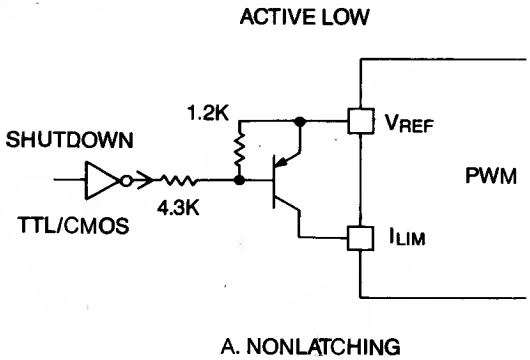


Figure 30. PWM Shutdown Circuits

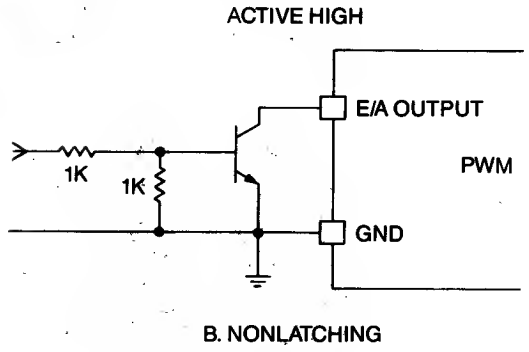
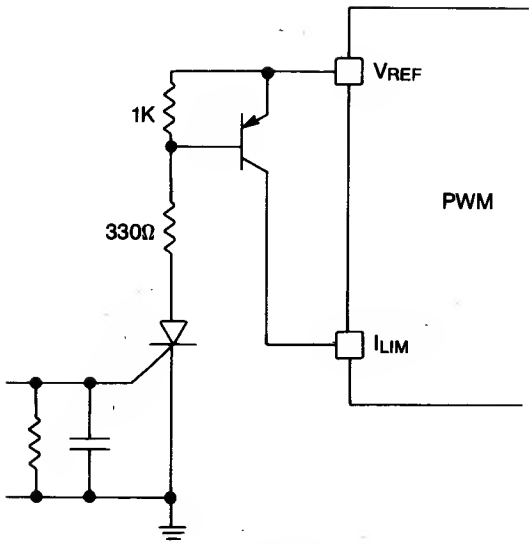


Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

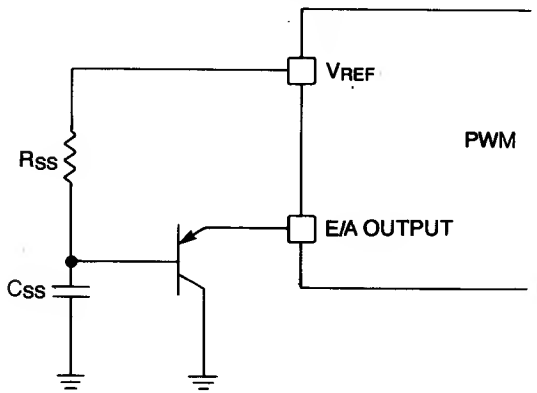


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror. The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

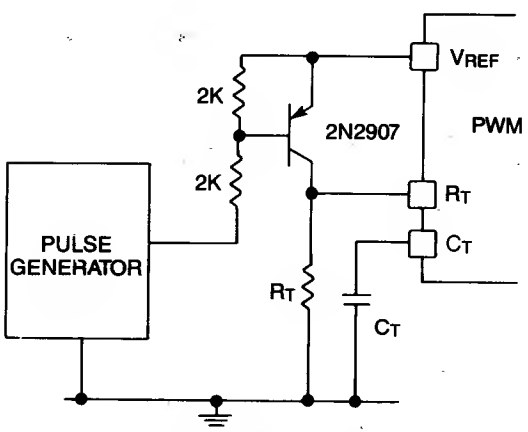


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

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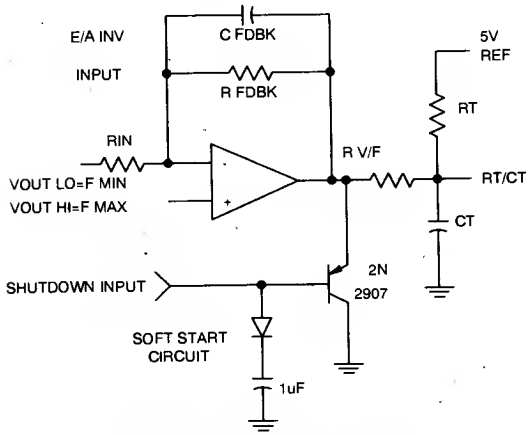
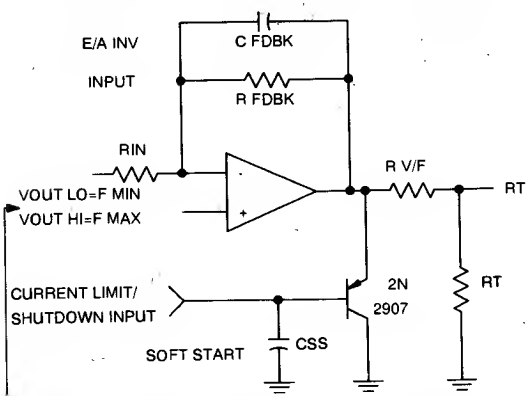
VOLTAGE CONTROLLED OSCILLATOR GENERAL CONFIGURATION

VARIABLE FREQUENCY OPERATION FIXED 50% DUTY CYCLE OSCILLATORS WITH SINGLE PIN PROGRAMMING



UC3851 / UC3844A / UC3845A
*GROUND RAMP OR CURRENT SENSE INPUT

OSCILLATORS WITH SEPARATE RT & CT PINS



UC3823 / UC3825 / UC3846 / UC3847
*GROUND RAMP OR CURRENT SENSE INPUT
USE NONINV E/A INPUT FOR REVERSE V/F OPERATION

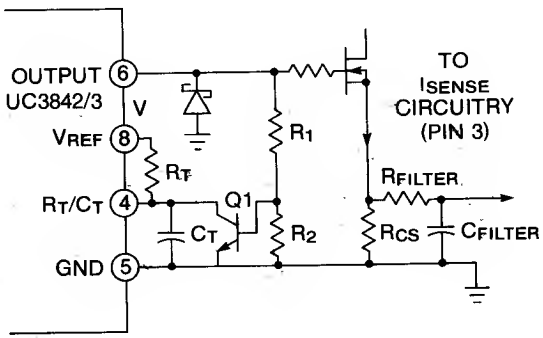
Fixed "Off-Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

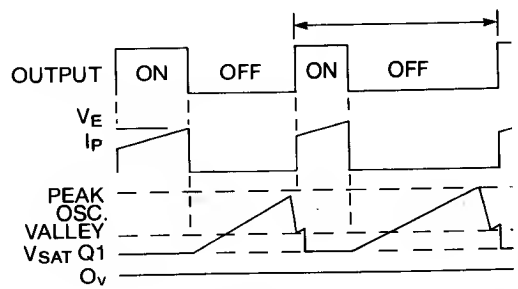
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold. The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

Current Mode ICs Used In Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

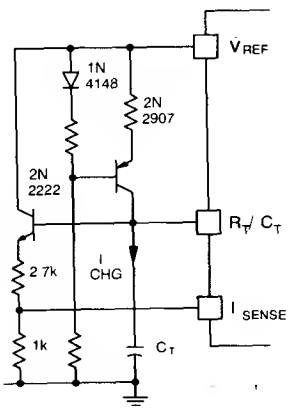


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

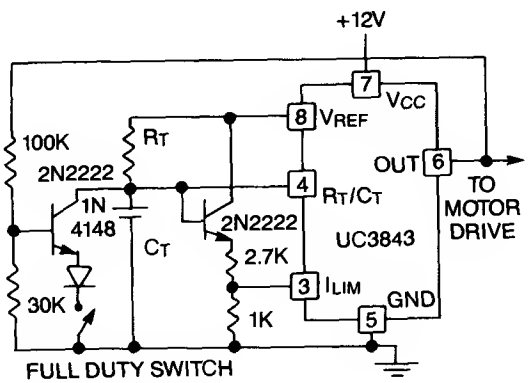


Figure 37. Full Duty Cycle Implementation

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VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (<35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

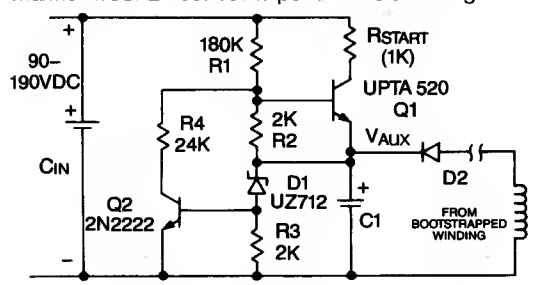

Figure 38. NPN Switches

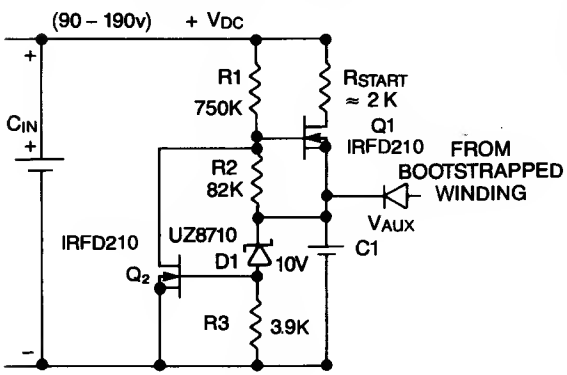

Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor C1 is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to C1 from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and C1 is charged through R start-up from the high voltage DC, as during start-up.

NOTE: SEE DESIGN NOTE DN-26 FOR ADDITIONAL CIRCUITS.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

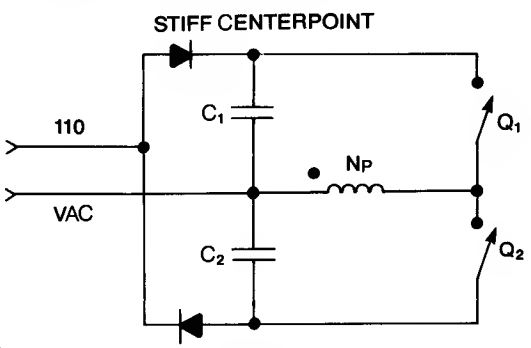

Figure 40.

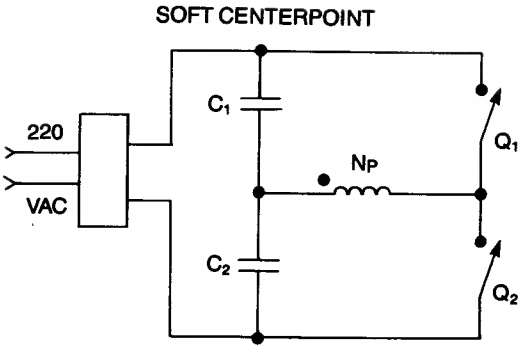

Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

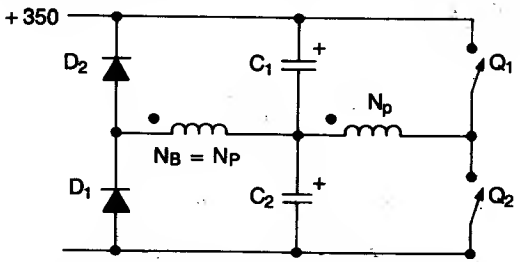

Figure 42. Schematic – Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

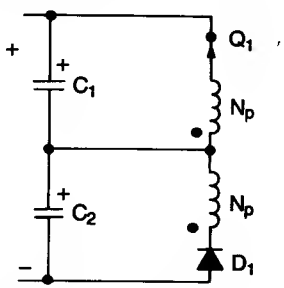

Figure 43. Transistor Q1 On

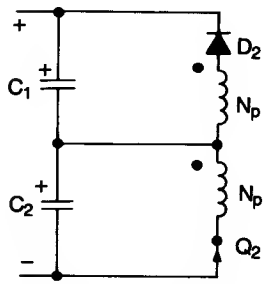

Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

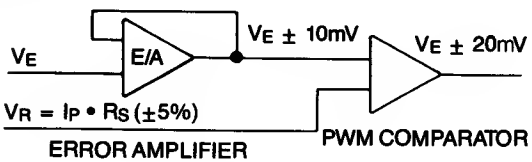

Figure 45. PWM Diagram

In reality, small offets of ±10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ±20 millivolt offset represents a ±2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ±20 millivolts introduces only ±0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ±5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (±2%) / Rs (±5%); therefore Ip' = Ip (±7%) The primary currents (hence output currents) will share within ±seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

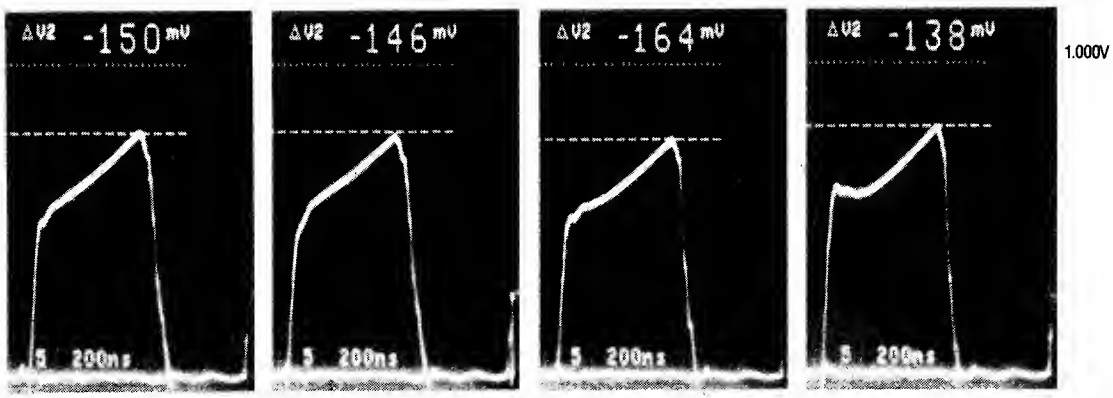

Figure 46. Primary Currents – Parallel Operation

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor. These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

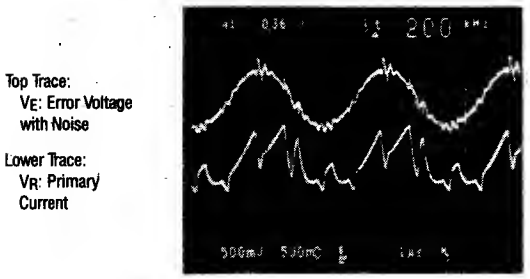

Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter.

Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

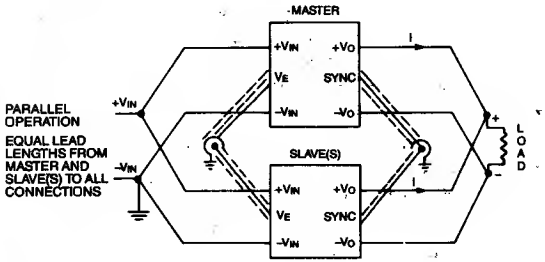

Figure 48.

9

A HIGH PRECISION PWM TRANSCONDUCTANCE AMPLIFIER FOR MICROSTEPPING USING UNITRODE'S UC3637

INTRODUCTION

If you ask a designer why he has chosen a stepping motor for a given application, chances are that his answer will include something about "open loop positioning." Stepping motors can provide accurate positioning without expensive position sensors and feedback loops, and this fact alone results in large savings.

But there is more: steppers are tough and durable, easy to use, and high in power rate. And if you want to close a feedback loop around them, you can do that, too.

Still, there are certain problems. Steppers are *incremental motion* machines, and as such they tend to be noisy and are prone to behave erratically under certain conditions; for example, when the stepping rate is such as to excite a mechnical or electro-mechanical resonant mode. Furthermore, although the angular increments may be small—especially when half-stepping is used—the positioning resolution is restricted to a finite number of discrete points.

Therefore, this question arises: "Is there a method of driving stepping motors such that the resulting movement is smooth and quiet—that is, essentially continuous, as opposed to incremental? And would this result in improved positioning resolution?" We will try to answer these questions here.

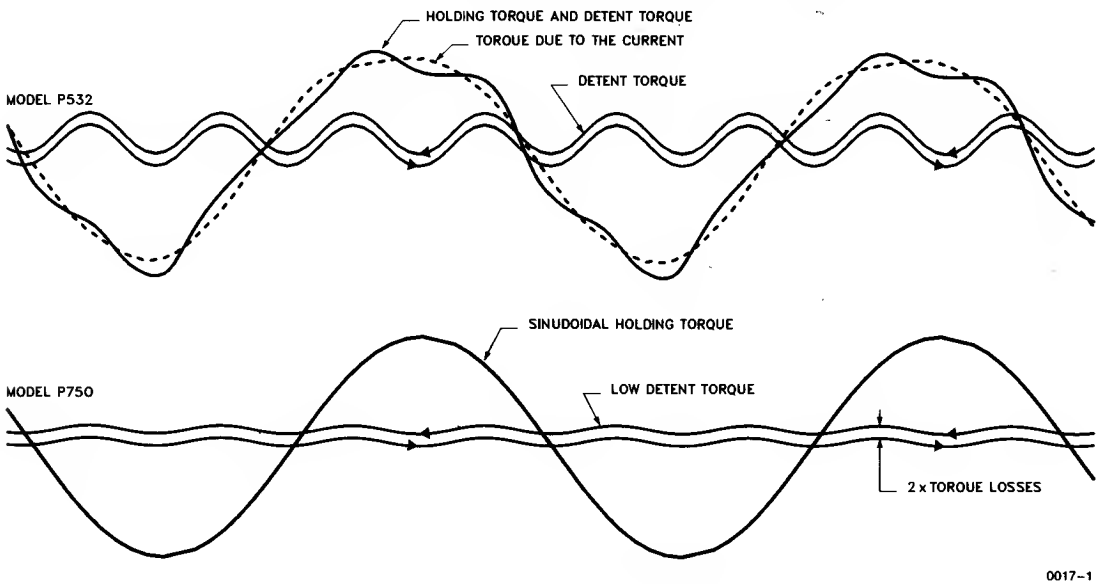

Figure 1. Static Torque Curves of Two Hybird Steppers

STATIC TORQUE CURVES

The curves in Figure 1 illustrate how a stepping motor torque behaves as a function of rotor angle. The detent torque component is a consequence of the magnetic field produced by the rotor magnet (or magnets), and is present with or without phase currents applied. It can be seen that this component contributes a fourth harmonic distortion to the static torque curves. The energized torque curves, in general, have additional harmonic components, mostly the third and fifth. Note that the two motors depicted in Figure 1 have very different characteristics in this respect. The distortion observed in the static torque characteristic is of no great consequence in the more usual applications of stepping motors, using either full step or half step sequences. It is when we start thinking about increasing the positioning resolution of these motors by some method of apportioning currents between the two phases, that we begin to be concerned about the effects of harmonic distortion. Even small amounts of added har-

monics can have a very noticeable effect on the waveshape, as shown in Figure 2.

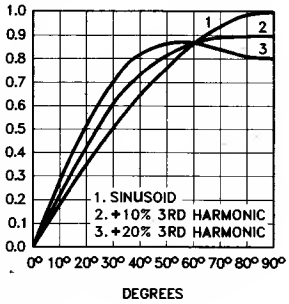

Figure 2. Effect of 10% and 20% Harmonic Content

Figure 3 shows the relationship between sine and cosine waveforms, and what it tells us is that if we can get a motor with a sinusoidal static torque characteristic—i.e., with no harmonic components—and drive phase A with a sine current function and phase B with a cosine current function, we would have smooth shaft rotation and accurate positioning at any angle.

Stepping motors having static torque curves with very low harmonic distortion are commercially available today. But most low-priced, mass produced hybrid steppers exhibit torque curves with enough harmonic components to require careful consideration in any attempt to improve resolution by what is known as *microstepping*. (The name *microstepping* originates from the fact that the required current waveforms are generated by a digital process that aproximates those waveforms incrementally. With thirty-two or sixty-four increments for an electical angle of $\pi/2$ radians, the resulting waveforms are hardly distinguishable from true sine or cosine signals.)

If the nonsinusoidal static characteristic of a given motor is known, it is possible to generate appropriate waveshapes for the phase currents so that the resulting torque curve becomes free of distortion, as required. Note that this involves no additional complexities, since it is just as easy—or difficult—to synthesize one waveform as another. Consequently, one can, in principle, linearize any motor for increased resolution and smoothness through microstepping.

Still, it should be noted that the best efficiency is obtained when the phase current waveshapes are undistorted, because of all suitable waveforms, the sine wave has the lowest form-factor.

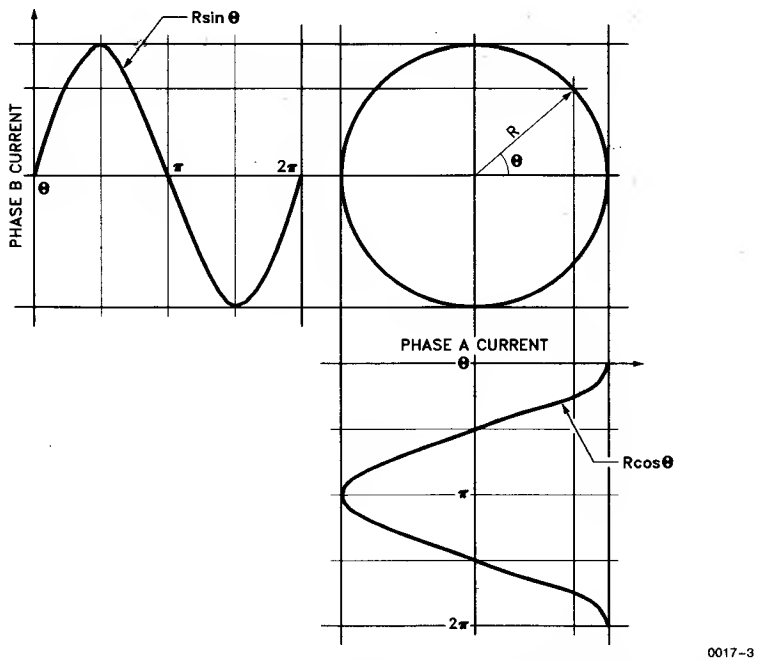

Figure 3. The sum of sine and cosine waveforms is a smoothly rotating vector.

The form-factor of a waveform is the ratio if its rms to average values. For a sine wave, this ratio is:

$$(1)\ ff_S = \frac{0.707}{0.637} = 1.111$$

Some manufacturers have used triangular waveforms—largely because they can be implemented with great simplicity—and it is interesting to note that for such a waveform, the average value is 0.5 V_{PK}, while the rms is 0.577 V_{PK}. Thus the form factor is:

$$(2)\ ff_T = \frac{0.577}{0.5} = 1.155$$

As a consequence, for the same peak power applied to the motor, the rms power of a triangular waveform is 18% less than that of a sine wave, whereas the average current is 21% less. It follows that microstepping with a triangular waveform does not use the full capabilities of the motor.

The same result is obtained with other-waveforms, as long as the peak power is limited, as it must be.

But regardless of all this, the fact remains that whether our motor has a sinusoidal torque curve or a very distorted one, the thing that will be inevitably required will be two amplifiers capable of converting the synthesized waveform into phase currents *at the required power levels*. In the next section, we will describe the design of one such amplifier, having a transconductance linearity of better than 1% and capable of delivering phase currents of up to ±6A.

UNITRODE'S UC3637 PWM CONTROLLER

Pulse width modulation (PWM) is a method of power control whose most attractive feature is the high level of efficiency that can be obtained. With careful design, and using power MOSFETs as output switches, one can easily achieve efficiencies higher than 80%.

The Unitrode UC3637 PWM controller, housed in an eighteen-pin DIL package, was originally intended to serve as a PWM amplifier for brush-type PM servomotors. But, because of its ingenious design, the device has found its way into various other uses as well, such as temperature control, uninterruptible power supplies, and even high fidelity sound reproduction. As we shall see, it can also be used in a high performance PWM transconductance amplifier.

BLOCK DIAGRAM AND LOOP EQUATIONS

A block diagram of the current feedback loop under consideration is shown in Figure 4, where the UC3637 is seen to contain the high-gain error amplifier and the main ingredients of the PWM amplifier. Since we are looking for an output of 6A, an H-bridge power stage must be added. The motor current I_M is sensed by means of a low value resistor R_S, and the derived voltage V_C is used to complete the feedback loop. Not shown in the block diagram is the back-EMF voltage, the product of motor shaft speed and K_V, the motor speed constant. Since this term does not contribute to the dynamics of the current feedback loop, it has purposely been left out.

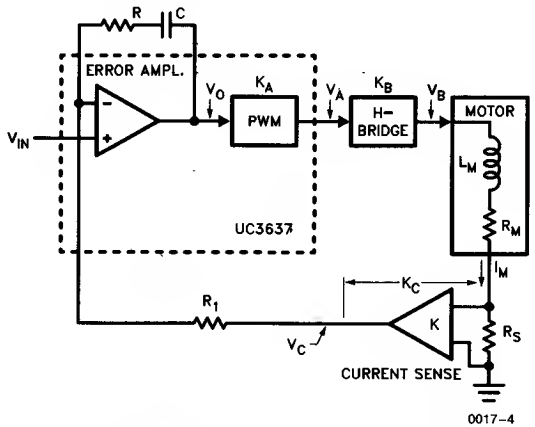

Figure 4. Block Diagram of the Complete Current-Control Loop

The transfer functions of the error amplifier and motor are as follows:

$$(3)\ \frac{V_O}{V_C} = -\frac{1 + sRC}{sR_1C}$$

$$(4)\ \frac{I_M}{V_B} = \frac{1}{R_M(1 + sTm)}$$

where $T_M = L_M/R_M$, the motor's electrical time-constant (R_S is assumed to be low compared with R_M). The forward transfer function is, then:

$$(5)\ G(s) = \frac{-K_A K_B (1 + sRC)}{sR_1R_MC(1 + sTm)}$$

For the feedback transfer functions, we have simply:

$$(6)\ H(s) = \frac{V_C}{I_M} = K_C$$

Thus, for the closed loop,

$$(7)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B (1 + sRC)}{K_A K_B K_C(1 + sRC) + sR_1R_MC(1 + sTm)}$$

If we make the time-constant RC equal to the motor's time-constant T_M, this becomes:

$$(8)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B}{K_A K_B K_C + sR_1 R_M C}$$

$$(9)\ \frac{I_M}{V_{IN}} = \frac{1}{K_C(1 + sT_1)}$$

where,

$$(10)\ T_1 = \frac{R_1 R_M C}{K_A K_B K_C} = \frac{R_1 L_M}{K_A K_B K_C R}$$

By making $RC = T_M$, we have eliminated one of the transfer function poles. The resulting closed-loop response, described by (7) has a gain of $1/K_C$ from $\omega = 0$ to $\omega = 1/T_1$, and drops at -6 bd/octave thereafter.

DESIGNING THE HARDWARE

In designing circuits intended to handle power, it is customary to start with the output stage. This is surely due to the fact that the power stage is more demanding of the designer's attention and care, whereas the low level circuits are far more adaptable to the requirements of the chosen output configuration.

In the present case, power MOSFETs were chosen for the H-bridge because of their low losses, and because of their compatibility with the UC3637 outputs. Each totem-pole leg of the bridge is made up of one N-channel and one P-channel device. Such a pair can be driven in many different ways, of which several were considered for this particular design. The method that was finally chosen, shown in Figure 5, requires a few comments.

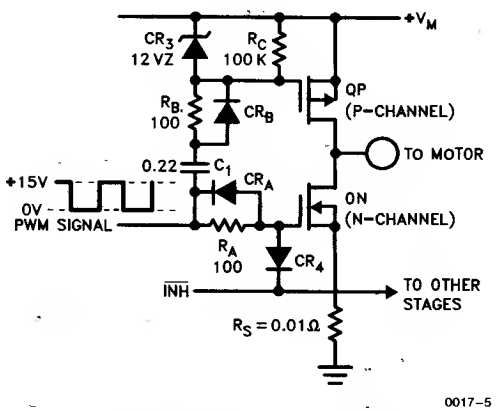

Figure 5. Totem-Pole Leg of Output H-Bridge

The first thing to notice is that the upper MOSFET, transistor QP, has its gate driven through a capacitor, C_1. This is not always practical of course, but in the case of a chopper drive combined with a stepping motor, it turns out that a driving signal is always present. At stand-still and at low speeds, it is the chopping rate that appears; at higher speeds, it is the stepping rate itself, or both. The driver is never required to deliver continuous DC (unchopped) to the motor winding, as it would to the armature of a brush-type DC motor at full speed. Consequently, QP never needs to be held in the ON state for more than a few microseconds, and for this the time constant of C1 R4 is adequate. Also, resistor R_A in parallel with CR_1, together with the gate capacitance of QN, cause this transistor to turn off faster than it turns ON. Since the same thing is done for QP, the problem of cross-conduction is neatly taken care of. The Zener diode CR3 serves as a clamp for the QP gate voltage. Finally, an inhibiting line, INH, is provided as a protection for QP and QN during the power turn-on time, when the $+V_M$ voltage is rising and C1 must be charged. An auxiliary circuit senses a positive dV_M/dt and holds the INH line low, thus keeping QN OFF during this time.

An important point in favor of this arrangement is that the gate-drive circuit losses are independent of V_M and so this voltage can be set anywhere within the Vds rating of the power MOSFETs.

We can now consider the H-bridge with its motor winding load, as shown in Figure 6. The bridge is shown schematically with its driving circuits, but the action is still as shown in Figure 5. For example, when V_{IN} is high, switch S1 is OFF and S3 is ON, and so forth. Furthermore, the opposite side of the bridge is driven by the complementary signal V_{IN}. With V_{IN} low, S1 and S4 will be conducting, and the load current I_M will increase in the positive direction (indicated by the $+I_M$ arrow). Similarly, when V_{IN} is high, both S2 and S3 conduct, causing I_M to increase in the negative direction. Remember that the load is inductive, and that inductance is an energy storing element. Therefore, if we have some positive I_M, due to S1 and S4 being closed, and we switch to S2 and S3 closed, the previous value of I_M will continue to flow "uphill," so to speak, while decreasing. At the time of switching, this current ceases to flow down through sense resistor R_{S4} to ground and starts flowing up through R_{S3} and back to the supply.

Switches S1 through S4 are able to conduct in either direction when in the ON state—a very neat feature of power MOSFETs. Furthermore, their intrinsic diode protects the devices from reverse voltage pulses during the switching no-overlap transition. Since we wish to control this current very closely in both magnitude and direction, it is

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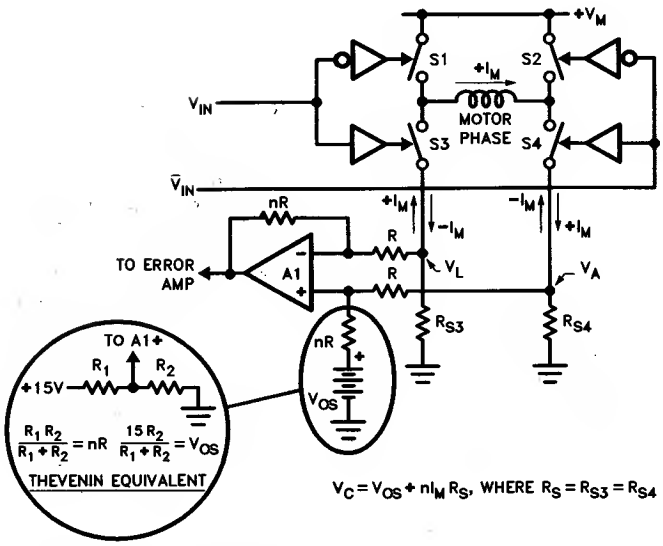


Figure 6. H-Bridge Configuration with Bidirectional Current Sensing

now necessary to generate a voltage V_C that gives an accurate indication of the current I_M over the full range from maximum positive to maximum negative. This is done by the circuit section of Figure 6 which includes the op-amp A1.

In that circuit, the voltage V_{OS} is meant to offset the output V_C of A1 to some chosen value that will correspond to $I_M = 0$. The value of V_C can be written as:

(11) $V_C = V_{CS} + nI_MR_S$

This offset is necessary when the design requires a single polarity supply, as in our case. When two supply polarities are available for the control circuit, one can simply make $V_{OS} = 0$. For the single supply case, the nR and V_{OS} combination is implemented by a simple resistor divider from $\pm V_{CC}$ to ground (a Thevenin equivalent) of the required impedance and open voltage.

To keep the circuit losses to a minimum, we should use low values for the sense resistors R_{S3} and R_{S4}. Yet, they need to be accurate and temperature-stable. In our case, having decided on a V_C scale of 0.5V per motor ampere, we have selected $R_S = 0.1\Omega$ and a current sense amplifier gain n = 5. We have also set $V_{OS} = V_{CC}/2 = 7.5V$, so that we will have $V_C = 7.5 + 0.5\ I_M$. This means that as the current I_M varies from +6A to −6A, the analog voltage V_C will vary from +10.5V to +4.5V. At $I_M = 0$, V_C will be equal to 7.5V.

SETTING UP THE PWM CONTROLLER

Having designed the power output stage (H-bridge) and the current-sense circuit, we can proceed to the PWM controller (UC3637) and its external components. The device itself has been described in great detail in its data sheet and in an application note (Publication U-102, available from Unitrode Integrated Circuits Corporation).

In the present design, we use the UC3637 to generate the two H-bridge driving signals V_{IN} and $\overline{V_{IN}}$, at the device's output pins 7 and 4, respectively.

Figure 7 shows in block form the internal workings of the device. Since operation from a single +15V supply is desired, pin 5 will be GROUND and pin 6 will be +15V. We selected, for the ramp oscillator, a waveform as shown in Figure 8, which fits well in the +15V headroom given by our V_{CC} supply. The formulas given in Figure 8 show how the various components are calculated.

Next, we set up the two PWM comparators by tying the inverting inputs (pin 10) of the A comparator, and the noninverting input (pin 8) of the B comparator together and apply the ramp (pin 2) to this line. The remaining comparator inputs (pins 9 and 11) are next connected together to become the PWM input point. It can be seen from the block diagram of Figure 7 that as the control voltage applied to this point varies from +5V to +10V, the duty cycle of the output at pins 4 and 7 also varies. V_4 and V_7 are complementary signals; and the voltage swing of each of these signals is from a low value between 0V and +2V, and a high value between (V_{CC} −2V) and V_{CC}.

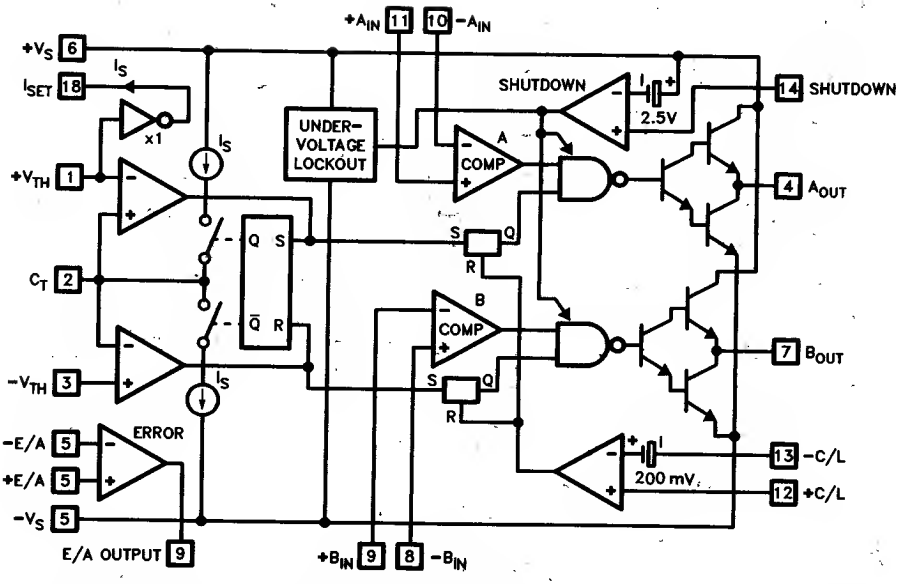
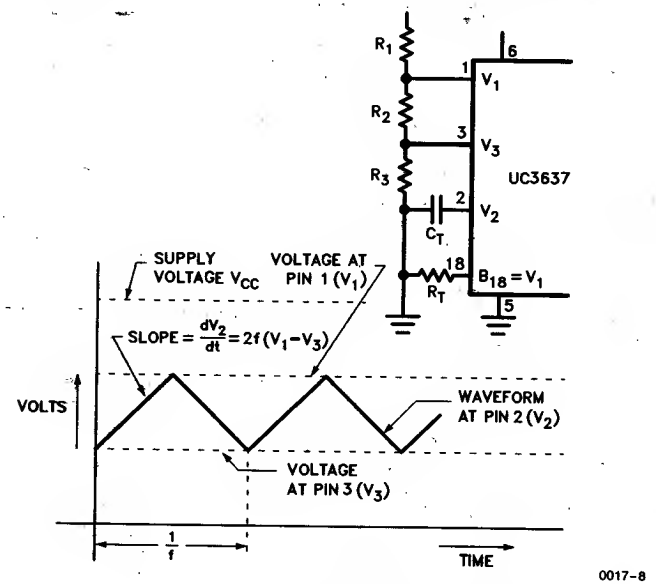


Figure 7. Block Diagram of the UC3637. The two outputs can drive power MOSFETs directly.



f = ramp frequency

$I_T = \frac{V_{18}}{R_T} = \frac{V_1}{R_T}$ (should be about 0.5 mA)

then, $R_T = 2000\ V_1\ (\Omega)$

$C_T = \frac{250 \times 10^{-8}}{f(V_1 - V_3)}(fd)$

Figure 8. Setting up the ramp oscillator requires only five external components.

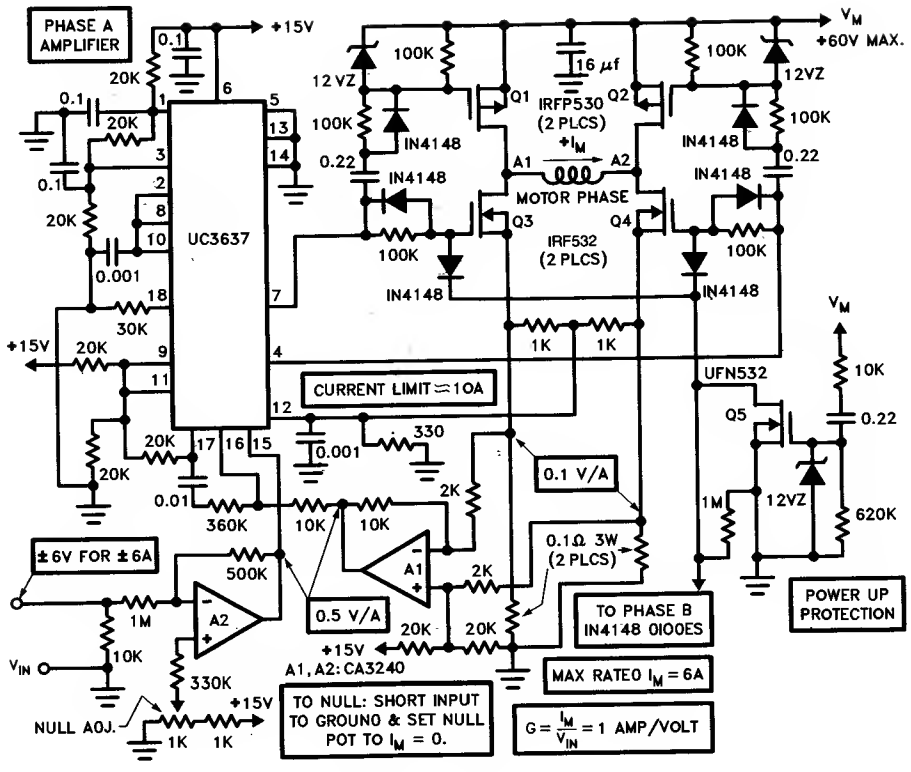


Figure 9. PWM Transconductance Amplifier UC3637

The error amplifier is used as a source for the control signal. But because its output (pin 17) has a voltage range greater than the +5V to +10V range of the V_C ramp signal, and we want to prevent the modulation range from ever reaching 0% or 100% (because of the capacitively coupled P-channel MOSFET devices) we add a simple resistive network consisting of three equal resistors to serve as an attenuator. The final result can be seen in the complete schematic of Figure 9.

CURRENT LIMIT AND CONTROL

The current limit feature of the UC3637 is used to protect the output transistors and motor from excessive current (6A in this case). As the block diagram of Figure 7 shows, the current limit comparator (pins 12 and 13) of the UC3637 is internally biased to a threshold of 200 mV. The network that connects the two sense resistors to pin 12, consisting of two 1K and one 330Ω resistors, causes a voltage of 200 mV to appear at pin 12 when the voltage at either sense resistor is about 1V, corresponding to a current of 10A. Consequently, the maximum output current will be limited to 10A. The current feedback loop is closed by feeding the output of the current sense amplifier to pin 16, the inverting input of the error amplifier of the UC3637. An RC time constant of 3.6 msec is used for the zero in this amplifier's transfer function (equations 8, 9, and 10) which is close to the effective electrical time constant of the motor. Also, a level-shift circuit is provided by means of op amp A2 to permit the use of a control input centered at zero volts, and a control range from −6A to +6A. The circuit allows this even though the op amp is powered by a single positive supply.

TEST RESULTS

The design circuit, shown in Figure 9, was breadboarded for testing at Unitrode and also at Portescap. The assembly includes two amplifiers, one for each motor phase and a "power on" auxiliary circuit for protection of the power MOSFETs. The output devices are equipped with small sheet metal heat sinks.

The circuit draws about 65 mA from the +15V supply. The power output section operates with a supply ranging from +20V to +60V, with no damage occurring if this voltage is lower than +20V.

The circuit performed very well, with excellent linearity and phase matching. The various plots taken, showing output current versus input voltage, are quite straight, and the transconductance is accurate to within 1%. Furthermore, the PWM frequency was subsequently increased to slightly above 100 KHz (by reducing C_T) and the performance re-checked. The result was a marked increase in motor efficiency, due to reduced current ripple, with all other results remaining excellent.

CONCLUSION

Microstepping is a technique of considerable interest in the design of many products, particularly those in which the lower cost of open-loop positioning is an essential parameter. A motor such as Portescap's Model P-750, with its accurately sinusoidal torque curve, becomes even more attractive once its microstepping driver is shown to be fairly simple and inexpensive. The end result is not only precise open loop positioning, but quiet operation, freedom from resonance problems, and excellent electrical efficiency. Incidentally, the motor is available with two quadrature speed sensing coils that can be used for speed and position control, if desired.

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DESIGN NOTES ON PRECISION PHASE LOCKED SPEED CONTROL FOR DC MOTORS

ABSTRACT

There are a number of high volume applications for DC motors that require precision control of the motor's speed. Phase locked loop techniques are well suited to provide this control by phase locking the motor to a stable and accurate reference frequency. In this paper, the small signal characteristics, and several large signal effects, of these loops are considered. Models are given for the loop with design equations for determining loop bandwidth and stability. Both voltage and current motor drive schemes are addressed. The design of a loop for a three phase brushless motor is presented.

PHASE LOCKING GIVES PRECISION SPEED CONTROL

The precise control of motor speed is a critical function in today's disc drives. Other data storage equipment, including 9 track tape drives, precision recording equipment, and optical disc systems also require motor speed control. As the storage density requirements increase for these media, so does the precision required in controlling the speed of the media past the read/write mechanism. One of the best methods for achieving speed control of a motor is to employ a phase locked loop.

With a phase locked loop, a motor's speed is controlled by forcing it to track a reference frequency. The reference input to the phase locked loop can be derived from a precision crystal controlled source, or any frequency source with the required stability and accuracy. A block diagram of the phase locked loop is shown in Figure 1.

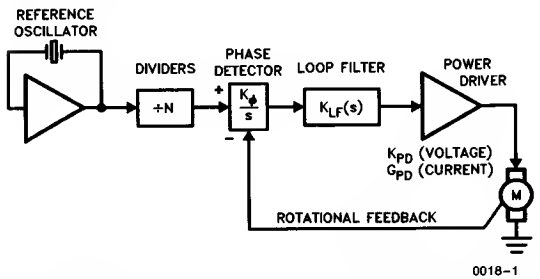


Figure 1. Precise motor speed control is obtained by phase locking the motor to a precision reference frequency.

In Figure 1, a precision crystal oscillator's frequency is digitally divided down to provide a fixed reference frequency. Alternatively, the motor could be forced to track a variable frequency source with zero frequency error. The motor speed is sensed by either a separate speed winding or, particularly in the case of the DC brushless motor, a Hall effect device. The two signals, motor speed and reference frequency, are inputs to a phase detector. The detector output is a voltage signal that is a function of the phase error between the two inputs. The transfer function of the phase detector, K_ϕ, is expressed in volts/radian. A 1/s multiplier accounts for the conversion of frequency to phase, since phase is the time integral of frequency.

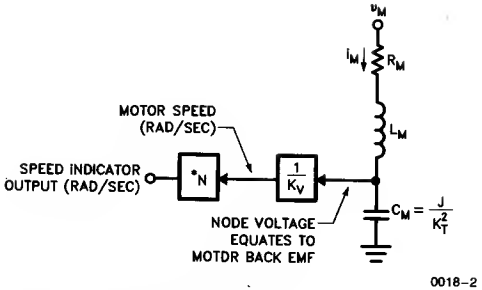
Following the phase detector is the loop filter. This block contains the required gain and filtering to set the loop's overall bandwidth and meet the necessary stability criteria. The output of the loop filter is the control input to the motor drive. Depending on the type of drive used, voltage or current, the driver will have respectively, a V_{OUT}/V_{IN} transfer characteristic, or an I_{OUT}/V_{IN} transconductance.

At first glance, it seems that the motor has simply replaced the V_{CO} (voltage controlled oscillator), in the classic phase locked loop. In fact, it is a little more complicated. The mechanical and electrical time constants of the motor come into play, making the transfer function of the motor more than just a voltage-in, frequency-out block. In order to analyze the loop's small and large signal behavior it is essential to have an equivalent electrical model for the motor.

A SIMPLE ELECTRICAL MODEL FOR A DC MOTOR

Figure 2 is an electrical representation of a DC motor. The terms used are defined here:

- L_M Motor winding inductance in henrys
- R_M Motor winding resistance in Ωs
- J Total moment of inertia of the motor in Nm-sec^2 (**Note:** 1 Nm = 141.6 oz-in)
- K_T Motor torque constant in Nm/Amp
- K_V Voltage constant (back EMF) of motor in volt-sec/rad (**Note:** $K_V = K_T$ in SI units)



*N = Number of speed sense cycles per motor revolution

Figure 2. This aimple electrical model is useful for determining the small and large signal characteristics of the motor. Capacitor, C_M is used to model the mechanical energy atorage of the motor.

In this model the winding inductance and resistance elements correlate directly with the corresponding physical parameters of the motor, with values taken directly off the manufacturer's data sheet. The capacitor, C_M, models the mechanical energy storage of the motor. Current into the capacitor equates, via motor constant K_T, to motor torque, and the voltage across the capacitor is equal to the motor back EMF. The back EMF voltage equates to motor velocity through the inverse of K_V. In the model, the term N is simply a multiplier equal to the number of feedback cycles obtained per revolution of the motor. For example, in a 4 pole brushless DC motor the commutation Hall effect device outputs will be at twice the rotational frequency of the motor, making N equal to 2.

The equation for the capacitor, given in Figure 2, has the units of Farads if J and K_T are expressed in SI units. In modeling the overall transfer characteristic, it is important that the moment of inertia of the load on the motor be added to the moment of inertia of the motor itself.

It is worthwhile to note that the current into the motor, minus idling current, is proportional to acceleration of the motor. This is easily seen from the model by realizing that the time derivative of the capacitor voltage relates directly to acceleration. The effects of loads on the motor can be modeled by including a current source across the capacitor for constant torque loads, or a resistor for loads that are linearly proportional to motor speed.

TRANSFER FUNCTIONS FOR VOLTAGE AND CURRENT DRIVEN MOTORS

Using the electrical model, the small signal transfer function of the motor is easily derived. Equations 1a and 1b give the small signal frequency response for both the current and voltage driven cases respectively.

$$1a)\quad \frac{N \times \omega_M(s)}{i_M(s)} = \frac{N}{K_V} \times \frac{1}{sC_M}$$

$$1b)\quad \frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{1 + sC_MR_M + s^2 L_MC_M}$$

The transfer function given in equation (1a) describes the small signal response of motor speed, $\omega_M(s)$, to changes in the drive current. Equation (1b) relates the dependence of motor speed to motor drive voltage.

The small signal response of the motor for the current driven case has a DC pole that results from the relationship of motor torque to velocity, that is, motor velocity is proportional to the integral of motor torque over time. In the current driven motor neither the winding resistance nor inductance appear in the transfer function. This is because these elements are in series with the current source output of the driver stage. As long as the output impedance of the driver remains large relative to the impedance of these elements, the resistance and inductance of the motor will have a negligible effect on the small signal response.

The voltage driven response has a second order characteristic that results from the interaction of the series RLC. In many cases the transfer function of the voltage driven case can be simplified. If the quality factor of the series RLC of the motor model is much less than one, as defined in equation 2, then the response of the motor can be accurately approximated by equation 3.

$$2)\quad Q_M = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} = \frac{K_T}{R_M}\sqrt{\frac{L_M}{J}}$$

$$\therefore Q_M \ll 1 \quad \text{If } R_M \gg K_T\sqrt{\frac{L_M}{J}}$$

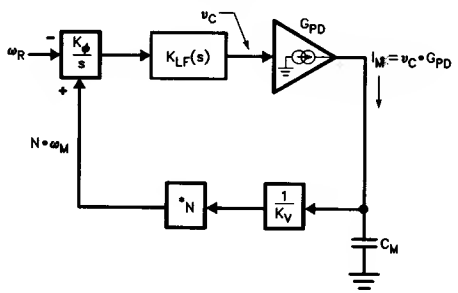
$$3)\quad \text{For } Q_M \ll 1$$

$$\frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{(1 + sC_MR_M)(1 + sL_M/R_M)}$$

CONSIDERING THE WHOLE LOOP

Figure 3 shows the complete speed control loop for the current driven case. The overall open loop response, A_{OLC}, is easily written.

$$4)\quad A_{OLC}(s) = \frac{K_\phi \times K_{LF}(s) \times G_{PD} \times N}{s^2C_M \times K_V}$$



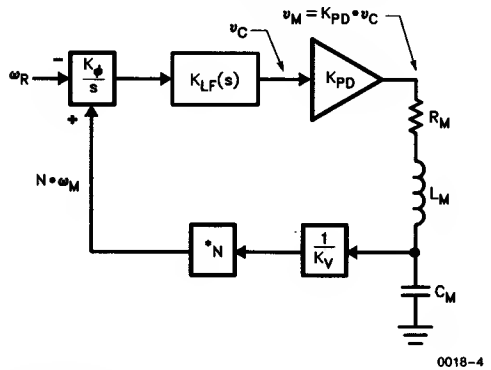
*N = Number of feedback cycles per motor revolution

Figure 3. In this phase locked loop, with current mode drive to the motor, the motor winding realatance and inductance csn be ignored aa long aa the current driver maintains a high output impedance.

For this loop, note that there are two poles in the response at DC, i.e., s = 0. One pole is due to the response of the current driven motor, the second pole is from the frequency to phase transformation of the phase detector. The 180 degrees of phase shift this pair of poles introduce force a phase lead configuration of the loop filter in order to obtain a loop phase margin greater than zero.

The complete voltage loop is shown in Figure 4, and its open loop response, $A_{OLV}(s)$, in equation 5.

$$5)\quad A_{OLV}(s) = \frac{K_\phi \times K_F(s) \times K_{PD} \times N}{sK_V \times (1 + sC_MR_M + s^2 L_MC_M)}$$



*N = Number of feedback cycles per motor revolution

Figure 4. With voltage mode drive to the motor the electrical time constant of the motor plays e part in the small signal response of the speed control loop.

This response has only one pole at DC, although the total number of poles is three versus two for the current driven case. For most motors, particularly those used in constant velocity applications, this transfer function can be simplified by applying the results of equations 2 and 3. This is best illustrated by looking at an example. Consider the following motor, (typical 3-phase brushless for disc drive applications):

K_T ..... 1.5×10^{-2} Nm/Amp
K_V ..... 1.5×10^{-2} V-sec/rad
J (including platters) ..... 1×10^{-3} Nm-sec2
R_M 2.5Ω
L_M ..... 2 mH

For this motor, the model capacitor, C_M, is calculated using the equation in Figure 2 to be equal to 4.4 Farads. If we calculate the quality factor of the series RLC, using equation 2, we find it is equal to 42.4×10^{-3}. This is considerably less than one, and the response closely approximates the non-complex response of equation 3 with poles at 0.014 Hz and 199 Hz.

Typical loop bandwidths will fall well inside this range of frequencies. As long as this is true, the loop response with a voltage driven motor can be approximated by:

$$6)\quad A_{OLV}(s) \approx \frac{K_\phi \times K_{LF}(s) \times K_{PD}/R_M \times N}{s^2 C_M K_V}$$

$$\text{If } Q_M \ll 1 \text{ and } \frac{1}{2\pi C_M R_M} < f < \frac{R_M}{2\pi L_M} \left(f = \left|\frac{s}{2\pi}\right|\right)$$

This expression is the same as the current driven response, equation 4, with the transconductance of the current drive stage, G_{PD}, replaced by the gain of the voltage drive stage divided by the motor winding resistance, K_{PD}/R_M.

CLOSING THE LOOP

When it comes to closing the loop the goal is to have a stable loop with the required loop bandwidth. The variables that must be considered are:

1) The motor
2) The power driver, type and gain
3) The phase detector gain
4) Loop bandwidth
5) The loop filter

The first four of the above variables are usually dictated by conditions other than the stabilizing of the loop. This leaves the loop filter as the tool for achieving the small signal loop requirements.

For many cases involving constant velocity loops for DC motor speed control, the following simple Bode analysis can be applied for determining the design of the loop filter. Assuming we know, or have preliminary guesses for the first four variables listed above, we can plot the Bode asymptotes for phase and gain of the combined response of the motor and power driver. Figure 5 shows, for a typical case, such a plot on a frequency scale that has been normalized to the desired loop bandwidth, or open loop unity gain frequency. This figure illustrates the small signal open loop response for the current driven case, equation 4, minus the response of the loop filter, K_{LF}. If the previously noted assumptions hold, this plot will also apply to the voltage driven case i.e., equation 6.

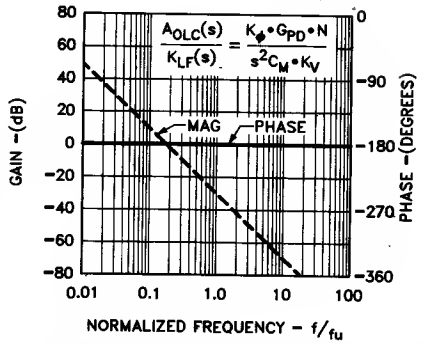


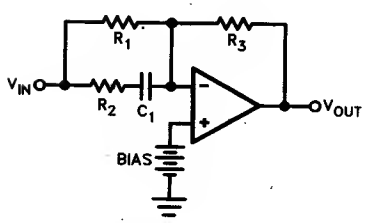
Figure 5. A Bode plot of the combined gain and phase response of the motor, motor drive, and phase dectector is useful in determining the requirements on the loop filter. This plot is normalized to the desired open loop unity gain frequency.

From Figure 5 two restrictions on the loop filter are readily apparent. First, since the remaining portion of the loop has 180° of phase shift over the entire frequency range, the loop filter must have a phase lead at the unity gain frequency and at all frequencies below the unity gain frequency. By meeting this restriction the small signal loop will be unconditionally stable.

Secondly, in order to achieve the desired loop bandwidth, the loop filter must have a voltage gain at the desired unity gain frequency of 30 dB. This level is simply the inverse of the remaining loop's voltage gain at the unity gain frequency.

A loop filter configuration that will meet these restrictions is shown in Figure 6. Also shown in this figure is the small signal response equation for the filter. The response starts out from DC with a flat inverting gain that breaks upward at the zero frequency, ω_Z, and then flattens out again at the pole, ω_P. The pole in this response is necessary to prevent excess feedthrough of residual reference frequency that is present at the outputs of many digital type phase detectors—in fact, as will be discussed in the design example, a separate reference filter is normally required.

A good choice for the relative positioning of the pole and zero of the loop filter response is to space them apart by 1 decade of frequency, and center them around the unity gain frequency. Figure 7 shows the Bode plots of this suggested positioning applied to the case illustrated in Figure 5. As shown, a phase margin of about 45° is obtained with this configuration.



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_3}{R_1} \times \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\,C_1}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

Figure 6. This loop filter configuration provides the required phase lead and gain at the loop crossover frequency.

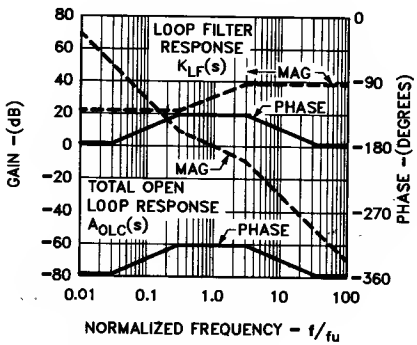


Figure 7. Using the criteria set forth for the design of the loop filter, the resulting Bode plot indicates a phase margin of 45°.

If the above results are acceptable, then the following simple steps can be applied to pick the loop amplifier component values. Referring to Figure 6.

9

1) Pick R_3 to be as high in value as acceptable for the Op-Amp and board restrictions.

2) $R_1 = (R_3 \times 3.33)/10^{X/20}$, where X is the voltage gain, in dB, required at the unity gain frequency.

3) $R_2 = R_1/9$, sets a 10:1 ratio for ω_P to ω_Z.

4) $C_1 = (2\pi \times R_2 \times 3.33 \times f_\mu)^{-1}$, where f_μ is the loop unity gain frequency.

Using this simple procedure the small signal loop is easily closed for stable static operation.

A DESIGN EXAMPLE

As an example, let us take a look at the complete design of a constant velocity speed control loop for a disc drive application. The performance characteristics for the circuit can be summarized as:

Motor speed ..... 3600 rpm ±60 ppm (0.006%)
Speed stability ..... ±50 ppm
Start-up lock time ..... 10 seconds
Input voltage ..... 12 Volts
Motor idling current ..... 0.5 Amps

The schematic for this design is shown in Figure 8. The motor is a 4 pole 3-phase brushless with the electrical and mechanical specifications given in the figure. The motor is current mode driven with the UC3620 3-phase Switchmode Driver. The speed control function is realized with the UC3633 Phase Locked Controller.

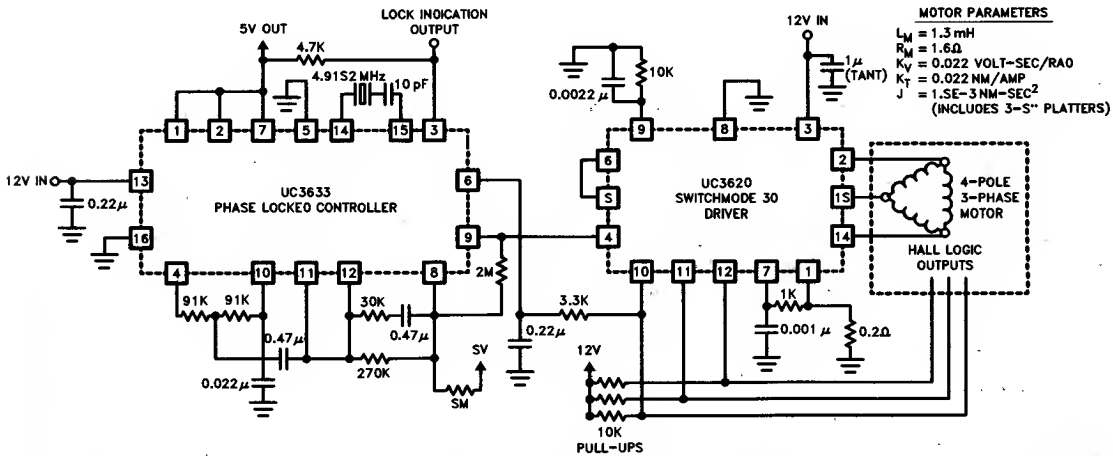


Figure 8. A precision speed control loop uses the UC3620 Switchmode 3-phase Driver and the UC3633 Phase Locked Controller to spin a DC brushless motor at 3600 rpm, ±60 ppm.

POWER DRIVER STAGE

In Figure 9 a detail of the driver IC and the associated circuitry is shown. The UC3620 is a current-mode, fixed off-time, chopper. Three 2-Amp totem pole output stages with catch diodes drive the three motor phases. The outputs are enabled by the internal commutation logic that responds to the three Hall logic signals from the motor. The motor is equipped with open collector Hall devices making the three 10k pull-up resistors on the UC3620 Hall inputs necessary.

Current is controlled by chopping the lowside drive to the phase winding under the command of the UC3620's current sense comparator. The RC combination on the timing pin of the driver sets the off-time at 22 μs. This results in a chopping frequency of well over 20 kHz under normal operating conditions.

The transconductance of the driver is set by the value of current sense resistor used at the emitter pin of the UC3620. With a value of 0.2Ω the transconductance from the error amplifier output to the driver outputs is 1 Amp/Volt. The UC3620 error amplifier is configured here as a unity gain buffer, thus the drive control signal is applied at the non-inverting error amplifier input with the same overall transconductance. An internal 0.5V clamp diode at the current sense comparator input results in a 2.5 Amp maximum drive current. There is a 1V offset internal to the UC3620 that is reflected to the drive control input at zero current. This offset combines with the 0.5 Amp idling current level of the motor to set the steady state DC voltage at the driver control input to be 1.5V.

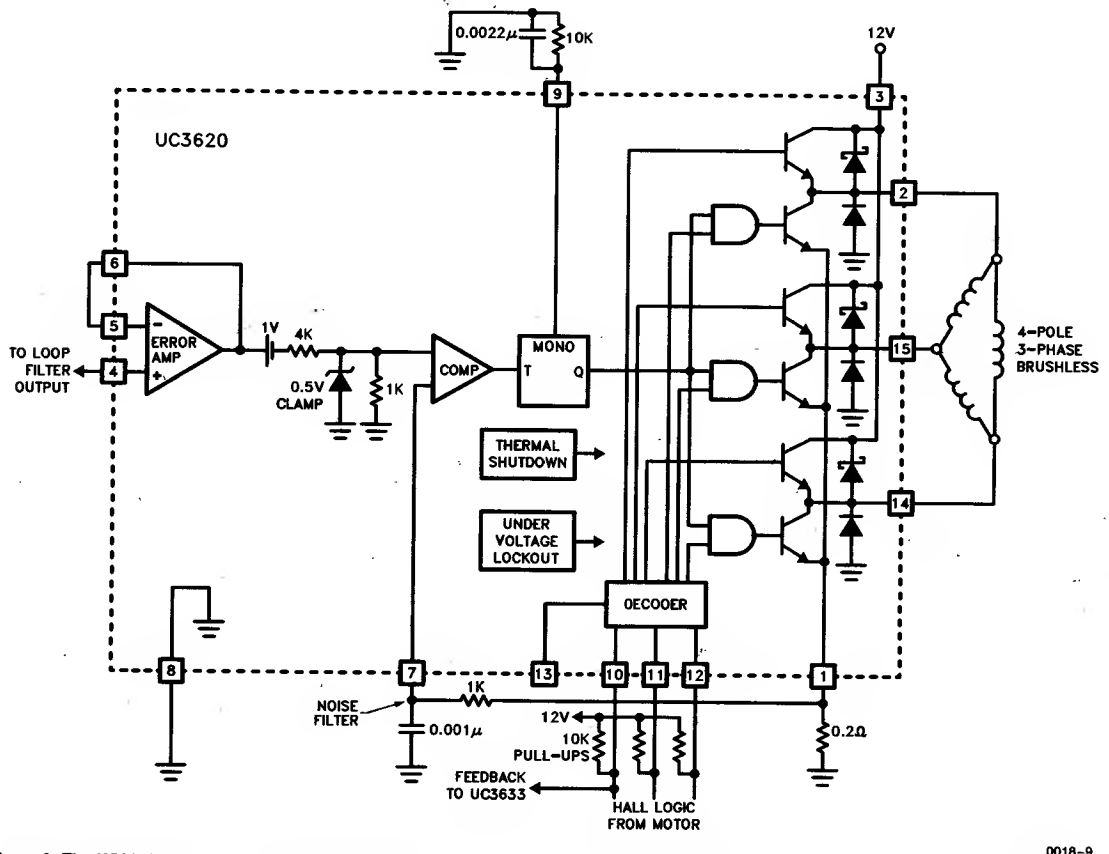


Figure 9. The UC3620 is a current mode fixed off-time driver. This device includes all the drive and commutation circuitry for a three phase brushless motor. The 0.2Ω current sense resistor and the internal divide by five sets the transconductance of this power stage to 1 Amp/Volt.

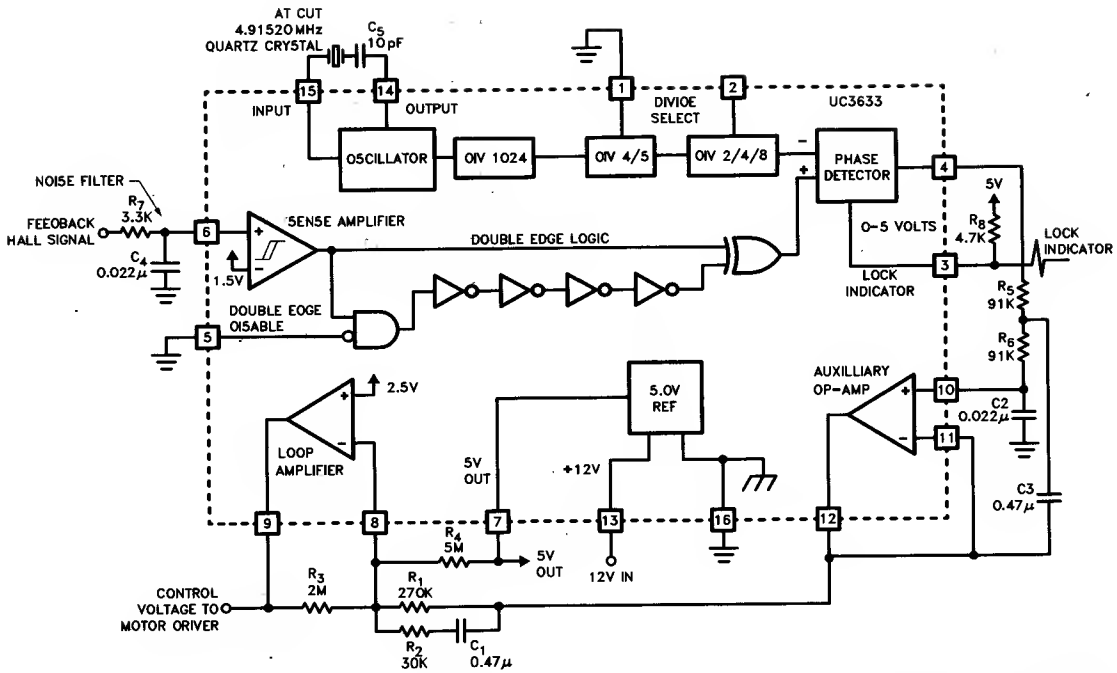


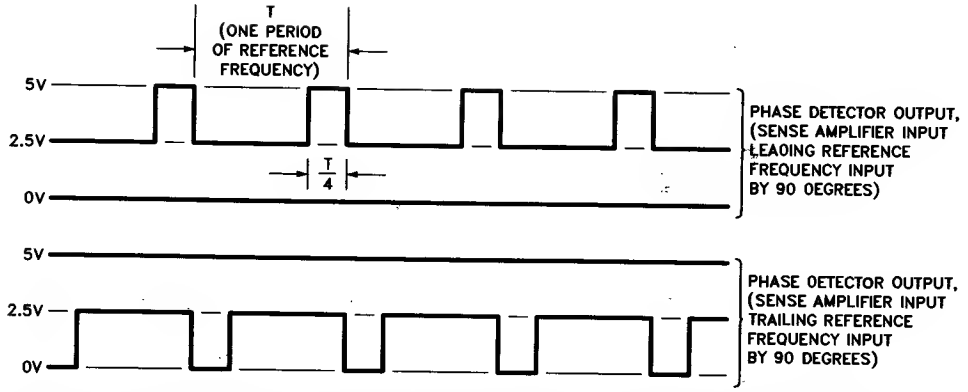
Figure 10. Phase locking the motor to a precision reference frequency is achieved with the UC3633. The double edge sensing option on this device doubles the loop gain and allows twice the reference frequency to be used for a given motor RPM by forcing the phase detector to respond to both edges of the Hall feedback signal.

PHASE LOCKED CONTROL CIRCUIT

A detail of the phase locked control portion of the design is given in Figure 10. The UC3633 contains all of the circuitry required for this function including: a crystal oscillator, programmable reference dividers, a digital phase detector, and op-amps for the required filtering. The UC3633 receives velocity feedback from the Hall signal applied at its sense amplifier input pin. The sense amplifier has a small amount of hysteresis that provides fast rising and falling input edges to the following logic. A double edge option is available on the UC3633 sense amplifier. When this option is enabled, as it is in this design, the phase detector is supplied with a short pulse on both the rising and falling edges of the feedback signal, effectively doubling the loop gain and reference frequency.

The required reference frequency for this loop is 240 Hz, given by the product of the motor rotation of 3600 rpm (60 Hz), the number of cycles/revolution at the Hall outputs (two for a 4 pole motor), and a factor of two as a result of the double edge sensing. The divider options on the UC3633 are set up such that standard microprocessor crystals can be used. In this instance, a 4.91520 MHz (±50 ppm) AT cut crystal is divided by 20,480 to realize a 240 Hz reference frequency input to the phase detector.

The phase detector on the UC3633 responds to phase differences at its two inputs with output pulses at the reference frequency rate. The width of the pulses is linearly proportional to the magnitude of the phase error present.



0018-11

Figure 11. The phase detector on the UC3633 is a digital circuit that responds to phase error with a pulsed output at the reference frequency rate. The width and polarity of the pulses depend respectively on the phase error magnitude and polarity. If any static frequency error is present, the detector will respond with a constant 0 Volt or 5 Volt signal depending on the sign of the error present.

The pulses are always 2.5V in magnitude and are referenced to 2.5V at the detector output. The polarity of the output pulses tracks the polarity of the input phase error. This operation is illustrated in Figure 11. The resulting phase gain of the detector is $2.5V/2\pi$ radians, or about 0.4V/rad, with a dynamic range of $\pm 2\pi$ radians.

The phase detector also has the feature of absolute frequency steering. If any static frequency error exists between the two inputs, the output of the detector will stay in a constant high, or low state; 5V, if the feedback input rate is greater than the reference frequency and 0V, if the opposite frequency relationship exists. The lock indicator output on the UC3633 provides a logic low output when any static error exists between the feedback and reference frequencies.

A unity gain bandwidth of 4 Hz was chosen for this loop. This unity gain frequency is well below the effective sampling frequency, the 240 Hz reference, and is sufficently high to not significantly affect the start-up lock time of the drive system. The design of the loop filter follows the guidelines described earlier. The magnitude of the loop gain, minus the loop filter, at 4 Hz is equal to:

$$\frac{K_\phi \times G_{PD} \times N}{(2\pi f)^2 \times C_M \times K_V} = \frac{(0.4)(1)(4)}{(2\pi 4)^2(3.1)(0.022)}$$

$= 37.2$ E-3 or -28.6 dB.

This dictates that the loop amplifier has a gain of 28.6 dB at 4 Hz. A value for the loop amplifier feedback resistor, R_3, of 2 MΩ was chosen. The values for R_1, R_2 and C_1 were calculated as follows.

$R_1 = (2E6 \times 3.33)/10^{28.6/20} = 248$ kΩ (270 kΩ used).

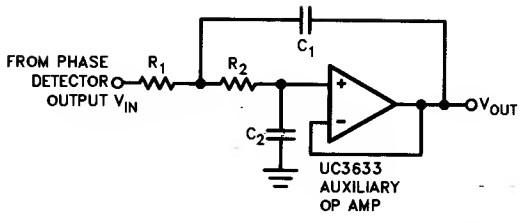
$R_2 = 270/9 = 30$ kΩ

$C_1 = (2\pi \times 30E3 \times 3.33 \times 4)^{-1}$
$= 0.4\ \mu F$ (0.47 μF used).

The additional op-amp on the UC3633 is used to realize a second order active filter to attenuate the reference component out of the phase detector. The filter is a standard quadratic with a natural frequency of 17.2 Hz and a Q of about 2.3. This circuit provides 46 dB of attenuation at 240 Hz while adding only 5° of phase shift at the 4 Hz loop crossover frequency. In Figure 12 design guidelines and response curves for this filter are given.

9

Reference Filter Configuration



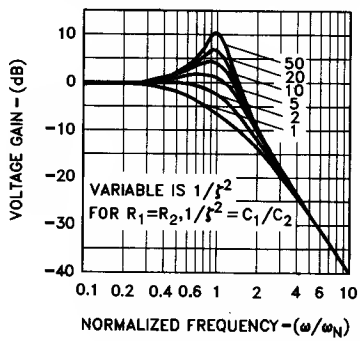
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid—Gain Response



Reference Filter Design Aid—Phase Response

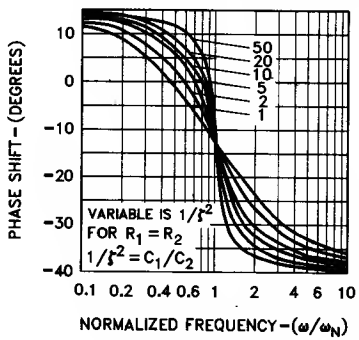


Figure 12. To keep feedthrough of the residual reference frequency at the phase detector output to a minimum, a simple quadratic filter can be used. The design of this filter is easily accomplished with the above equations and response curves.

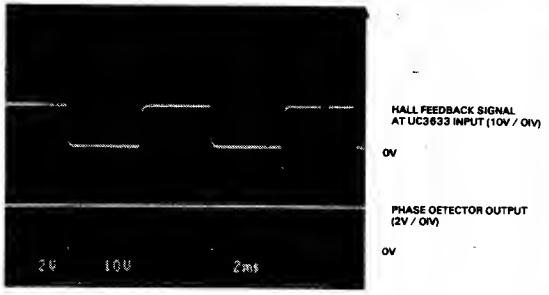
As mentioned earlier, a separate reference filter is required in this type of phase locked loop to attenuate the reference frequency feedthrough at the output of the phase detector. With the active filter following the phase detector, the feedthrough to the loop amplifier is kept to less than $20mV_{pp}$ under the worst case condition of $\pm\pi(180°)$ phase error. This is small compared to the 1.25V DC signal out of the detector at this phase error. If the reference ripple into the loop amplifier becomes large compared to the averaged phase error term, large signal instabilities may result. These are primarily the result of the unidirectional nature of the motor drive.

The static reference ripple at the motor drive input, during phase locked conditions, can be minimized by forcing the loop to lock at zero phase error—at zero phase error there is no reference frequency component at the detector output. The finite DC gain through the loop filter, dictated by the inherent second order nature of the loop, results in a static phase error that is a function of: the DC level required at the motor drive input, the DC gain and reference voltage of the loop amplifier, and the voltage levels out the phase detector. The addition of resistor R_4, see Figure 10, from the loop amplifier's inverting input to

the 5V reference sets the zero phase operating voltage at the loop filter output to 1.5V. This matches the nominal operating voltage required at the UC3620 control input, taking into account the 0.5 Amp idling current of the motor and the 1V offset of the driver. This cancellation is subject to variations due to shifts in DC operating levels, so, while it does significantly reduce static reference feedthrough, it can not be expected to reliably set exactly zero phase operation.

The oscilliscope traces in Figure 13 show the Hall input to the UC3633 along with the output waveform of the digital phase detector under static phase locked conditions. Notice that the phase detector output is alternating between positive and negative output pulses. This is a result of a slight asymmetry on the Hall input signal in conjunction with the use of the double edge sensing being used. In this case, the asymmetry is due to differences in the rising and falling edges of the Hall signal that result from the RC filter at the sense amplifier input. This filter is required to keep high frequency noise from the motor drive out of the phase detector.

The startup response of the motor is pictured in Figure 14. Shown are the voltage waveforms at the lock indicator output, the loop amplifier output, and the phase detector output of the UC3633. At the moment the lock indicator goes high the motor has reached its operating velocity. The absolute frequency steering of the phase detector forces a slight overshoot in frequency that delays the settling of the loop by about 1 second. Without the frequency steering feature the phase detector would command a much lower average drive signal during startup, extending the start time by over 50%.



0018-15

Figure 13. This oscilloscope trace shows the static waveforms at the Hall sensor input, and phase detector output of the UC3633. The static phase error has been adjusted, with R_4 in Figure 10, to be very small. The alternating positive and negative pulses at the output of the phase detector is due to an asymmetry in the Hall signal.

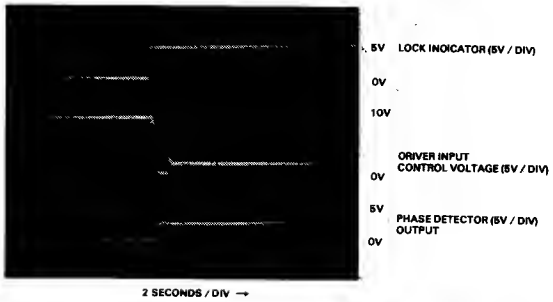


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Figure 14. The startup lock time of the motor is minimized with the absolute frequency steering feature of the phase detector, keeping lock times under 10 seconds.

9

UC 3841 PWM CONTROLS 300 WATT OFF-LINE POWER SUPPLY

by Bill Andreycak
UICC Application Dept.

INTRODUCTION

With the introduction of the UC3841, Unitrode has provided a control chip uniquely optimized to implement primary side control for a broad range of power supply applications. This form of control requires significant programming and fault protection intelligence over and above the requirements for merely regulating an output voltage. These are included in the UC3841 in the form of over-voltage, under-voltage, and over-current sensing, in addition to low-current start-up, feed-forward line regulation, duty cycle limiting, slow turn-on, and optional fault latch-off.

Although all of these features are important to most off-line power supplies - and are incorporated in the design described herein - it is beyond the scope of this paper to discuss the inner workings of the control circuit. Rather, the reader is referred to the UC1841/3841 data sheet and to Unitrode Application Note U-91 describing its predecessor, the UC1840 for details of the IC implementation. This note describes the use of the UC3841 as the controller in a typical application - a 300 watt off-line power supply.

TOPOLOGY OVERVIEW

A buck-derived, two transistor forward topology was selected for this example for several important reasons: two 400 volt transistors are typically much less expensive than one 800 volt unit; peak currents and ripple are much less than with a flyback configuration; clamping is done to the bulk DC lines eliminating the need for dissipative high-voltage snubbers; and transformer reset is automatic requiring only a 50% maximum duty cycle limitation. The basic power stage configuration and typical operating waveforms are shown in Figure 1.

While the UC3841 is compatible with either voltage or current mode control, this design is a voltage-mode configuration which takes advantage of the UC3841's controlled PWM ramp waveform to accomplish fast feed-forward line regulation while also guaranteeing an absolute 50% maximum duty cycle clamp.

SWITCHING FREQUENCY

A design decision of equal importance to the power topology is the choice of switching frequency. For this example, 200 kilohertz was selected as an optimum compromise between minimizing the sizes of the magnetic and storage components and achieving a high overall efficiency. This frequency is high enough to keep the number of transformer turns low and yet not so high as to incur significant switching or core losses. Standard commercial devices were used throughout to demonstrate the cost effectiveness of this design.

DESIGN SPECIFICATIONS

The specification goals which were established - and met - for this design example are the following:

Input voltage (110 VAC input) = 85 min, 135 max VAC

Input voltage (220 VAC input) = 170 min, 275 max VAC

AC line frequency = 50 Hz min

DC bulk voltage = 200 min, 385 max VDC

Output voltage = 15 volts

Output current = 20 amps max continuous

Switching frequency = 200 kilohertz

Line regulation = 10 mV

Load regulation = 10 mV

Output voltage ripple = 100 mV pk-pk, DC to 20 MHz

Efficiency = 85% at full load

CIRCUIT OVERVIEW

The complete schematic for this 300 watt power supply is shown in Figure 2 but before discussing the details of the design, it is instructive to understand the overall approach.

The design starts with a 110 volt input voltage doubler for a nominal 290 volt DC main allowing either 110 or 220 volt operation. The control and drive circuitry are configured for low start-up current so that starting energy is accumulated in a low voltage capacitor, C10 in Figure 2, which is charged from the high-voltage bulk DC through a large-valued resistor, R2. After starting, the higher operating currents of the control and drive circuits are supplied from an efficient low-voltage winding on the power transformer. This would normally be a separate primary-referenced axillary winding and isolation would be incorporated in the feedback path for output voltage control. For this example, isolation was

TWO-TRANSISTOR FORWARD CONVERTER

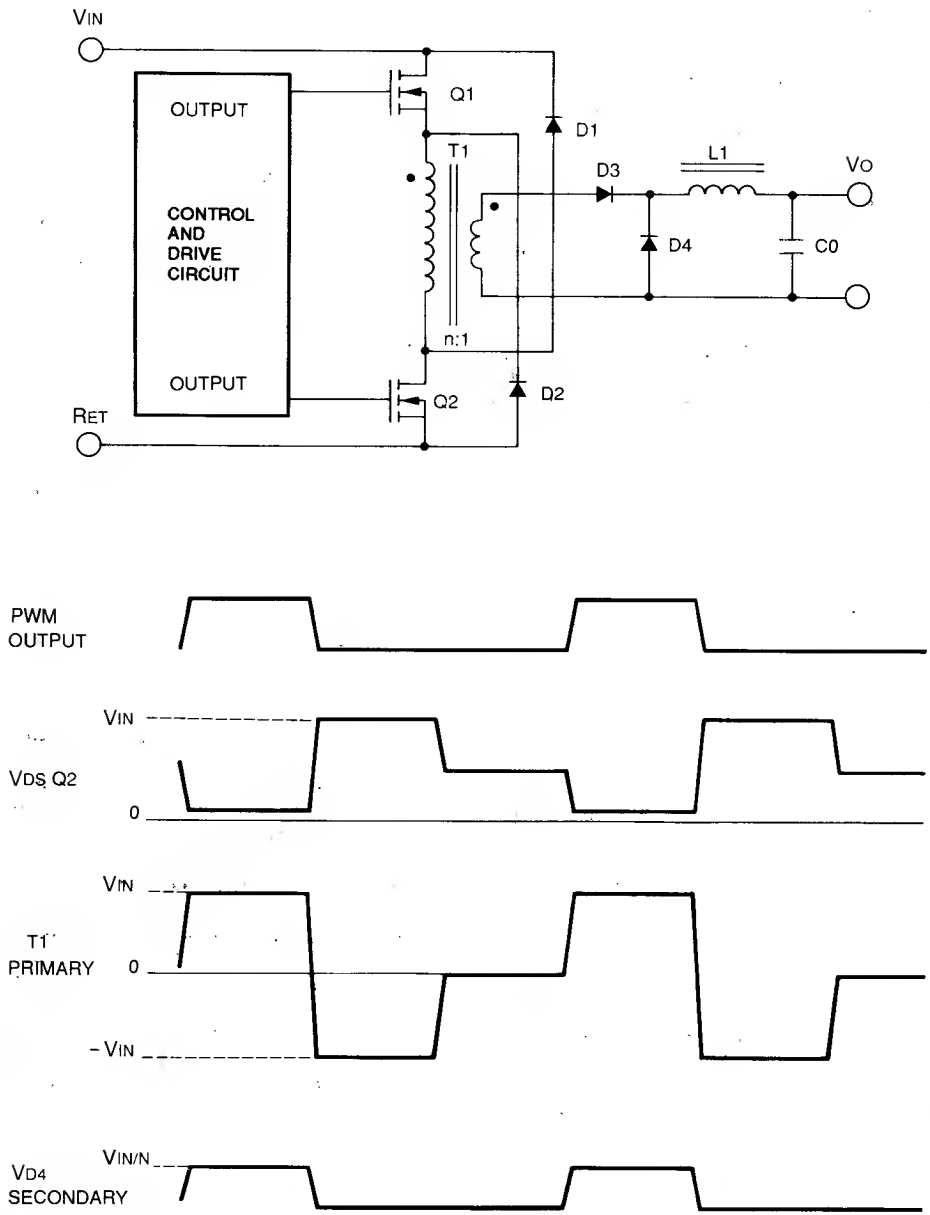

Figure 1. Basic power topology and typical waveforms for the Two-Transistor Forward Converter

ignored and operating power after start-up was taken from the 15 volt output - a simplification which can easily be remedied using common techniques which will not affect the remaining design.

The UC3841 provides the means to sense adequate energy in the start-up capacitor and initiate the turn-on sequence. It then activates the UC3707 Driver which boosts the PWM output from the UC3841 to a high peak current, source/sink drive command.

This signal is level-shifted by transformer T1 and applied simultaneously to the gates of the two power MOSFET switching devices, Q2 and Q3. These two FET's drive the power transformer, T2, in the forward direction with reset provided by D6 and D9.

Additional features which are incorporated in this design include slow turn-on - both initially and after fault shutdown, over-voltage and over-current shutdown, pulse-by-pulse current limiting for light overloads, feed forward for fast line regulation, and a maximum duty cycle clamp.

CIRCUIT DESIGN DETAILS

INPUT STORAGE CAPACITANCE

The amount of input, or bulk storage capacitance for a given power supply design will be determined by the more stringent of three separate requirements:

1. Maintaining a minimum DC bulk voltage as the input capacitor supports the converter between AC cycles.

2. Providing a minimum hold-up time for operation after loss of the AC line voltage.

3. Meeting the requirements for AC RMS charging current.

In this case, the value was calculated to support the primary voltage between AC cycles to a minimum of 200 VDC. In a dual voltage system, the most stringent case is the doubler configuration where there is a 180 degree phase shift between the voltage waveforms on each of the series capacitors. The minimum DC bulk voltage is then the sum of the minimum voltage on one series capacitor plus the average voltage on the other. The value of each capacitor is calculated from the following formula:

$$C1 = C2 = \frac{\text{Output power}}{\text{Efficiency} \times \text{AC frequency} \times (Vc\ peak^2 - Vc\ min^2)}$$

Where, in this example,

AC frequency = 50 Hz,

Vc peak = (80 x 1.414) - Vd = 115 V, and

Vc min = .33 (2 x 200 - Vc peak) = 95 V

which determines a value for C1 and C2 of 1680 microfarads each. This was actually implemented as shown in Figure 2 by four 1000 uF units, C1 through C4.

PRIMARY AND SECONDARY CURRENT

An estimate of the maximum primary and secondary currents is needed to select the power switches, diodes, and transformer wire sizes. A first-order approximation can be calculated from the equation:

$$Ipeak = \frac{\text{Output power}}{\text{Efficiency} \times \text{Input voltage} \times \text{Max duty cycle}}$$

$$= \frac{300}{0.85 \times 200 \times 0.50} = 3.52 \text{ Amps}$$

For rectangular wave forms, RMS currents are calculated by multiplying peak current by the square root of the duty cycle yielding 2.5 Amps of primary current and 14 Amps for the secondary winding.

MOSFET SELECTION

As described in the Topology section, one advantage of the two-transistor forward converter is that the maximum voltage on the power switches does not exceed the peak input voltage. In this example, it allows the use of 500 Volt IRF 840 power MOSFETs which have a fairly low on resistance of 0.8 ohm, more than adequate current capability, and are available in plastic TO-220 packages. Heatsink requirements can be calculated by starting with the DC losses:

$$P\ loss = Ip\ peak^2 \times Rds_on\ max \times D\ max$$

Extrapolating the maximum Rds on value for the IRF 840 to a junction temperature of 110°C yields 1.75 ohms which means a DC loss of 10.8 watts. Rounding up to 12 watts to include switching losses means that with a maximum ambient temperature of 70 °C, the junction will stay below 110 °C if the total thermal resistance, including the 1.0°C/W of the TO-220 package, is held to less than 3.3°C/W.

RESET DIODES

Since the current through the reset diodes, D9 and D10, returns to zero when the core completes reset, diode reverse recovery time is not critical. Forward turn-on time is still important, though, in order to catch the transformer energy when the power switches turn off, but this is a much simpler problem and UES 1106 rectifiers are more than equal to the task.

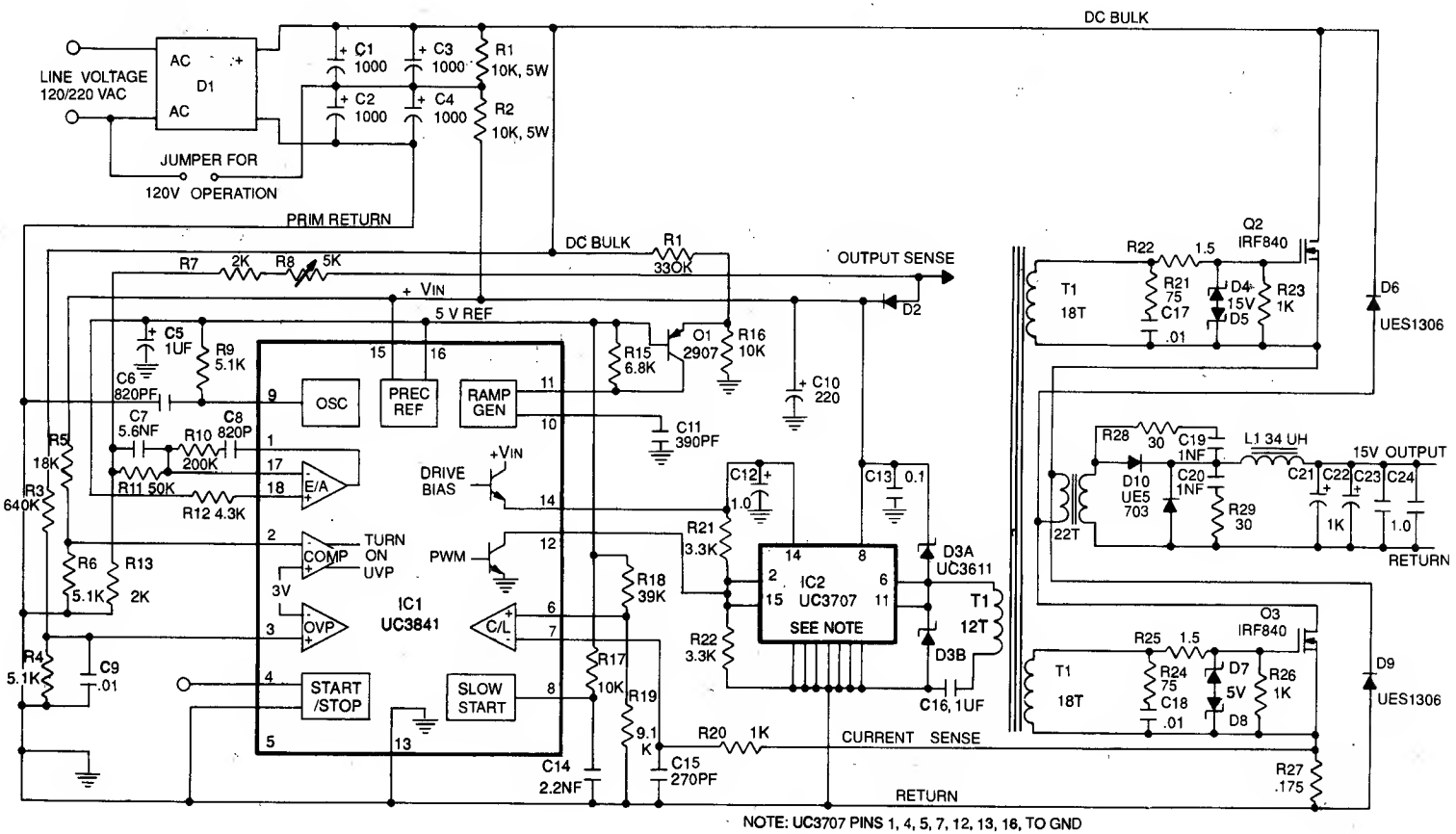

Figure 2. Overall schematic for a 300 watt, off-line power converter using the UC 3841 for control

TRANSFORMER DESIGN

As a general guideline, operation at higher frequencies usually produces a transformer design which is core loss, rather than flux swing, limited. Under these conditions, it is best to start with the core area-product calculation using the formula:

$$AP = AwAe = \left(\frac{Pin \times 10^4}{120\ K\ 2f_t} \right)^{1.58} \times (Kh\ f + Ke\ f^2)^{.66} cm^4$$

where:

Pin = Input Power = 353 Watts

K = Winding Factor = .141 (for a fwd conv)

f_t = Transformer Frequency = 200 kHz

Kh = Hysteresis Coefficient = 4×10^{-5} (3C6A)

Ke = Eddy Current Coefficient = 4×10^{-10} (3C6A)

For this design, the area-product calculates to 2.9 cm^4 allowing a comfortable selection of an ETD-44 ferrite core made of 3C6A material. Core selection is typically an iterative process with the first core choice used to define the windings which, in turn, allows calculation of both winding and core losses. If these answers are not acceptable, another core size is selected and the process repeated.

The manufacturer defines the ETD-44 core as having a volume of 18.0 cm^3 and a thermal resistance of 12°C/W. Selecting 40° C as a reasonable limit for the maximum temperature rise of the transformer and recognizing that core loss will be an important factor, an arbitrary starting point for the transformer design is to allocate 30°C to the core and 10°C to the copper. With this assumption, the core power density can be calculated from:

$$\text{Power Density} = \frac{\text{Temp rise}}{\text{Therm Resist x Volume}} = 140\ mW/cm^3$$

The manufacturer's curves of core losses for the 3C6A material at an operating frequency of 200kHz show a corresponding peak flux density of approximately 600 Gauss which equates to a peak-to-peak value of 1200 Gauss, or 0.12 Tesla. Additional data needed to calculate the primary turns are the primary voltage, Vp = Vin - Vsat, and an estimate of the maximum duty cycle which, to provide some margin, is initially set at 0.47. With these inputs, the primary turns are defined by:

$$Np\ min = \frac{Vp \times Ton \times 10^4}{\text{Flux swing x Core area}}$$

$$= \frac{190 \times 2.35 \times 10^{-6} \times 10^4}{12 \times 1.74} = 21.3 \text{ turns}$$

The transformer turns ratio is defined as:

$$\frac{Np}{Ns} = \frac{Dmax \times Vp}{Vo + Vd} = Dmax \times \frac{190}{15.8} = 12.025\ Dmax$$

At this point, there are two considerations to balance: The desire to make Dmax as close to 0.5 as possible so that the peak current is low, while keeping the number of turns to low, whole numbers. For this example, the best choice is

$$\frac{Np}{Ns} = \frac{22 \text{ Turns}}{4 \text{ Turns}}$$

and Dmax = 0.46.

With this duty cycle, the peak primary current can be more accurately calculated as 3.84 Amps with an RMS value of 2.6 Amps.

The remaining transformer calculations are summarized below:

Primary inductance, $Lp = Al \times Np^2 = 1.26$ mH

Magnetizing current, Im = Vp x Ton / Lp = 347 mA (peak)

Primary conductor area, Axp = Ip rms / 450 = .00578 cm^2 min

Secondary conductor area, Axs = Is rms / 450 = .0301 cm^2 min

While the primary wire area corresponds to a wire size of AWG 19, and the secondary is equivalent to AWG 12, both have to be evaluated in terms of their active area at 200 kHz. From Eddy Current calculations it can be determined that the depth of penetration of current at 200 kHz is .017 cm which does not effectively utilize the .091 cm diameter of AWG 19 wire. While multiple strands of finer wire help, increasing the number of strands also increases the number of layers which forces the wire thickness to be substantially less than the penetration depth in order to minimize the AC loss.

A more effective solution - which is made more practical because of the relatively few number of turns - is the use of flat copper strip. For the primary, a strip .0044 cm thick (approximately 2 mils) and 2.5 cm wide was insulated with 2 mil mylar between each turn and wound in two sections - eleven turns under and eleven turns over the secondary. The secondary was also made of copper strip, in this case .020 cm thick. A cross section sketch of the transformer winding technique is shown in Figure 3.

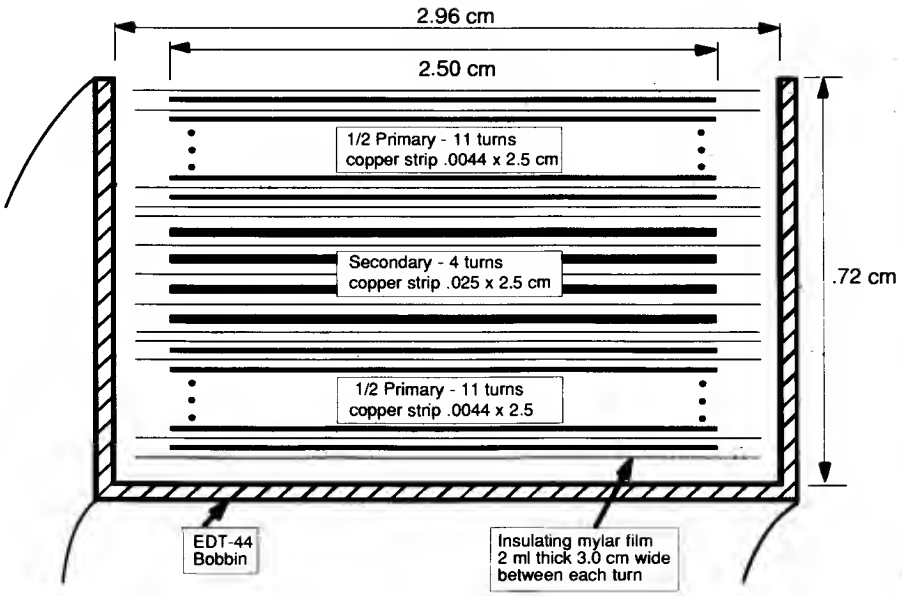

Figure 3. Cross section of one-half of the power transformer illustrating the strip winding techniques which minimize both Eddy Current losses and leakage in ductance.

With the windings defined, the total transformer losses may be calculated as follows:

Core loss = Power density x Volume = 2.52 Watts

$$\text{Primary resistance} = \frac{\text{Copper ohm-cm x ave cm/turn x Np}}{\text{Strip cross-section area}}$$

$$= \frac{2.29 \times 10^{-6} \times 7.6 \times 22}{.0044 \times 2.5} = 35 \text{ milliohm}$$

Wire loss (prim) = Ip_{rms}^2 x Rp = 0.24 Watts

$$\text{Secondary resistance} = \frac{2.29 \times 10^{-6} \times 7.6 \times 4}{.020 \times 2.5} = 1.39 \text{ milliohm}$$

Wire loss (sec) = 0.26 Watts

Total power loss = 2.52 + 0.24 + 0.26 = 3.02 Watts

Temperature rise = 3.02 W x 12 °C/W = 36 degrees.

GATE DRIVE TRANSFORMER

Since both the number of turns and the currents are small for this gate drive transformer, a toroidal core shape is an efficient solution and the core selected was the Ferroxcube 846T250 made of 3C8 ferrite material with an outside diameter of 0.875 inches. The design equations and guidelines are similar to the power transformer example. In this case, the primary winding is capacitively coupled to the driver IC to prevent core saturation. Because of the DC offset voltage on the capacitor, the primary voltage will now be to some extent dependent upon pulse width. A step-up turns ratio was used to the secondary with 15 volt zener clamps to limit the gate-to-source voltage on each FET. Twelve turns were used for the primary resulting in a 500 Gauss flux swing. Each secondary winding consists of 18 turns and the total core loss is calculated at 0.13 Watt.

OUTPUT INDUCTOR

The output inductor was designed for less than 1.8 Amps of ripple current at full load and minimum duty cycle using the equation:

$$L = \frac{(Vo + Vd) \times Toff}{\Delta \text{ Io max}}$$

and from:

$$Dmin = Dmax \times \frac{Vin\ min}{Vin\ max} = 0.46 \times \frac{200}{385} = 0.239 \text{ and}$$

$$Toff\ max = \frac{1 - Dmin}{f_t} = \frac{0.761}{0.2\ MHz} = 3.81 \text{ us}$$

the inductance value is then defined as:

$$L = \frac{15.8 \times 3.81}{1.8} = 33.4 \text{ uH Min}$$

9

Selected for this application was an ETD type core made from 3C8 material. This material was chosen because of its high saturation flux density of greater than 3000 gauss. Here again, it is necessary to determine whether the design will be core loss or saturation limited but since this is a forward converter with the inductor in the continuous mode, the AC ripple current is a small percentage of the DC load current and the core should be saturation limited.

The core selection process again starts with a calculation of window - area product using the equation:

$$AP = AwAe = \left(\frac{L \times Ipk \times Ifl \times 10^4}{420 \times K \times Bmax} \right)^{1.31} cm^4$$

$$= \left(\frac{34 \times 10^{-6} \times 25 \times 20 \times 10^4}{420 \times 0.7 \times 0.3} \right)^{1.31} = 2.36\ cm^4$$

With this AP value, an ETD-39 core was selected with a value of Ae = 1.25 cm^2. The minimum number of turns can then be calculated from:

$$Nmin = \frac{L \times Ipk \times 10^4}{Bmax \times Ae} = 23\ Turns$$

The gap length is then calculated using the classic inductance formula:

$$lg = \frac{\mu_o \times \mu_r \times N^2 \times Ae \times 10^{-2}}{L} = 0.219\ cm$$

with $u_o = 4\ \pi \times 10^{-7}$ and $u_r = 1$. To obtain the desired inductance, however, the actual gap must be almost twice as large to account for the fringing field which is not included in the above formula.

This inductor was also wound with copper strip but in this application the task is easier as neither Eddy Current losses nor space for high-voltage insulation need be considered. A strip 2.5 cm wide of 10 mil (.025 cm) copper was used which, with a mean turn length of 6.7 cm, gave a DC resistance of

$$R = \frac{2.29 \times 10^{-6} \times 6.7 \times 23}{0.025 \times 2.5} = 5.65\ mohms$$

and a power loss at full load of 2.26 Watts.

OUTPUT CAPACITOR

There are two sources of ripple voltage which need to be considered in meeting the design goal of 100 millivolts and they are both caused by the inductor ripple current. The first is merely

$\Delta Vo = \Delta Q / Co$

and, for a given ripple current, is minimized by increasing the capacitor value. The minimum capacitance, if this was the only contributor, is

$$Cout\ min = \frac{1 \times \Delta Io \times 1 \times 1}{2 \times 2 \times 2f \times \Delta Vo}$$

$$= \frac{1.8}{8 \times 200k \times 0.10} = 11.25\ microfarads$$

The second source of ripple voltage is the voltage drop across the ESR of the capacitor caused by the ripple current. The maximum ESR allowable for 100 mV ripple is

ESR max = 100 mV / 1.8 A = 56 mohms.

The two contributors of ripple voltage do not add directly as there is a 90 degree phase difference between them. Typically, in order to achieve a reasonable ESR, the capacitance value becomes so much greater than the minimum value that the $\Delta Q / Co$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

For this design, two 470 uF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 mohms - a broad range necessitated by the difficulty in getting specified high-frequency data from capacitor manufacturers.

A final component added to the output filter is a good, high-frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. A 1.0 uF ceramic monolythic capacitor is a good selection for this application.

OUTPUT RECTIFIERS

The output diodes need to be able to handle the output current of 20 Amps, have 150 Volt reverse capability, and be extremely fast. Unitrode UES 703 rectifiers were selected for this application because of their 35 nsec reverse recovery specifications, as well as their low forward drop of 0.8 Volts max. Since one of the output diodes will always be conducting, it is advisable to mount both on the same heatsink designed to dissipate approximately 16 Watts with a 30 °C temperature rise. This will keep the junction temperature below 100 °C in a 70 °C ambient.

PROGRAMING THE CONTROL FUNCTIONS

With the completion of the power path design, the remaining tasks all relate to programing the many functions of the UC3841. In the interests of readability, the description which follows is a somewhat qualitative discussion of the methods for implementing the functions rather than a rigorous derivation of each component's value. Again, reference to the UC3841 data sheet is necessary for detailed specification limits and tolerances.

POWER SUPPLY START UP

When line voltage is first applied, the UC3841 is in its OFF state and draws less than 5mA from the line through R1 and R2. While there is an additional 2.4 mA due to the various programing resistors, the UC3707 draws no current as it is powered from the Driver Bias output of the UC3841 which is off during start up. Therefore, resistors R1 and R2, which are necessary anyway to discharge the bulk storage capacitors, can easily provide the current to charge the start up capacitor, C10, without the power dissipation which would require complex circuitry to disconnect them after start up.

The resistor divider of R5 and R6 performs two functions. The ratio of these resistors determines the actual turn-on voltage at C10 while their effective series impedance provides hysteresis such that turn-off occurs at a lower level than turn-on. In this circuit, the turn-on voltage is 17V and the hysteresis is 3.5V. This means C10 will charge to 17V while most of the circuit is off. When turn-on is initiated, the added load of the driver will cause this voltage to decay and it will fall either to 14.4V where the power supply output will catch it through D2, or, if start up does not take place, to 13.5V where the control will turn off and start a new cycle.

Prior to turn-on, and after a low-voltage turn off, the Soft-Start capacitor, C14 on Pin 8, is clamped low. At turn on, although the Driver Bias immeadiatly activates the UC3707, no power pulses are generated while Pin 8 is low. As C14 charges, PWM commands begin and the pulse width increases with a rate of increase defined by the time constant of C14 and R17. This time constant needs to be selected remembering that while start up is taking place, all the drive energy is coming from C10 so the charge of C14 has to be faster than the discharge of C10. These waveforms are shown in perspective in Figure 4.

START-UP WAVE FORMS

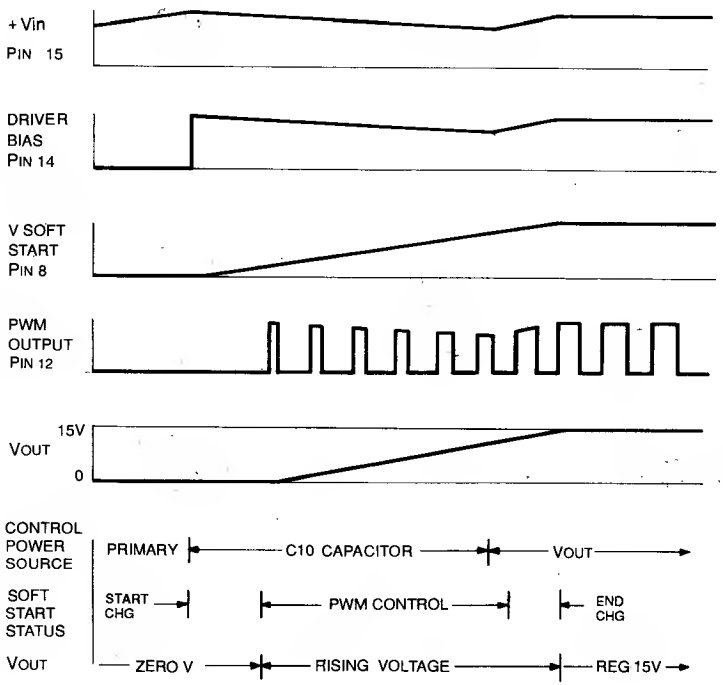

Figure 4. Initial start-up waveforms showing the slow turn on of the power output stage.

OSCILLATOR AND RAMP

The UC3841 operates at a fixed frequency determined by R9 and C6 on Pin 9. The pulse width modulation is performed by comparing the Error Amplifier's output to a separate ramp waveform generated on Pin 10. The slope of this ramp is given a minimum value by R15 charging C11 from the 5.0V reference. These components define a rise time of 2.5 usec and thereby establish a maximum duty cycle clamp of 47 percent. The network of Q1, R14, and R16 sense the DC bulk voltage and provide an increasing charge current to C11 - thereby increasing the slope of the ramp for bulk voltages above 200 volts. This increase in slope linearly tracks the input line voltage and modulates the PWM output signal providing fast, pulse-by-pulse, open-loop line regulation which greatly eases the requirements of the feedback control loop.

FAULT PROTECTION

Load current is sensed through the power transformer by a sense resistor, R27, in series with the power switches. The value of R27, in conjunction with the divider of R18 and R19, establish a threshold at Pins 6 and 7 of 23 Amps as related to the output. When this threshold is exceeded, the UC3841 goes into a pulse-by-pulse reduction in width to limit the energy and allow the power supply output to fall. Because of circuit delays, however, this limiting only works to a minimum pulse width which might allow too much energy to protect against a short circuit. This eventuality is covered by a second, higher threshold in the current sensing circuit which triggers a Fault Latch for immediate shut down. This Fault Latch is also activated by the Over-Voltage comparator which, in this case, is monitoring the input line voltage through R3 and R4.

Once triggered, the Fault Latch immediately terminates the PWM signals and discharges the soft-start capacitor. If the Reset Pin 5 is high, once latched, the circuit will stay off until either the input line is recycled or Pin 5 is momentarily pulled low. If Reset is already low, the Fault Latch will reset when the soft-start capacitor completes its discharge, allowing an automatic restart. The Fault Latch may also be activated externally by forcing positive current into Pin 4.

THE UC3707 DRIVER

This device is used only as an interstage driver to take the pull-down output from the UC3841 and develop the high current turn-on and turn-off commands to the power MOSFETs. This is a dual driver but in this case the two channels are connected in parallel to provide a maximum peak current of 3 Amps, source or sink. Of course, the DIL package would provide a power limitation were it not for the fact that the high currents are needed only to charge and discharge the MOSFET gate capacitance. When driving a load which has both inductance and capacitance, it is important to keep any ringing which might appear on the output of the driver chip confined within the limits of the supply voltage to that chip. This is easily accomplished with the UC3611 Schottky diode array used for diodes D3A and D3B.

CLOSING THE LOOP

In this voltage-mode application, the output filter will exhibit a two pole response to the control loop. Loop compensation at the Error Amplifier is designed to contain two pole-zero pairs by using the configuration shown in Figure 5. This will insure overall loop stability with maximum high frequency response while retaining a large low frequency gain.

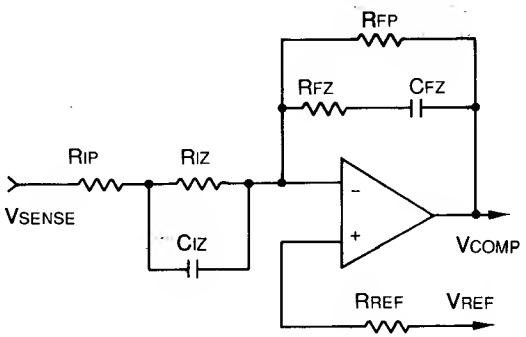

Figure 5. A generalized two pole-zero compensation approach to providing good loop stability.

The generalized approach to this compensation network is to place the first pole at a low frequency, typically around one Hertz. Two zeros are then introduced at approximately one-half the output filter break frequency to compensate for its two-pole rolloff. The amplifier's second pole is placed at a fairly high frequency to provide a predictable gain reduction; however, the amplifier will usually run out of gain-bandwidth prior to reaching this pole.

The output filter response is defined by:

Lout = 34 uH, Cout = 1000 uF,

Rload = 0.75 to 10 ohms, ESR = 3 to 15 mohms

$$\text{Pole freq} = \frac{1}{2\pi\sqrt{LC}} = 865 \text{ Hz}$$

$$\text{ESR zero} = \frac{1}{2\pi \times C \times ESR} = 10.6 \text{ to } 53.1 \text{ KHz}$$

The error amplifier compensation poles and zeros are located at the following frequencies referenced to the components of Figure 5:

$$\text{Input zero} = \frac{1}{2\pi \times Riz \times Ci} = 568\ Hz$$

$$\text{Input pole} = \frac{Rip + Riz}{2\pi \times Rip \times Riz \times Ci} = 23\ kHz$$

$$\text{Feedback zero} = \frac{1}{2\pi \times Rfz \times Cf} = 970\ Hz$$

$$\text{Feedback pole} = \frac{1}{2\pi\,(Rfp + Rfz)\,Cf} = 1\ Hz\ (approx)$$

The effect of these poles and zeros is shown graphically in Figure 6 where it can be seen that they provide an overall response with a single pole roll-off to 10 kHz. The gain crosses zero dB at approximately 8 kHz with more than adequate phase margin, regardless of the output capacitor's ESR.

POWER SUPPLY PERFORMANCE

The use of the UC3841 control IC has allowed a very straight forward and simple implementation of a relatively high performance power supply with a remarkedly small number of components. Representative waveforms of performance at several points within the supply are shown in Figures 7 - 10. All the initial performance goals defined for this design were met and it is hoped that with the information presented above, application to more sophisticated or specialized design tasks will be eased.

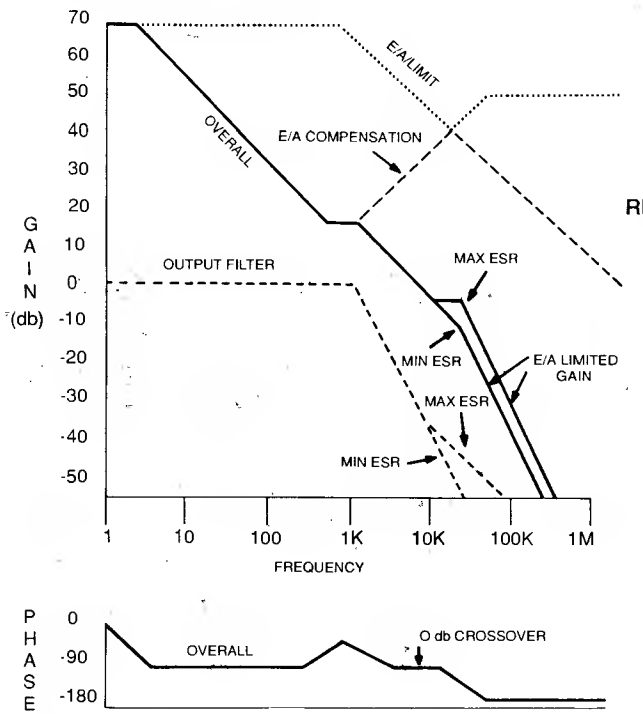

Figure 6. Total power gain and phase relationships showing the effects of loop compensation.

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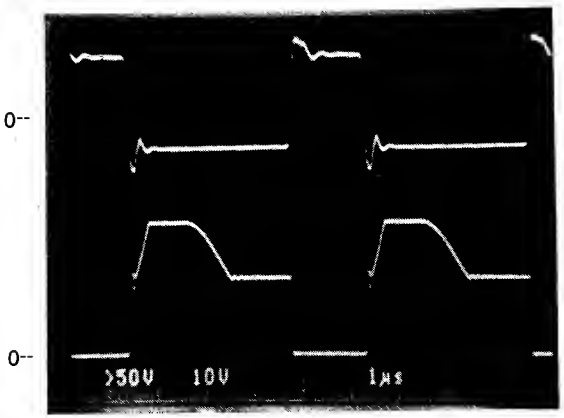
9

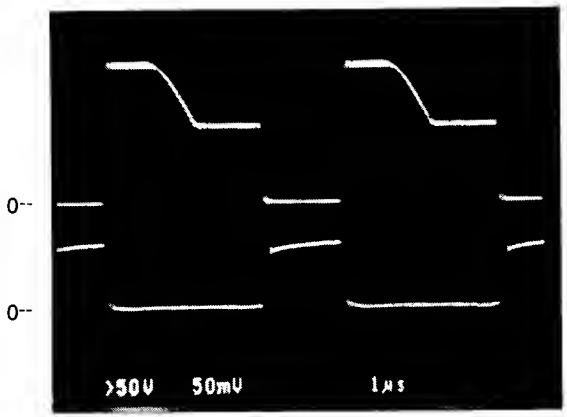
OPERATIONAL WAVEFORMS



PRIMARY

Top: V_{GS} Q1 10 v/cm
Bottom: V_{DS} Q1 100 v/cm
Horizontal: 1 µs/cm

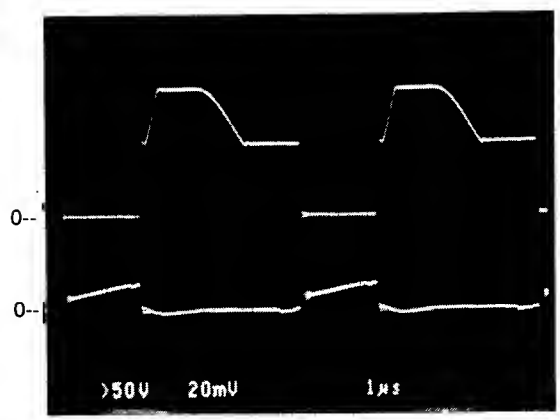
Figure 7. Gate-to-source and Drain-to-source voltage waveforms for the upper FET switch



FULL LOAD

Top: V_{DS} Q1 100 v/cm
Bottom: Ipri 2 A/cm
Horizontal: 1 µs/cm

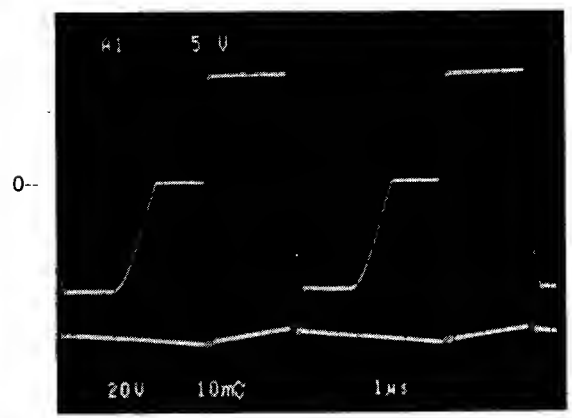
Figure 8. Power switch voltage and current waveforms at full load.



LIGHT LOAD

Top: V_{DS} Q1 100 v/cm
Bottom: Ipri 1 A/cm
Horizontal: 1 µs/cm

Figure 9. Power switch voltage and current waveforms at light load.



SECONDARY

Top: Vsec 20 v/cm
Bottom: Vout (AC) 10 mv/cm
Horizontal: 1 µs/cm

Figure 10. Transformer secondary voltage and power supply output ripple.

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New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors

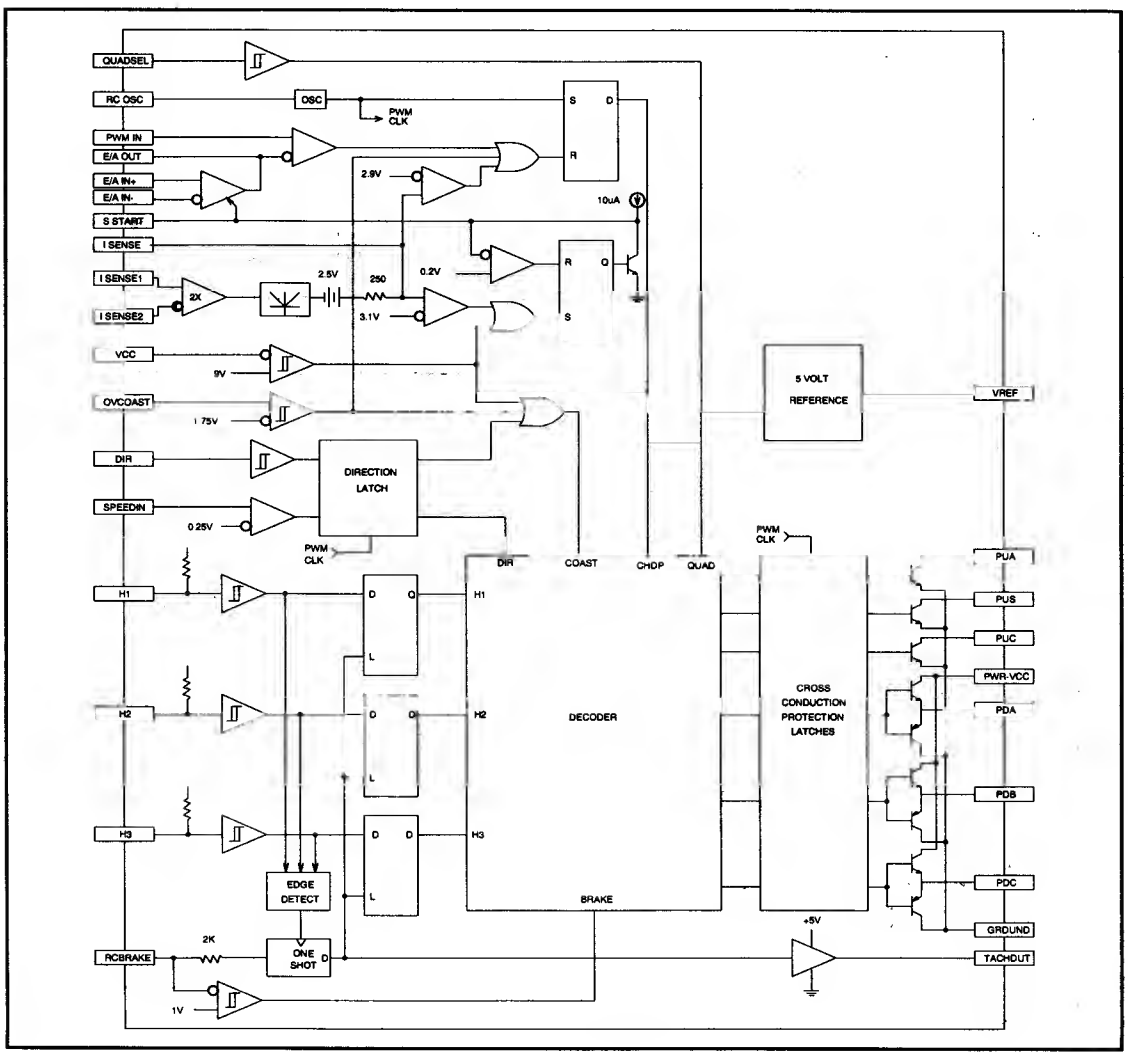
Bob Neidorff, Unitrode Integrated Circuits Corp., Merrimack, NH

Abstract

A new integrated circuit for brushless DC motor control is presented that implements many new techniques to enhance reliability and reduce the detrimental effects of noise. In addition to safety features and noise rejection circuitry, the new circuit contains a complete pulse-width modulator (PWM), a practical tachometer, a precision voltage reference, a high-speed current-sense amplifier, and high-voltage, high power, output stages.

Various applications of the IC are discussed in detail, including using the PWM for fixed frequency and fixed off-time control, driving power MOSFETs, driving bipolar power transistors, and sensing winding current. The IC is shown in applications that allow braking and direction reversal without damage to the motor or the power semiconductors.

BLOCK DIAGRAM OF THE UC3625



9

The Problem

Conventional brush motors have proven reliable and versatile. They remain popular partly because the pressures to improve haven't been high, and partly because nothing better has been available that is practical. Brushless DC motors (BDCMs) can pack the same horsepower into smaller, lighter boxes. They can also accelerate faster due to inherently lighter rotor construction. Without the friction and arcing of brushes, they are acoustically quieter. As they have permanent magnet rotors, they are faster to manufacture. Permanent magnet rotors also dissipate very little power, so BDCMs have far less heat dissipation problems.

One thing that has held the motor industry back has been the availability of economical control electronics. Recent price trends in power MOSFETs and monolithic motor controllers have reduced these limits. The final hurdle to broad acceptance is assurance of reliability. Brush motors proved their reliability not through design, but instead through over a hundred years of development of rugged brusheS and slip rings.

Two problems with BDCMs today are performance and reliability in the presence of noise. Noise here can refer to externally generated electromagnetic noise, internally generated chopping noise, or inappropriate commands from the operator of the system.

The UC3625 specifically addresses the need for an economical, robust BDCM controller by specifically addressing these failure modes and also by implementing many functions and features desirable in high performance motor systems. The following table outlines some of the important features of the UC3625:

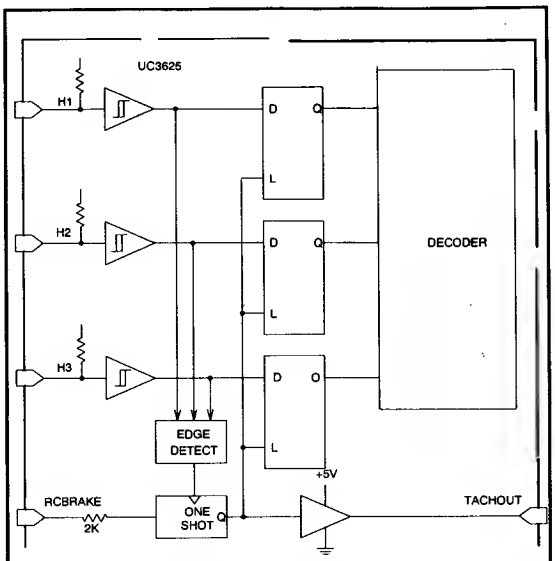
- Push-Pull Low-Side Drivers
- Versatile High-Side Drivers
- Complete PWM
- Two or Four-Quadrant Chopping
- Tachometer
- Soft Start
- Undervoltage Protection
- Overvoltage Protection
- Active Safe Braking
- Differential Current Amp
- Hysteresis on all inputs
- Direction latch
- Cross Conduction prevention

Unique Features For Noise

All logic inputs to the UC3625 have hysteresis and /or latches for maximum noise rejection. The position sensor inputs specifically contain 0.8 volts of hysteresis, yet still meet TTL input thresholds. These inputs also contain pull-up resistors allowing them to directly interface to open-collector sensors.

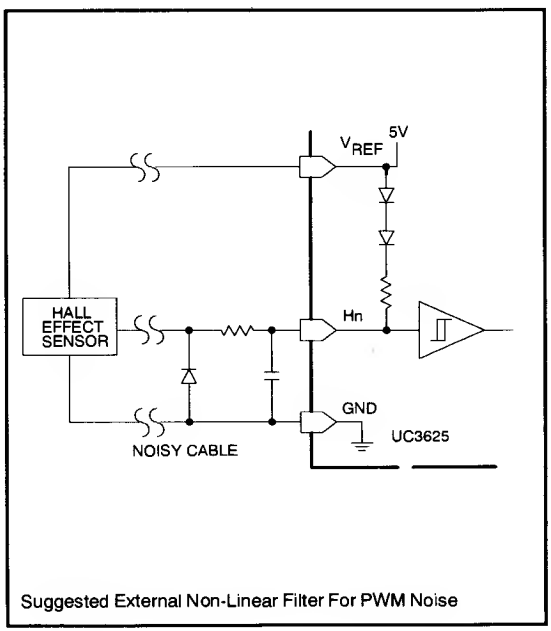
Position sensor inputs are latched immediately following commutation, and remain latched through the on-time of the tachometer monostable (one-shot). This prevents commutation noise from reaching the decoder, latching out the largest noise spike in the motor system. Although this sets a maximum motor speed, correct choice of pulse width guarantees operation up to the maximum speed of the motor while still affording excellent noise rejection.

The one-shot pulse also drives a low saturation-voltage driver connected to TACH OUT. The average value of the voltage on TACH OUT is directly proportional to motor speed, so that the pulse generator doubles as a simple tachometer.



Tachometer Doubles As Input Noise Gate

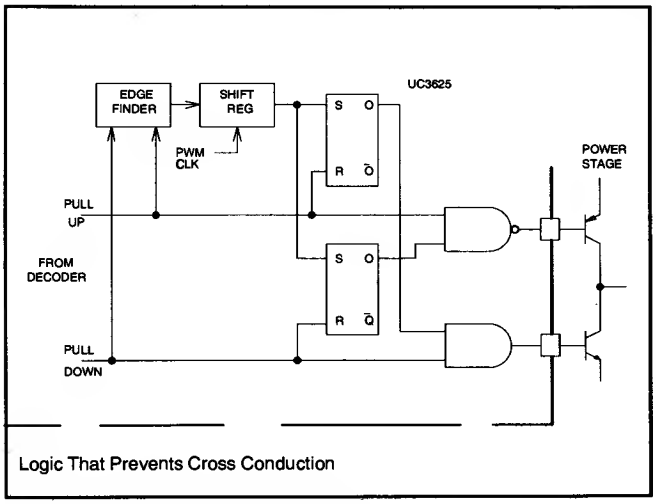
Even with input latches, external noise filtering is often valuable. Chopping noise lends itself to analog low-pass filtering because of its dominant high-frequency components. As high-frequency noise energy can be very strong, zener clamping ahead of the filter can be very effective.



Suggested External Non-Linear Filter For PWM Noise

Cross-Conduction Prevention

To further assure noise immunity, the UC3625 contains latches and a shift register to guarantee that all power stages turn off and remain off for a minimum time before changing states. In addition to preventing noise-induced cross conduction, this prevents cross conduction due to slow power stages.



Logic That Prevents Cross Conduction

The delay time is only inserted when an output is commanded from high to low or vice versa. During normal three phase commutation, outputs are turned off (opened) for a full cycle before changing states, so this delay will not impede normal operation. The only times that this delay will be inserted are during noise spikes, direction reversal, and braking.

Pulse-Width Modulation System

Motors perform better with higher operating voltages because for a given value of inductance, higher voltages can change winding current faster. A necessary adjunct to higher supply voltages is current control, either by linear amplifiers of pulse-width modulation (PWM). The UC3625 uses fixed frequency PWM for chopping.

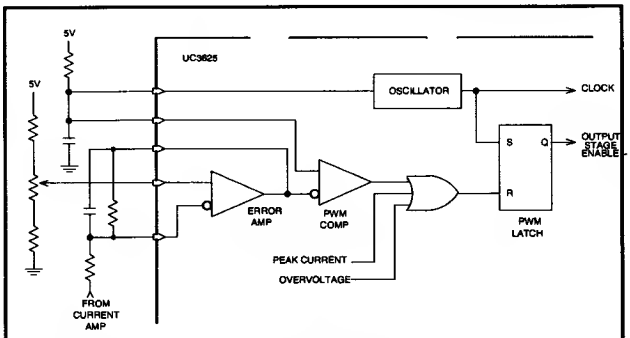
At the heart of the PWM is a sawtooth oscillator. The oscillator is programmed up to 500kHz with one resistor to the reference and one capacitor to the ground. This oscillator is used to enable the PWM latch every cycle, and also to clock the protection shift registers.

Another fundamental part of the PWM is the PWM latch. The output of this latch enables the power stages. The latch is set once per cycle by the oscillator, and cleared by either the PWM comparator, a peak current signal generated in current-sense circuitry, or by a fault signal from the OV/COAST input. This latch is reset dominant, meaning that a steady reset signal from any of three sources completely inhibits the power stages.

The other elements in the PWM are the PWM comparator and the error amplifier. The PWM comparator is an NPN-input comparator dedicated to comparing the output of the error amplifier to some other signal such as a command voltage, ramp, or sensed signal. The error amplifier is a PNP-input op-amp compensated for unity-gain operation, who's inputs can operate linearly down to ground.

The PWM can be configured into any number of different loops that regulate winding current (torque is nearly proportional to winding current), regulate speed, or regulate some other parameter. The PWM is internally configured for peak current control as well, although this is not intended to be the principle feedback loop.

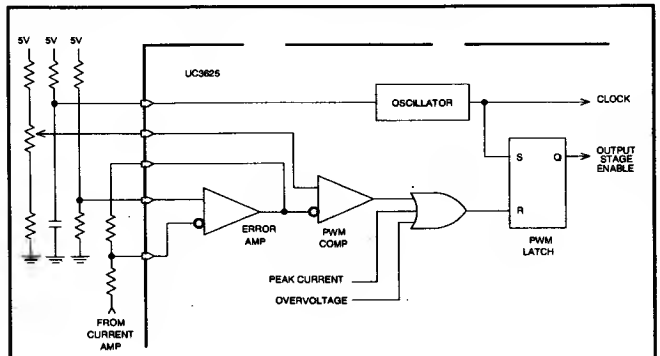
The approach above compares winding current to a DC voltage with the PWM comparator, and pulse-by-pulse regulates winding current. This is similar to "current mode" in PWM power-supply systems, and offers the advantage of removing the pole caused by load inductance from the feedback loop.



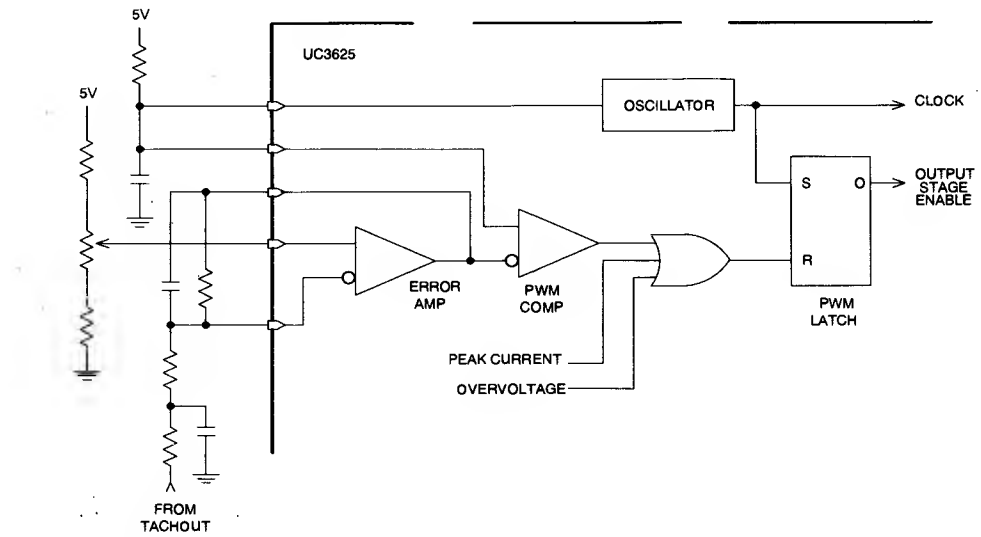
PWM Configured For Average Current Feedback

The PWM can also be configured to use the error amplifier to amplify the difference between the winding current and a desired current, and to use the PWM comparator to compare the error amp output to the oscillator ramp. This current loop operates on average, rather than peak current.

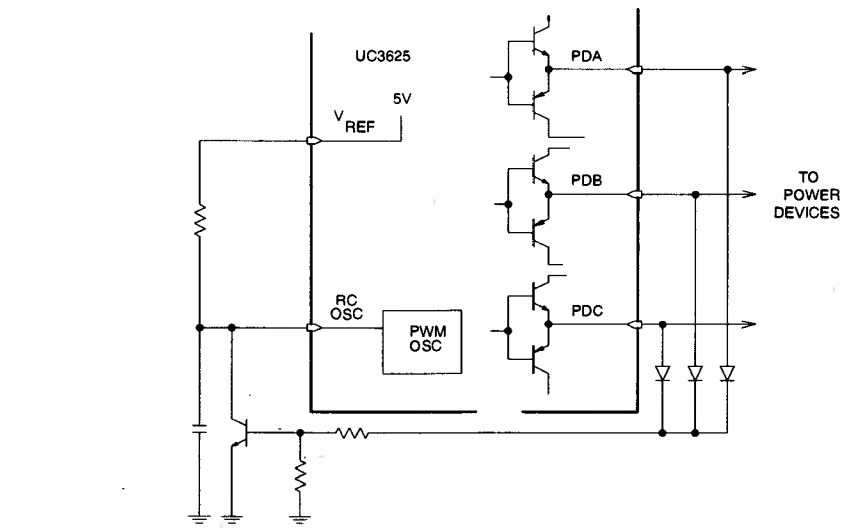
If the PWM comparator is used to compare the oscillator ramp to a DC voltage, then the load duty cycle is directly proportional to the applied DC voltage, as is the average load voltage. This "voltage mode" loop comes close to controlling speed because speed is nearly proportional to average winding voltage. If an overall speed feedback loop is required to regulate speed, this "voltage mode" topology can serve as a local feedback loop to make the system transfer function more linear, and the error amplifier can be used as the overall loop amplifier.



UC3625 PWM Block Diagram Configured For Pulse-By-Pulse Current Control



Voltage Mode Speed Control



Circuit For Fixed Off-Time PWM Using the UC3625

The advantages of each topology must be weighed considering complexity, overall stability, and sensitivity to load. In cases where current feedback seems nearly impossible to compensate, some compromise between currrent feedback and voltage feedback is dictated.

The PWM is also configurable to fixed off-time PWM rather than fixed frequency PWM by adding a few external components that couple the output off signal back into the oscillator.

Fixed off-time control is sometimes desirable because it uses one of the easiest feedback loops to compensate. Its main drawback is that the modulation frequency varies with load and speed. This means that for some loads chopping noise can become audible (below 20kHz). This also allows variation in the dead time inserted to prevent output stage cross conduction.

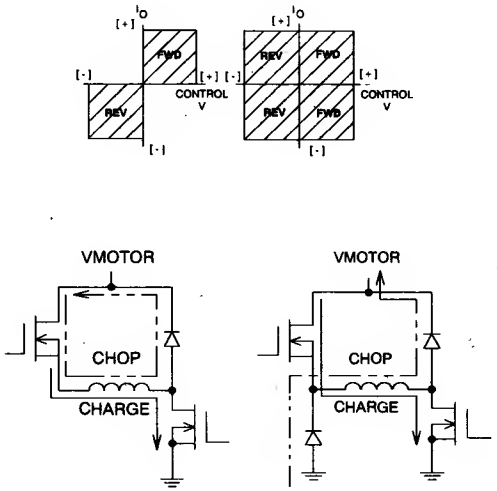
Different Chopping Techniques

Chopping capitalizes on the inductance of the load to maintain load current when the driving voltage is removed. The driving voltage is normally supplied through power switches, and diodes normally conduct across the load when the switches are opened.

Two different methods are common for chopping. The more efficient method chops one low-side power switch while one high-side switch is on. This is referred to as a two-quadrant PWM.

Two-quadrant PWM normally operates with a low duty cycle, as winding current is charged principally by the supply voltage, yet winding inductance is discharged by the voltage drop in the diode circuit (see figure below). Motor back EMF reduces the effective supply voltage and increases the effective diode voltage drop, so the duty cycle tends to increase with speed.

The main advantage of two-quadrant chopping is efficiency. Its main drawback is that it can't quickly decrease winding current. This can be very troublesome in position feedback systems.



Two-Quadrant vs. Four-Quadrant Chopping

In contrast, four-quadrant PWM systems chop both switches, and circulate load current through two diodes backwards into the supply.

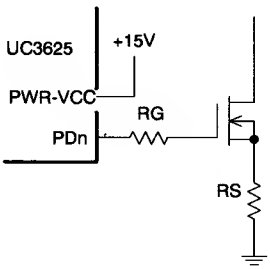
Again ignoring back EMF, four-quadrant chopping produces a nearly symmetrical current waveform, as current rises due to the supply voltage impressed on the load inductance, and decays due to reverse supply and load inductance. With four-quadrant chopping, a motor can decelerate as quickly as it can accelerate.

To program the UC3625 for one approach or the other, apply a logic signal to the QUAD SEL input. QUAD SEL can also be changed during operation to tailor performance to specific requirements.

Power Drivers

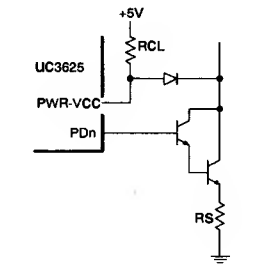
The overwhelmingly dominant power output device in new designs is the N-Channel Enhancement-Mode Power MOSFET. Bipolar power transistors and power darlingtons still have advantages in very high-voltage systems, but these advantages are being continuously eroded by developments in MOSFET structures and merged bipolar MOSFET devices. The UC3625 is able to drive both power MOSFETs and bipolar transistors.

The low-side drivers in the UC3625 are totem-poles capable of greater than 250mA peak gate or base current, but the package and the die are not constructed for continuous power dissipation greater than 1 watt, which imposes an upper limit on the available current for bipolar device drive.



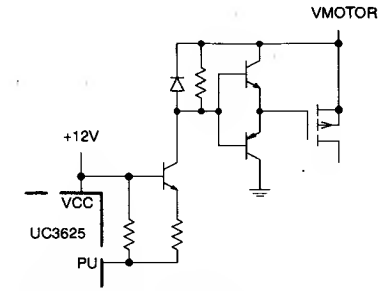
Driving Low-Side MOSFETs with the UC3625

The Power Vcc pin is separated from signal Vcc so that high gate current peaks can be isolated from signal Vcc, and also so that Power Vcc can be tailored to the power device. For fastest switching of power bipolar devices, the Power Vcc pin can be limited and clamped, as shown in this example.

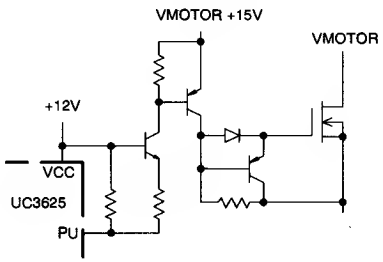


Driving Low-Side Darlingtons with the UC3625

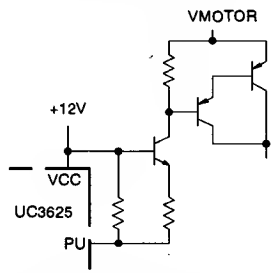
Driving high-side devices with the UC3625 requires level shifting if the motor supply is greater than 50V. The UC3625 high-side outputs are open collector NPN transistors which pull low to turn on high-side MOSFETs or bipolar transistors.



Driving High-Side P-MOSFETs



Driving High-Side N-MOSFETs



Driving High-Side PNP Darlingtons with the UC3625

Although capable of 50mA current sinking, the open collector outputs are normally operated with lower currents to minimize the power supplied by the high-voltage supply.

As a high-side switch, P-channel power MOSFETs are far easier to drive than N-Channel power MOSFETs because the gate of P-channel MOSFETS need not be pulled above the positive supply to obtain low voltage drop. Unfortunately, P-channel power MOSFETs are more expensive and less available than N-channel devices, so the added supply in the N-channel design is often justified.

Current Sense

The UC3625 contains a high-speed gain-of-two differential amplifier dedicated to current sensing. This amplifier can be connected directly across a low-value current-sense resistor or between two different current-sense resistors. Since the amplifier common mode range allows operation one volt below ground, the amplifier has excellent common-mode noise rejection.

The current-sense amplifier also embodies an ideal diode that performs absolute value and level shifting of the input, giving a transfer function of:

$$Vo = 2.5 + 2\ ABS\ (Vi_2 - Vi_1)$$

If the low-side power devices and the lower catch diodes are returned to the same current-sense resistor, and the UC3625 is chopping in four-quadrant mode, then the winding current always flows through the current-sense resistor. The voltage on the current-sense resistor flips polarity every time the PWM chops, but the absolute value current-sense amplifier rectifies this, giving a smoother representation of continuous winding current, and requiring less filtering.

Some filtering of the current-sense signal is always required, however, and the output of the current-sense amplifier is the best place to filter. The amplifier is stable with all capacitive loads, and has approximately 250 ohms output impedance.

Filtering at the input of the current-sense amplifier is also valuable to remove spikes that are faster than the amplifier can track. However, to insure that the absolute value circuit continuously trecks current, use only a minimal amount of input filtering.

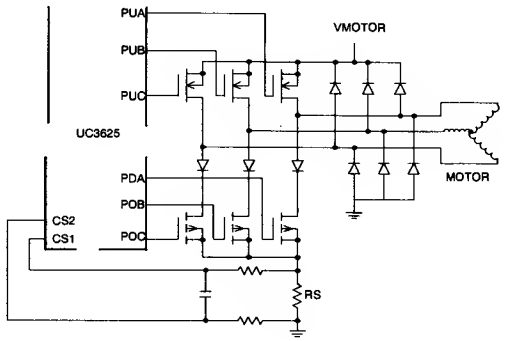
The output of the current emplifier drives two comparators through the filtering resistor: the peak current comparator and the overcurrent comparator. The peak current comparator resets the PWM latch whenever the current-sense voltage exceeds approximately 200mV. The overcurrent comparator initiates soft start if the current-sense voltage exceeds approximately 300mV.

The peak current comparator can be used to limit maximum peak winding current while e lerger feedback loop limits winding current to control some other parameter, such as speed or position. The overcurrent comparator then functions as a fail-safe device that commands SOFT START if the peak current loop loses control, as might heppen if a power device becomes shorted.

Is it Brake...or Break?

The UC3625 contains provisions for braking by way of a multifunction pin called "RC / BRAKE". This pin also serves es the timing pin for the internal tachometer, pulsing between 1.67V and 3.33V every time the position sensors commutate. To commend BRAKE, pull RC/BRAKE low with an open collector gate or switch. The tachometer then stops pulsing and all three low-side drivers turn on.

Normal PWM configurations do not allow braking current to be modulated because the braking current does not normally flow through the sense resistor. The motor control circuit below includes three added diodes that, during BRAKE and all other circumstances ceuses winding current to flow through the sense resistor. Using this circuit, the UC3625 stops e motor as fast es the peak limit current setting allows and protects the output power devices and the motor.



Circuit For Safe Braking Series diodes guarantee that braking current will flow in the current-sense resistor

Direction Reversal is Worse

As with braking, direction reversal can also force excessive current into power devices if not checked. Direction reversal forces two of the three driver channels to go from high to low or low to high directly. With the UC3625, cross conduction is completely prevented, but high winding current is dependent upon the application. The higher the speed, the higher back EMF, and the higher the potential peak current.

The approach mentioned for braking also limits peak winding current during direction reversal. In addition, the direction latch and shift register in the UC3625 can be configured to prevent direction reversal until motor speed drops to a safe level. This latch also commands COAST whenever a direction reversal is commanded and motor speed is too high.

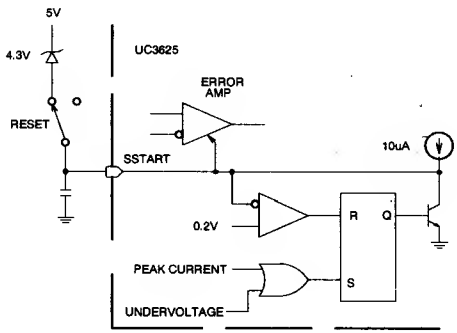
The easiest way to configure this protection is using the internal tachometer to drive "SPEED IN" through a low-pass RC filter. The "SPEED IN" threshold is set to prevent reversal whenever input voltage exceeds approximately 250mV.

Other Protection Features

To prevent confusion or insufficient drive to power MOSFETs, the UC3625 contains a comparator to lock off all six outputs until the Vcc input exceeds 9V, called under-voltage lock-out. The UC3625 also contains an uncommitted comparator that inhibits the outputs and clears the PWM latch whenever its input exceeds 1.75V. This can be used with a voltage divider for an over-voltage inhibit, or can be directly driven from TTL or CMOS for a logic controlled COAST input.

To prevent very high power supply current spikes and to limit average current during faults, the UC3625 contains latched soft start. The latch is set by low power-supply voltage or overcurrent fault, and is only cleared when the setting condition goes away and the soft start input discharges to below approximately 200mV.

Normally, the UC3625 is configured with a capacitor from soft start to ground, which is charged by the soft start 10uA current source. The UC3625 can also be configured to latch soft start until cleared by connecting a 4.3 volt zener and a normallly closed switch from Vref to soft start. The switch then functions as a reset switch.



Manual Fault Reset Circuit Uses Zener Diode to Latch Faults

Voltage Reference

Finally, the UC3625 contains a precision voltage reference trimmed to 5V +/- 2%. This reference powers most of the internal circuitry for supply rejection and is available on the "Vref" pin for driving other circuitry such as Hall-effect position sensors and bias circuits. Operation of the voltage reference is guaranteed with loads up to 30mA, and the reference is also short circuit current limited to approximately 100mA.

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A NEW LINEAR REGULATOR FEATURES SWITCH MODE OVERCURRENT PROTECTION

Robert Mammano and Jonathan Radovsky, Unitrode IC Corp; and
George Harlan, Power General

ABSTRACT

This paper presents a new linear control circuit which, in addition to offering benefits such as low input-out-put differential and a precise reference voltage, features a unique and innovative approach to overload protection. By using duty-ratio, switch-mode protection, this circuit eliminates both the high internal dissipation of constant current limiting and the latch-up tendencies of limiting with current foldback.

THE CURRENT LIMIT PROBLEM

As an opening statement, let us offer as a "given" that all linear power supplies need some form of over-current protection. Traditionally, this protection consists of configuring supply to control current - rather than output voltage - once an established threshold of maximum current has been exceeded. The method of current control can usually be classified as either "constant-current" or "current-foldback" current limiting and, while simple to classify, choosing between these two methods is often less than satisfying.

The protective method most acceptable to the user is constant current limiting with a characteristic as shown in Figure 1. With the knowledge that a power supply will only deliver a maximum current regardless of what he might do to it, the user's job of scaling his cables, switches, connectors, and other components associated with the power inputs to his system is greatly eased. He knows that no matter how non-linear his load may be, he can count on a regulated voltage whenever his current drain is within the supply's rating. Further, he knows that the maximum rated current is always available to meet any demand asked of the supply.

The "benefits" of constant current limiting are another matter to the power supply designer, however. For example, a regulator designed to deliver 12 Volts at a maximum load current of 5 Amps, would probably start with a bulk input voltage of approximately 15 Volts and a constant current limit of 5.5 Amps. Under maximum rated load, the internal dissipation of the regulator is 3V x 5A or 15 watts but with a short to ground, this dissipation jumps to 15V x 5.5A or more than 80 Watts! This means that the thermal management and heat sinking must be sized for the short circuit condition resulting in a massive overkill in terms of volume, complexity, and cost with respect to normal operating conditions.

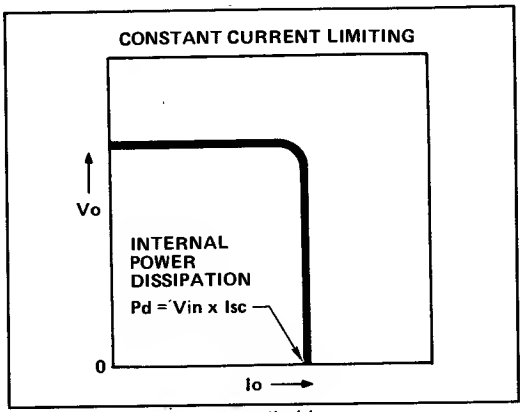


Figure 1: Constant current limiting.

A common solution to this problem is to design a current limiting scheme as illustrated in Figure 2. Here the protection is actuated at 5.5 Amps when the output voltage is at 12 Volts but the allowable current then "folds back" as the output voltage falls due to increasing overload, until it reaches some much lower value - say one Amp in this example - with a shortened output. Now the dissipation with a short circuit is close to the same as it was with rated current and our designer's thermal problems are solved.

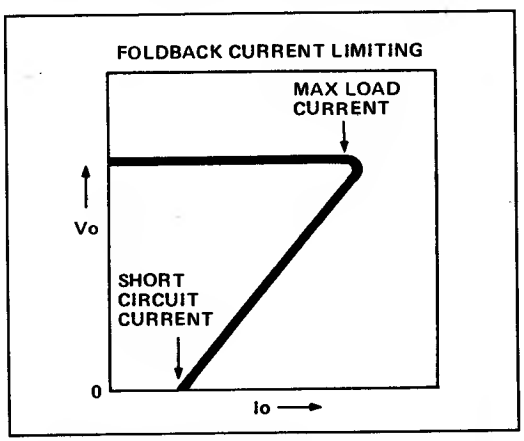


Figure 2: Foldback current limiting

Minidip package allows the potential for meeting the cost objective (plus the benefit of less PC board area), but in several important ways, also restricts the device's versatility. Recognizing this fact led to the introduction of the same chip in a 14-pin package with a UC1832 designation. The block diagram of this device, in a uA723-type application, is shown in Figure 8.

The characteristics of the UC1832 include all the performance features of the UC1833 plus the following:

1. Separating the +Vin line from the CS+ terminal so that the controller could be supplied from a higher potential, low-current, auxiliary voltage while sensing current from the main supply.

2. Separating the Reference from the Error Amplifier (+) input and making both accessible to the user. Among other things, this allows phase reversal, an external or divided-down reference, and a convenient access point for soft-start.

3. Providing a separate input to the Driver's local current limiter allows considerable flexibility in setting that limit either higher or lower than the 300 mA (typical) defined by the internal 2.4 ohm resistor.

4. A separate logic-level digital shutdown function has been added to give more programming options such as accepting a shutdown command from an over-voltage sensor or implementing a turn-on delay. This input is fail-safe as it must be pulled low to allow the regulator to turn on.

5. Allowing the input offset of the current sense amplifier to be programed with an external voltage on the V_{ADJ} terminal, normally provided by a voltage divider form V_{REF}. With V_{ADJ} high or open, the offset is 130 ON V, equivalent to the UC1833. When V_{ADJ} = 0, the offset is increased to 300mV, allowing a much higher current limit level. A capacitor on this pin can be used to provide higher peak currents at turn on but lower levels for faults which occur later.

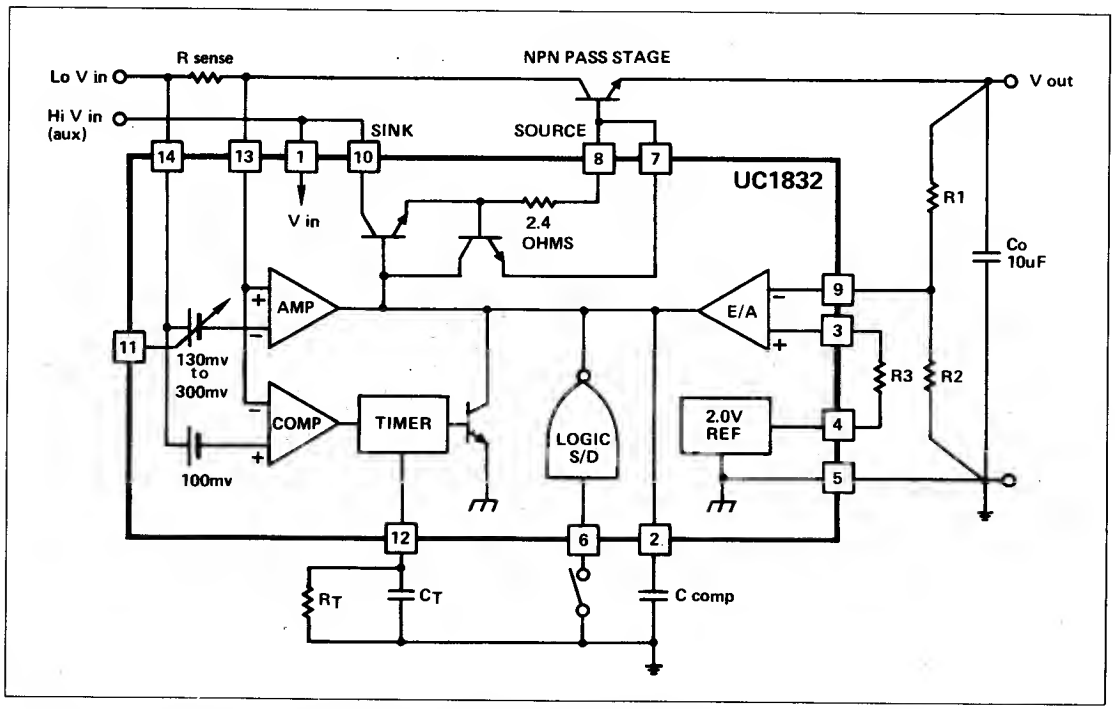


Figure 8: A 14-pin version, designated UC1832 / UC3832, offers enhanced versatility.

Timing waveforms during an overload cycle are shown in Figure 7 where the upper graph shows the output current from the regulator, the center one plots the voltage on the timing components, and the regulator's output voltage is shown in the lower graph. Following the sequence of events as drawn in the figure, when the load current ramps up and crosses the 100 mV Comparator threshold, the initial ON time begins. This initial period is about twice the duration of successive ON-times as the timing capacitor starts its charge from zero initially, while subsequent ramps begin from the lower Comparator threshold. While the timing capacitor is charging, the regulator current is limited by the action of the Current-sense Amplifier to maintain a level of 130 mV across the sense resistor. While in current limiting, the regulator's output voltage falls to whatever value that current will allow across the faulted load impedance.

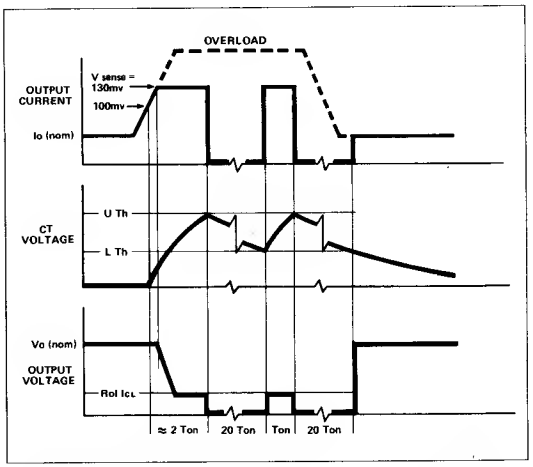


Figure 7: Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

The ON-time continues until the internal 10k resistor charges the timing capacitor to the upper Timer threshold. At this point, both the ON-time of the regulator and the charging of the timing capacitor are terminated, and the capacitor now discharges through RT, while the regulator is held OFF until the voltage on CT reaches the lower threshold, at which point the cycle repeats. If the load fault is removed during an ON-time, the Timer is immeadiatly disabled allowing the regulator to recover and the timing capacitor to discharge back to zero. If the fault is removed during an OFF-time, the Timer must complete that cycle of capacitor discharge before allowing the regulator to turn back on. In special applications requiring an extended ON-time, the correspondingly long recovery may be accelerated by interrupting the input voltage, as the falling internal 5 V source will discharge CT through D1 and an equivalent 1k impedance.

Duty-ratio protection has greatly eased the problem of heat sinking created with a constant-current solution since the area of the heat sink, or its thermal resistance, need only remove the average power as reduced by the duty ratio. Heat sinks for the internal power devices must now only have adequate thermal mass to absorb the high peak power of the initial ON period.

REMAINING CONTROL CIRCUITRY

Other blocks within the UC1833 include a 2.0 Volt band-gap reference internally trimmed to 1% and a low input-offset Operational Transconductance Amplifier (OTA) to serve as the error sensing and amplifying circuitry. The OTA Error Amplifier has a gm of about 4 millimho and an output current capability of +/- 300 uA. This form of amplifier can usually be compensated with a simple network - often a single capacitor - from its output to ground; but more commonly, an R-C pole-zero pair is also added to compensate for an external PNP pass transistor's gain characteristics.

The Error Amplifier is followed by a unity-gain Buffer Amplifier which controls the Driver Stage consisting of a Darlington transistor pair with local current limiting. This Driver can either source or sink current, allowing its use as a driver for either NPN or PNP pass transistors. The Pullup and Pulldown current-sources shown at the Sink and Source terminals of Figure 6 are to provide turn-off bias to the pass transistor during duty-ratio switching so that it is not turned off into a BV_{CEO} condition.

Not shown on the schematic are two additional forms of protection built into the UC1833: Thermal Shutdown (TSD), and Under Voltage Lockout (UVLO). While it could be argued that thermal protection on the control chip does nothing to protect the pass transistor, the fact that the Driver can conduct up to at least 100 mA with a large portion of the input supply voltage across it, can result in more than acceptable internal heating of the UC1833. A good practice, when voltage levels permit, is the addition of an external resistor in series with either the Source or Sink outputs of the Driver to remove some of the voltage - and therefore some of the dissipation - from the controller.

Under Voltage Lockout keeps the Error Amplifier output low until the supply voltage reaches approximately 4 Volts insuring that all internal circuits - particularly current limiting functions - are intelligent before allowing the pass transistor to turn on. The UVLO function also disables the Pullup current feeding into the Sink terminal, for low input voltages, so that the pass transistor cannot be driven in the reverse direction should the input supply fall with a charged capacitor or other energy source on the output. The Source Pulldown current source is also disabled with UVLO but this terminal also has a two-diode path from the Source to the Compensation terminals. This is to allow any shutdown function which pulls the Comp pin low to discharge capacitance at the regulator's output without reverse-biasing the Driver's emitter-base junction.

THE UC1832 14-PIN CONTROLLER

An important objective in the design of the UC1833 was that in addition to providing significant operating benefits over the omnipresent uA723, the resulting product should be cost-competitive with that device. Committing the UC1833 to an 8-pin

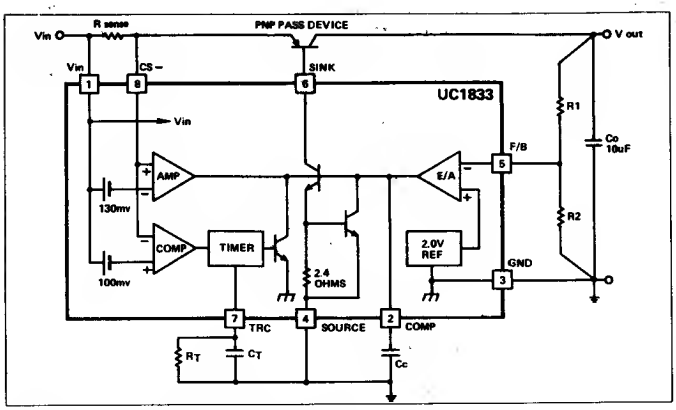


Figure 5: The new UC1833 / UC3833 linear regulator.

The Amplifier part of the current sense circuitry has an input threshold of 130 mV and overrides the output of the Error Amplifier to control the driver - when enabled by the ON-time of the timer - to regulate the supply's output current to a maximum amount determined by 130 mV divided by the value of the sense resistor. The 30 mV differential between the thresholds of the Amplifier and Comparator insures that current limiting can never occur without prior initiation of the timer.

OVERLOAD PROTECTION CIRCUITRY

The operation of the overload protection circuitry can be better understood by referring to the simplified schematic of Figure 6.

The current sensing portion of this circuit is to the left of this figure where the current-sense Comparator and Amplifier are shown sharing the same input sense pins. Note that their offset voltages are derived by a constant current through R1 and R2 in series rather than independently as shown in the more simplified earlier block diagram. By adding 30 mV to the 100 mV offset of the Comparator, the Amplifier's offset will more accurately track that of the Comparator should any variations occur, and the criteria to have the Comparator always activate first is assured.

A characteristic important to current protection is the accuracy of its threshold as any tolerance represents a window of undefined operation which works to the disadvantage of both designer and user of the power supply. Recognizing this, the UC1833's thresholds are derived from its precision reference resulting in a Timer activation threshold guaranteed to 5 percent over all operating conditions.

The output of the Current Amplifier connects into the output stage of the Error Amplifier where it can easily take command when activated. The compensation capacitor must compensate both the voltage and current feedback loops, and since the current loop must override the voltage control, its gain will be higher making the current loop the more difficult to stabilize. To evaluate the current loop, grounding the Timing pin will disable the Timer and allow continuous constant current operation. This can be useful either as a temporary measure while designing the current compensation network, or permanently to implement a constant-current limited power supply.

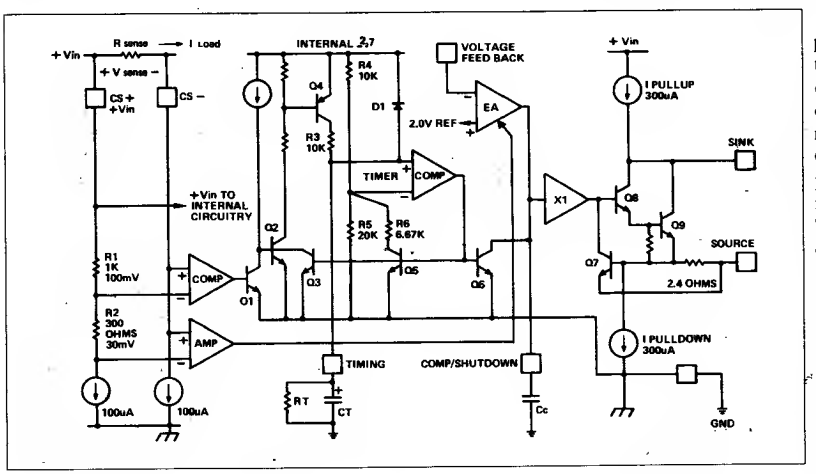


Figure 6: A simplified schematic of the UC1833 control circuitry.

The Current Sense Comparator is phased such that its activation turns off Q1 which turns on Q2 and Q4 to start the timing cycle. The timer is a gated astable relaxation oscillator with ON and OFF times independently programmed using an external resistor and capacitor, RT and CT. The external components work in conjunction with an internally switched 10k timing resistor shown in the schematic as R3. With RT much greater than 10k, the ON time is defined by R3 and CT, while RT and CT determine the OFF time. The thresholds for the Timing Comparator are set at 1/3 and 2/3 of the internally regulated 2.7V source by the values of R4, R5, and R6.

9

But what about his customer? His load may be complex, nonlinear, and often not even well understood. Figure 3 shows typical load characteristics for digital and analog circuitry but an actual system may include all of these plus motors which need to be started and capacitors which need to be charged. Any protection scheme which allows the static load line to intersect the foldback current curve as shown in Figure 4 is potentially subject to latch up because the load draws more current than the regulator can supply at the voltage where the curves cross.

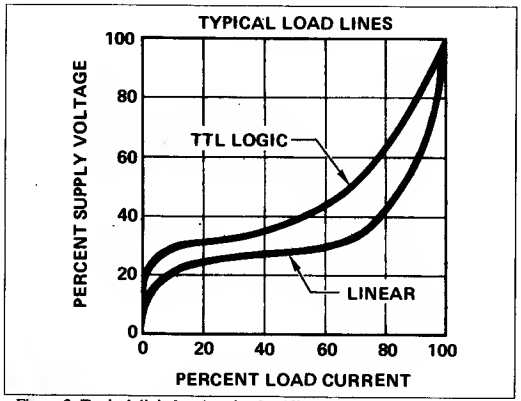


Figure 3: Typical digital and analog load lines.

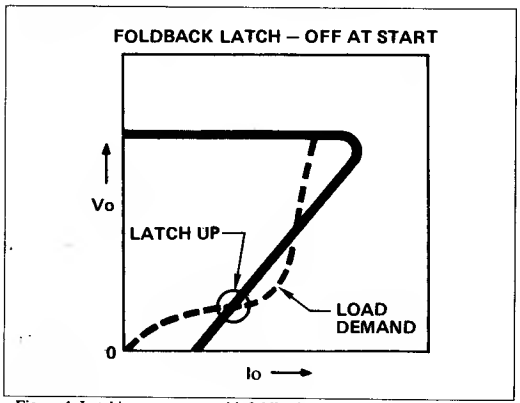


Figure 4: Latching at start-up with foldback.

An application particularly susceptible to latch up due to foldback current limiting occurs when two supplies are used to provide positive and negative voltages to a load where there is a path for "rail-to-rail" loading. As the regulators turn on, their output capacitors are charged at rates determined by the values of the capacitors and the amount of current each regulator can provide as its output rises up the foldback curve. Since these curves are unlikely to be perfectly matched, one output will dominate the other. As the faster one's output voltage increases, it provides more current through the common load. This forces the slower one back down the foldback curve where it provides less current, compounding the problem and ultimately latching when its output is driven past zero to a reversed polarity. Thus a foldback-limited regulator, which might be stable when used by itself, may latch when used as one-half of a dual-polarity system due to this "turn-on slew rate" phenomenon.

So what we have concluded is that while the power supply designer needs to incorporate foldback current limiting to reduce power dissipation, his customer needs constant-current limiting to insure reliable starting. It is the contention of this paper that what they both really need is duty-ratio protection.

DUTY-RATIO OVERCURRENT PROTECTION

Duty-ratio protection can be simply described as a constant current limiting regulator with a timer. The timer's function is to turn the regulator's power stage OFF and ON with an established duty cycle ratio such that the high internal power dissipation of constant current limiting is reduced by the duty ratio to a much more manageable average value.

Referring back to our earlier example of a 12V, 5A regulator, consider setting the constant current limit at 5.5 amps but additionally establish a duty ratio for the timer at 1 to 20 for "ON" to "OFF". If we set the "ON" time sufficiently long to charge whatever capacitance might be on the output, the regulator will power up with the constant current characteristic, insuring start-up regardless of the loading. In the event of an overload or short circuit (defined in this device as remaining in current limiting for a period of approximately 2 x Ton), the regulator will periodically shut down for a time equal to 20 x Ton and then continue to cycle in a 1 to 20 duty cycle until the fault is removed. Although the peak power during Ton might be 80 Watts, the average fault dissipation at this duty ratio is only 4 Watts - less than the normal 15 watt operating power loss, and we have thereby satisfied both the designer and his customer.

INTRODUCING THE UC1833 / UC3833

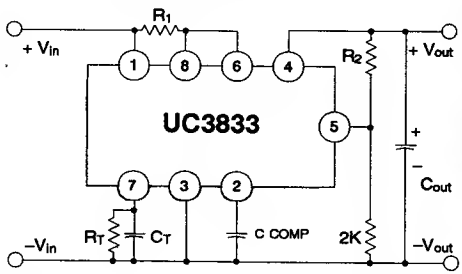
The block diagram of this new linear regulator control IC is shown in Figure 5. This circuit can be used in many different ways but its primary intent is as a high-efficiency regulator implemented with an external PNP pass transistor as shown in the figure. The circuitry in the right half of the UC1833 block generates the voltage error signal used to activate an NPN Darlington driver which, in turn, drives the base of the PNP pass device. This common-emitter pass transistor configuration allows this type of regulator to operate with a minimum input-output differential of well less than one Volt, even at high loads.

Duty-cycle current limiting is accomplished with the circuitry on the left half of the block diagram, where an Amplifier and a Comparator are seen, both monitoring the voltage drop across a single current sense resistor. The Comparator has an input threshold of 100 mV and, when activated, initiates a timer to alternately clamp and release the base of the driver to ground thereby switching the output of the regulator from Vout to Zero with a low duty ratio.

UC3833 Typical Applications

See appendix for component selection

LOW CURRENT APPLICATION
using the UC3833 internal drive transistor

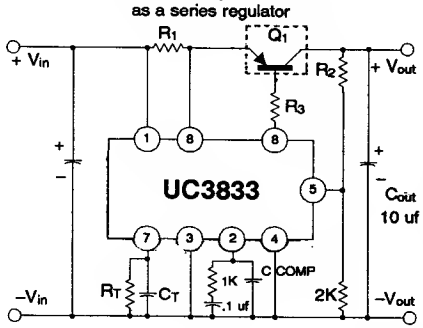


TYPICAL OUTPUT CURRENT vs. V_{In} and V_{out}
of the UC3833 internal drive transistor
for P_{diss} = 0.5 W (approx.)

		V_{In}					
	Volts	5	9	12	15	18	24
Vout	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

Fig. 3

LINEAR REGULATOR
using an external power transistor
as a series regulator



P CHANNEL POWER MOSFETs
can also be used as the series pass transistor Q_1

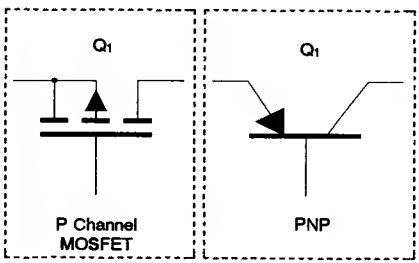
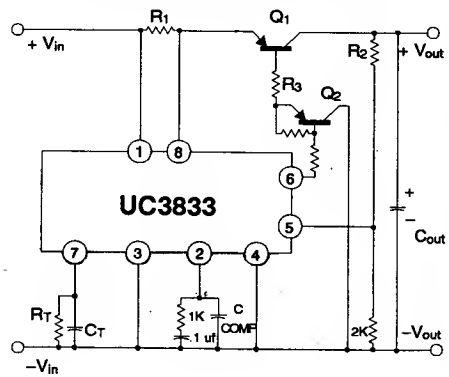


Fig. 4

HIGH CURRENT REGULATOR
using drive transistor Q_2 to increase Q_1 base drive
and reduce UC3833 power dissipation



PARALLEL PASS TRANSISTORS
can be added for high current
or high power dissipation applications

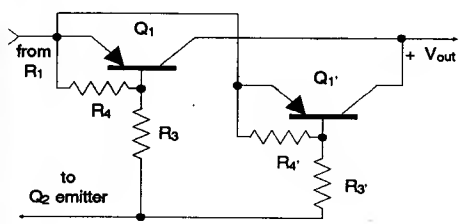


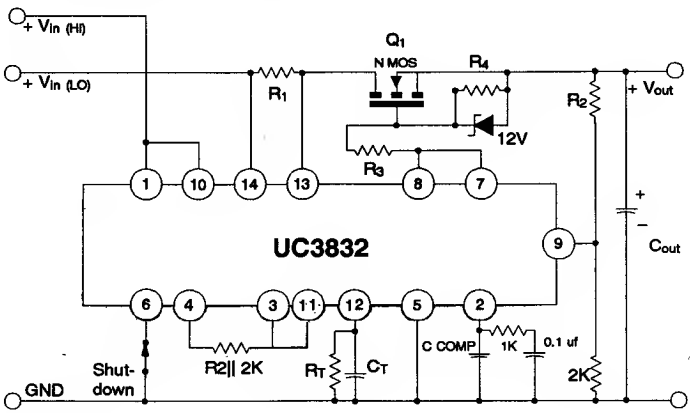
Fig.5

UC3832 Applications

See appendix for component selection

LOW DROPOUT REGULATOR

Tha UC3832 features a seperate supply input for operation from an auxiliary power source. Useful in low dropout applications.

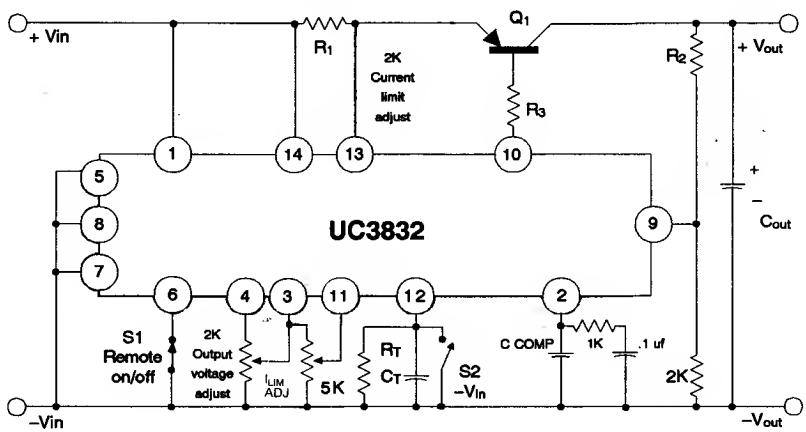


S1 - Closed: Normal operation
Open: Output disable

Fig. 6

PRECISION LABORATORY POWER SUPPLY

featuring adjustable voltage and currant limiting



S1 - Closed: Normal operation
Open: Output disable

S2 - Open: Duty ratio current limit
Closed: Constant current output
or I_{MAX} adjust.

Fig. 7

APPENDIX

Design Equations and Component Selection

R_1 - Current Sense Resistor

R1 = 0.135 V/I_{OUT} (max) UC1833 AND 1832 WITH V_{ADJ} = 2.5V

LOW CURRENT	
I_{OUT} mA	R_1 ohms
10	13
20	6.5
30	4.3
40	3.3
50	2.7
60	2.2
70	1.8
80	1.6
90	1.5

GENERAL USE	
I_{OUT} A	R_1 ohms
0.10	1.30
0.25	0.52
0.50	0.27
0.75	0.17
1.0	0.13
2.0	0.065
3.0	0.043
4.0	0.032
5.0	0.026

HIGH CURRENT	
I_{OUT} A	R_1 mohm
5	26
6	21
7	18
8	16
9	14
10	13
15	8.6
20	6.5
25	5.2

R_2 - Output Voltage Divider Resistor

$R_2 = (V_{OUT} - 2.0V)/1mA$

FIXED	
V_{OUT}	R_2
5.0	3.0K
9.0	7.0K
12.0	10K
15.0	13K
18.0	16K
24.0	22K

ADJUSTABLE	
$V_{OUT(MAX)}$	R_2
7.0	5K POT
12	10K POT
22	20K POT

R_3 - Drive Current Limit Resistor

$R_3 = ((V_{in} - V_{BE} - V_{sat}) * \text{Beta (min)})/I_{OUT}$ (max)

I_{OUT}	V_{in}		
A	9V	15V	24V
0.10	1.8K	3.2K	5.6K
0.25	680	1.2K	2.2K
0.50	330	650	1.1K
0.75	220	430	750
1.0	180	330	560
2.0	82	160	270
3.0	57	100	180
4.0	43	82	120

For circuit diagram of Fig. 4,
Beta (min) = 25, V_{BE} = 0.7V, V_{SAT} = 1.5V

I_{OUT}	V_{in}		
A	9V	15V	24V
1.0	200	350	560
2.0	100	175	270
4.0	50	87	140
5.0	40	70	110
7.5	27	47	75
10.0	20	35	57
15.0	13	24	38
20.0	10	17	27

For circuit diagram of Fig. 5,
Beta (min) = 25, V_{BE} = 0.7V,
$V_{SAT} \approx V_{BE}(Q_2) + V_{SAT}$ (UC3833) $\approx$ 1.5V

9

R_T and C_T - Timer Duty Duration and Ratio Resistor and Capacitor

$T_{on} = 0.693 * 10K * C_T$

$T_{off} = 0.693 * R_T * C_T$

Duty Ratio = $T_{on}/(T_{on} + T_{off}) = 10K/(10K + R_T)$

NOTE: Typical duty ratios are between 0.5% and 5%

Duty Ratio	R_T ohms
5%	180K
4%	240K
3%	330K
2%	470K
1%	1 MEG
0.5%	2 MEG

T_{on} msec	C_T* uf
1	0.15
2	0.30
5	0.68
10	0.15
20	3.0
50	6.8
75	10
100	15

T_{on} sec	C_T* uf
0.1	15
0.2	30
0.5	68
1.0	150
2.0	300
5.0	680
7.5	1000
10.0	1500

* Timing capacitor C_T should have extremely low leakage current.

Q1 - Pass Transistor

I_{OUT} A	PNP Transistor	P Channel MOSFET	N Channel MOSFET
< 1.0	TIP30 D41D4	IRF9511 RFP5P12	IRF511
2.5	TIP32,34 D45C2	IRF9521 RFP6P08	IRF521
5.0	D45H5,8 MJE6040	IRF9531 RFP12P08	IRF531 IRFZ10
7.5	TIP36 2N6666*	IRF9541	IRF541 IRFZ20
10.0	TIP36,145* 2N6648*	IRF9541 RFK25P08	IRF540 IRFZ20
15.0		IRF9Z30 RFK25P08	IRFZ30
20.0	2N6285*	RFK25P08	IRFZ40

* Darlington transistor

A higher power application is shown in the schematic of Figure 10 which was designed to supply 5 Volts at 5 Amps. The UC3833, configured as shown, will meet this requirement with an input voltage as low as 6 Volts due to the low saturation voltage of the paralleled 2N6489 transistors and the fact that the maximum non-fault voltage on the sense resistor is less than 100 mV. Actually, a little more sense voltage was sacrificed in the interests of selecting a standard resistor value, with the excess divided down by the 56/100 ohm divider. The additional BD438 drive transistor was added to boost the UC3833 drive current and keep the internal power dissipation low.

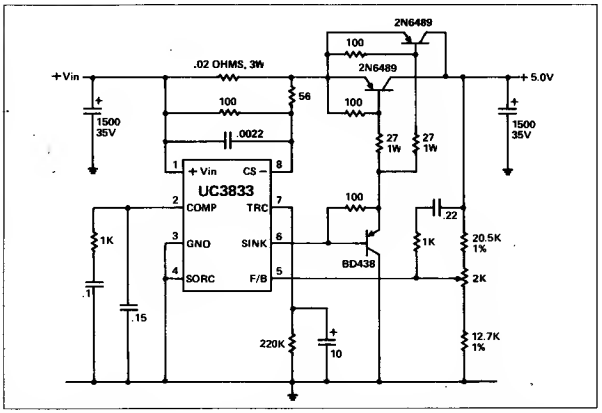


Figure 10: A high-efficiency configuration with added current boost will deliver 5V at 5A from a 6V source.

A third application of the UC3833 is one which took particular benefit from duty-cycle current limiting. This was for a disk drive power supply which required considerable current at turn-on to accelerate the disk. The circuit schematic is the same as that shown in Figure 10 with the voltage sense resistors selected for a 12 Volt output. The power requirements dictated a peak start current of 5 Amps decaying to 3 Amps in 30 seconds as the motor reached operating velocity. The current sense resistor was chosen to give a Timer initiation at 4.75 A and a constant current limit of 6.1 Amps. The timing capacitor value was set at 3300 uF yielding an ON-time of approximately 20 seconds, with 40 seconds for the initial turn on period - during which time the motor current will decrease to less than the lower threshold. With a duty-ratio of 20:1, when a fault does occur, the OFF-time will now be greater than 6 minutes, but, if this is excessive, recycling the input voltage to the regulator will reset the timing capacitor.

CONCLUSION

While no one can deny the long-term success of the uA723 as a general-purpose linear regulator controller, there has also long been a call for a device to improve its many limitations. While other products have been marketed offering some parametric improvements, the UC1833 - and its companion UC1832 - are the first to offer an innovative solution to a very basic problem. By combining switch-mode protection with linear regulation, these devices answer the question of which form of protection is best for whom, with a solution that is best for everyone.

9

UC1860 – NEW IC CONTROLS RESONANT MODE POWER CIRCUITS

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ABSTRACT

A new integrated circuit, the UC1860, is introduced. Its prime purpose is to provide the control function in resonant mode power supplies operating at frequencies up to 3 MHz. A frequency modulated, fixed on-time control scheme is implemented. Additional features include a programmable under voltage lockout circuit and a programmable soft-start/hic-up circuit.

BACKGROUND

For years, rumblings of the coming (or perhaps more correctly, reapplication) of resonance as a useful tool in the power control world have been growing progressively louder. Being a recognized manufacturer of pulse width modulation control ICs, some of these noises have been focused directly at Unitrode Integrated Circuits Corporation. Receiving, conditioning, filtering, and discriminating these signals, however, has been somewhat of a frustrating chore. Information indeed has been sought to aid in the definition of chip to perform all required resonant mode control functions. Too often the response was an inverse request: "Tell me what the chip looks like and then I can design my power supply." The immaturity of the technology has naturally made the sharing of information somewhat less than authorative. Finally there came a day when a best guess architecture and specification goals list had to be embraced as presumed gospel. It is that choice that has resulted in the chip to be discussed in this paper.

This paper, then, will describe the UC1860 with respect to its architecture and the specific features and performance of some of the sections. The chip is intended to fully implement all features necessary for the control function in a resonant mode power supply.

BLOCK DIAGRAM

The UC1860 control IC is designed to control power conversion circuits requiring frequency modulated fixed pulse widths such as resonant or quasi-resonant mode power supplies (figure 1).

The central section of the system is composed of 6 main blocks. A precision reference is provided for the error amplifier. These serve as the basis to control a variable frequency oscillator (VFO) which in turn triggers a one-shot. The programmable one-shot determines the output pulse width of the output drivers which are specifically designed to drive power mosfet gates. Finally a toggle flip flop steers the one-shot signal to the appropriate output stage.

In a typical application, the error amplifier is used to compare power supply output voltage to the internal reference. The error amplifier is also used as a gain block with which to compensate the overall power supply control loop. The output of the amplifier is resistively coupled to the VFO to control frequency. VFO frequency is directly proportional to error amplifier output voltage. Output pulse width is selected by an external RC pair. Pulses are sequenced to the output pins to activate the switches in the power circuit.

On chip peripheral housekeeping blocks are under voltage lockout (UVLO), fault management, and start-up/restart sequencing. The UVLO block forces the chip to wake up in a consistent and intelligent state when power is applied.

An additional uncommitted open collector comparator is on chip. This comparator can be used to accomplish a host of user defined functions.

ERROR AMPLIFIER

Understanding the chip requires considering the blocks one by one. The first block of interest in the main control section of the chip is the error amplifier. This amplifier is a high bandwidth, low offset, clamped swing design (figure 2). The non-inverting input is internally connected to a resistive divider from the reference voltage. While the divider is set for 3V, the combination of offset voltage and divider accuracy is specified as a ratio of the reference voltage. This allows an external reference of greater accuracy to drive the chip reference for better system accuracy.

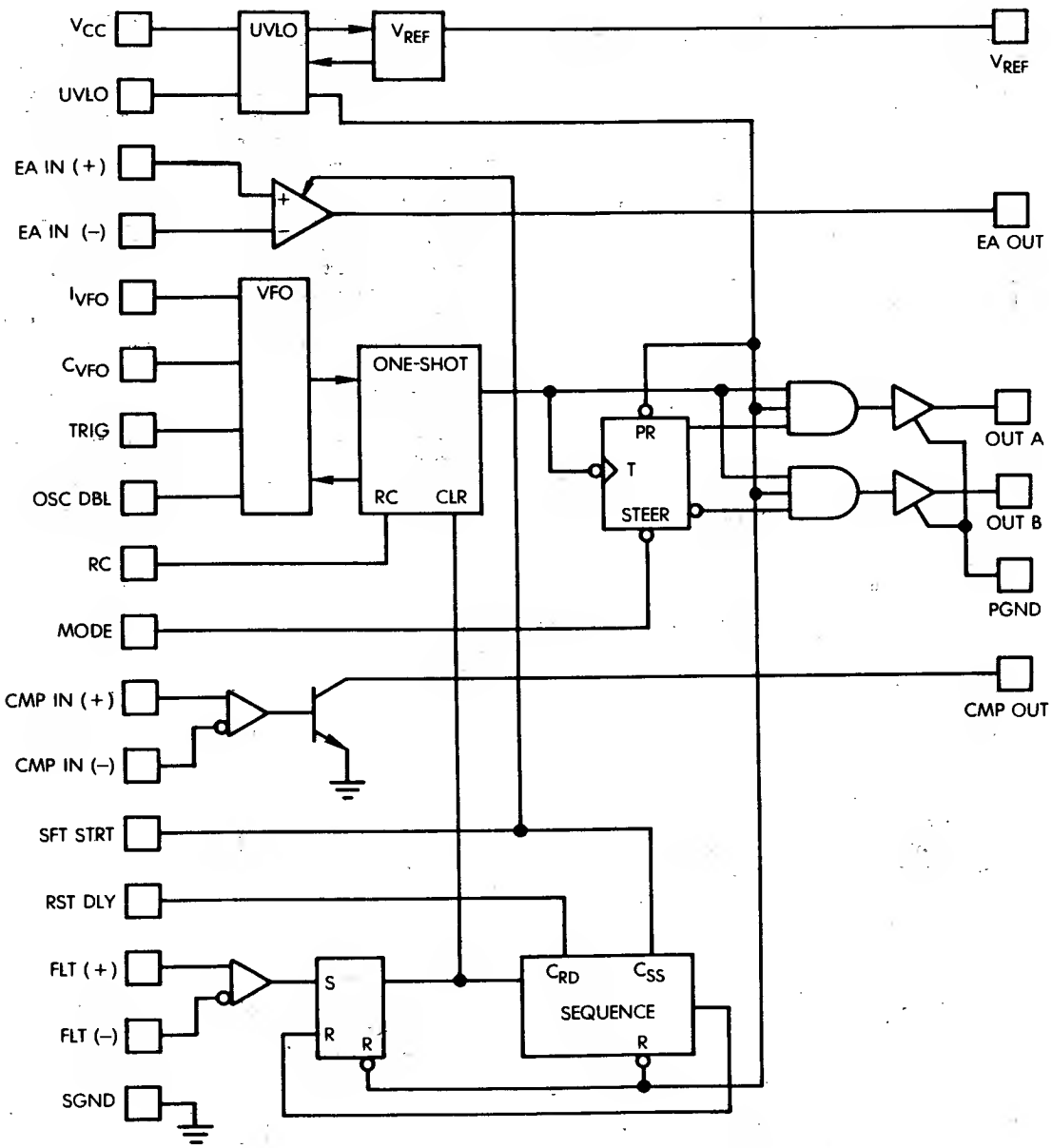

FIGURE 1. UC1860 SIMPLIFIED BLOCK DIAGRAM.

With three gain blocks (transconductance, transresistance, and voltage), the amplifier is compensated by two capacitors. The first feeds forward around the first stage directly to the second stage. This is because the first stage is designed for high gain and low offset but has poor high frequency characteristics. The second capacitor, the main

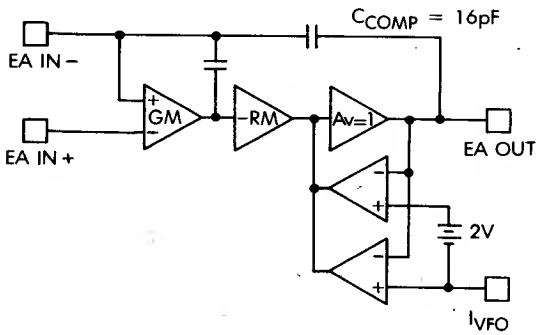

FIGURE 2. ERROR AMPLIFIER WITH OUTPUT SWING CLAMPS.

compensation capacitor, is connected from the output to the inverting input.

Amplifier bandwidth is controlled by the impedance seen by the inverting input terminal. To the first order, bandwidth in a simple feedback configuration is easily calculated by the equation

$$fo = \frac{1}{2\pi(Rin)(Ccomp)} \quad . \quad \text{(eq. 1)}$$

where Ccomp is the internal 16 pF compensation capacitor that appears between the output and inverting input pins. The amplifier is unity gain stable for unity gain bandwidths less than 5 MHz (ie. Rin > 2 kohm).

Higher gain bandwidth products can be obtained by choosing Rin and closed loop gain appropriately. Figure 3

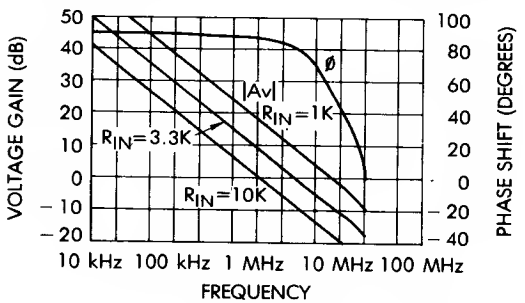

FIGURE 3. ERROR AMPLIFIER FREQUENCY RESPONSE.

shows the gain and phase characteristics of the amplifier for various resistive input impedances. Note that the phase curve is the same at higher frequencies for all three values of Rin shown. This is to be expected, since the higher order poles are internal to the amplifier. The combination of Rin and Ccomp primarily adjust the first pole position leaving higher frequency phase response unchanged.

Since the error amplifier is intended to control the frequency of the VFO, the outputs are clamped to obtain predictable minimum and maximum frequency. Each clamp circuit is actually an independent amplifier that monitors the output of the error amplifier and compares it to a reference. The reference for the lower clamp amplifier is the voltage at the I_{VFO} pin while the upper clamp is 2V higher. If the error amplifier attempts to exceed either of these levels, the appropriate clamp amplifier overrides the third stage of the error amplifier and the output is held at the clamped value. Figure 4 shows a plot of typical input offset voltage as a function of output voltage. In the figure, the horizontal axis is output voltage referenced to the I_{VFO} voltage. Note the sharp edges at the two extremes indicating clamped operation.

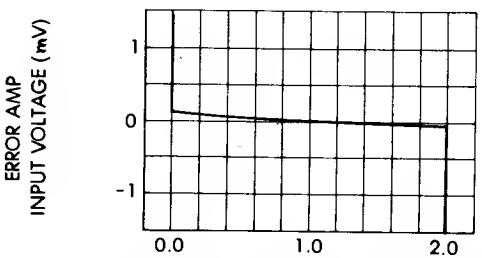

FIGURE 4. ERROR AMPLIFIER DC CHARACTERISTICS.

VARIABLE FREQUENCY OSCILLATOR

The variable frequency oscillator and one-shot functions are closely integrated to achieve the desired operating characteristics. ECL type logic gates and comparators are used to facilitate high frequency (3 MHz) operation. The oscillator will free run at a frequency of approximately

$$f(osc) = \frac{I_{VFO}}{C_{VFO}} \quad . \quad \text{(eq. 2)}$$

In no case, however, can the frequency of the oscillator ever exceed the frequency required to support a complete pulse width from the one-shot.

Figure 5 is a detailed block diagram of both the VFO and the one-shot. The frequency of the VFO is proportional

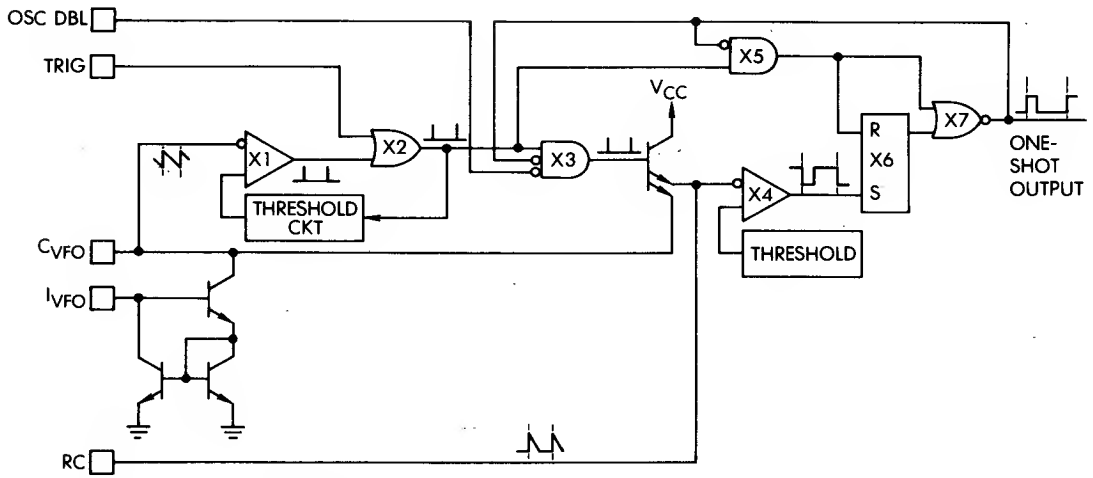

FIGURE 5A. DETAILED BLOCK DIAGRAM OF VFO AND ONE-SHOT.

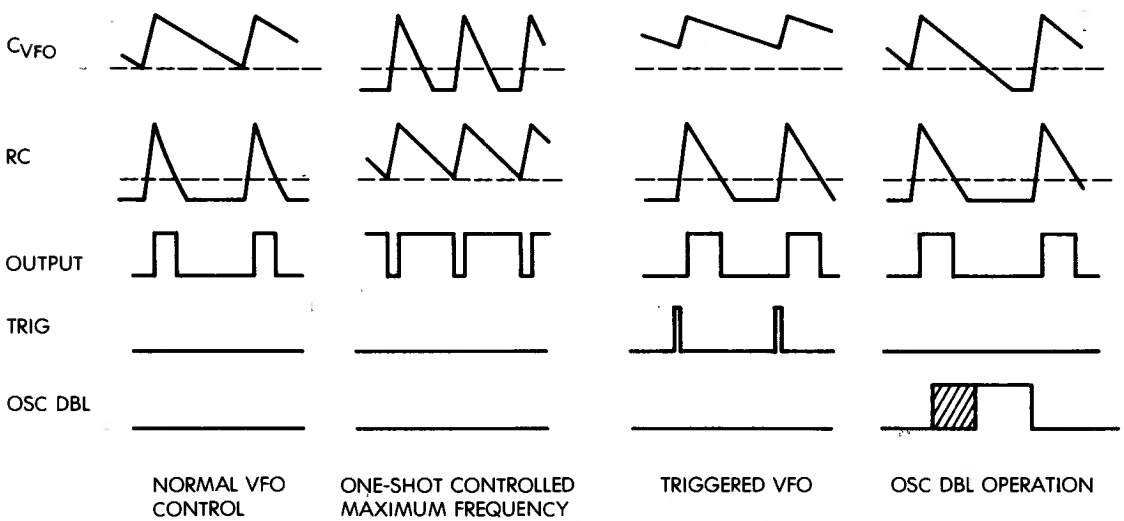

FIGURE 5B. TIMING DIAGRAMS FOR THE VFO AND ONE-SHOT.

to the current into the I_{VFO} pin. This pin is the input to a Wilson style current mirror and exhibits the temperature coefficient of two diodes (approximately 1.4V at 25C with a temperature coefficient of −4mV/C). I_{VFO} current is mirrored about to discharge the timing capacitor, C_{VFO}. Under normal operation, when C_{VFO} discharges to the lower oscillator threshold, hysteretic comparator X1 changes state causing gate X3 to recharge both C_{VFO} and the timing capacitor on the RC pin. Hysteretic comparator X1 then resets and the oscillator recycles.

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The trigger (TRIG) and oscillator disable (OSC DBL) inputs can be used to modify the free running characteristics of the oscillator. If TRIG is raised above its threshold during the discharge time of the oscillator, the recharge sequence is immediately executed, resulting in synchronous operation. If, however, OSC DBL is true when either the lower threshold is crossed or the trigger input is received, X1 will change states, but X3 will not recharge the capacitors. They will continue to discharge until a lower retaining level is reached. As soon as OSC DBL returns false, then recharge action occurs immediately.

When the error amplifier output and the oscillator input, I_{VFO} are coupled with a resistor, R_{VFO}, then the oscillator frequency is determined by

$$f(osc) = \frac{V_{EA} - V_{IVFO}}{R_{VFO} * C_{VFO}} \quad \text{(eq. 3)}$$

where V_{EA} is the output voltage of the error amplifier and V_{IVFO} is the input voltage at the IVFO pin. The VFO gain, df/dV_{EA} is

$$\frac{df(osc)}{dV_{EA}} = \frac{1}{R_{VFO} * C_{VFO}} \quad \text{(eq. 4)}$$

With this simple arrangement the maximum frequency is given by

$$f(max) = \frac{2V}{R_{VFO} * C_{VFO}} \quad \text{(eq. 5)}$$

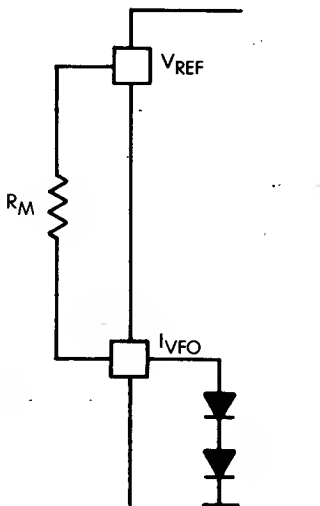
since the error amplifier maximum output is clamped two volts above the IFVO pin. Likewise, the minimum frequency should be zero. There is, however, an obvious limitation of minimum frequency in the input offset voltage of the lower clamp amplifier. Actual minimum frequency is

$$f(min) = \frac{vio}{R_{VFO} * C_{VFO}} \quad \text{(eq. 6)}$$

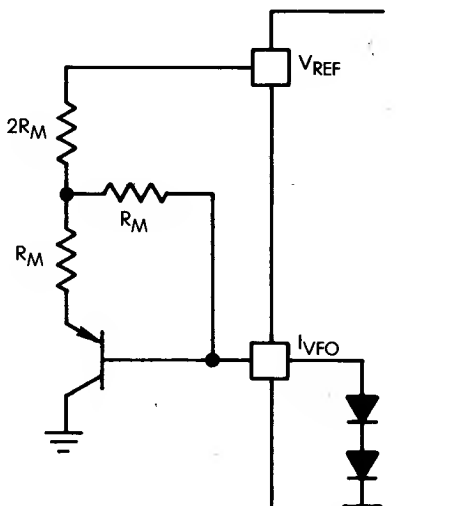
For lower clamp offsets less than 5mV, the maximum range of frequency would be the ratio of 2V and 5mV, or 400 to one.

When a nonzero minimum frequency is desired, an additional current can be injected into the I_{VFO} pin independent from the error amplifier. This can be most easily accomplished by a single resistor from the I_{VFO} pin to V_{REF} (figure 6). In this case, minimum frequency is given by

$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}} \quad \text{(eq. 7)}$$



$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}}$$



$$f(min) = \frac{1V}{R_M * C_{VFO}}$$

FIGURE 6 MINIMUM OSCILLATOR FREQUENCY.

where R_M ia the external resistor. It is important to note that this method is not inherently flat over temperature since the voltage at the I_{VFO} pin varies as two diodes. If this variation is unacceptable, three resistors and a pnp transistor can overcome this problem resulting in a minimum frequency of

$$f(min) = \frac{1V}{R_M * C_{VFO}} \quad \text{(eq. 8)}$$

ONE SHOT

The one-shot capacitor at the RC pin is recharged concurrently with C_{VFO}. This sets the output of comparator X4 to a low state allowing S/R latch X6 to be reset. The latch is reset by the signal coming from the output of X2 in the oscillator section via gate X5. The output of X5 also blanks the one-shot off. This is done for accuracy reasons so that the on time is solely a function of the resistive discharge of the RC pin. When both caps have been charged fully, the oscillator circuit drives the output of X2 low allowing both caps to discharge. The timing cap is discharged by an external resistor. The threshold of comparator X4 is set at 80% of the timing capacitor's full charge value. 0.22 time constants are required to reach this threshold making the on time

$$t(on) = 0.22 * RC. \quad \text{(eq. 9)}$$

When the lower threshold is reached, X4 output goes high setting S/R latch, X6, and the one-shot pulse is terminated.

It is important to observe two interactions between the VFO and the one-shot. While the one-shot is high, gate X5 prevents the oscillator from erroneously blanking the output low. The high output also prevents X3 from recharging the timing capacitors in the same way that OSC DBL does. This insures that in no case can the oscillator period (the inverse of eq. 2) be shorter than the time required for the one-shot. In cases where the VFO attempts to overrun the one-shot, the one-shot dominates and establishes maximum frequency.

TOGGLE FLIP FLOP

The output of the one-shot, in addition to limiting the VFO from out running the one-shot, performs two other functions (figure 1). A logic high level from the one-shot causes one or both of the outputs to drive high. The falling edge of the one-shot not only turns the output(s) off, but it triggers the toggle flip flop to change state. The toggle flip flop selects the output to be driven if the output mode control pin is low. If the output pin is high, both toggle outputs are high causing outputs A and B to operate in unison.

OUTPUTS

The output blocks are well suited to driving the active capacitive load presented by power mosfet gates. With this load in mind, they are designed to deliver currents up to 3A in both source and sink directions. Current rise times are in the order of 75A/us. This results in rise and fall times of 50 ns when driving series loads of 10nF and 2.4 ohma (figure 7). Unloaded transitions are 12ns. Of course, cross conducted charge has been minimized within the constraints of high speed design goals.

It is well worth noting that careful attention to low inductance printed circuit board layout along with proper damping and application of schottky clamp diodes are necessary when driving a large capacitive load directly. Disregard for this caution will result in the output/load combination becoming a highly excited tank that will ring and inject current into the chip substrate. Such injection is almost always a sure cause of problems in bipolar ICs.

REFERENCE

The bandgap reference needs little mention since it is a standard, borrowed from many previous designs. Trimmed for precision at wafer probe to 5V, it is specified at 1% tolerance at room temperature with no more than a 2% spread over temperature. While intended as a reference, not a voltage regulator for external use, it has line and load rejection capabilities that will allow it to be used as such for loads under 10mA. A bypass capacitor is required on the reference.

UVLO

The UVLO block (figure 8) consists of three comparators arranged to allow for flexibility of application. They can accommodate off-line, DC to DC, and even operation from a 5V supply.

The first of the three comparators monitors V_{CC}. It has hysteretic thresholds of 17 and 10V. This spread is ideally suited to off-line applications. The output of the V_{CC} comparator is an emitter follower that can go no higher than approximately 6.5V.

The second comparator monitors the UVLO pin which is resistively driven from the output of the V_{CC} comparator. This comparator turns the reference on or off, controlling the bias in the chip. When the reference is off, I_{CC} ia less than 0.5mA. After operation commences, I_{CC} increased to approximately 35mA. The thresholds of this second comparator are 4.0 and 3.5V.

The third comparator monitors V_{REF} and has a threshold of 4.5V. If either this comparator or the second has a low output, then the chip is disabled and reset. When this is the case, both output are driven to a low state, the toggle

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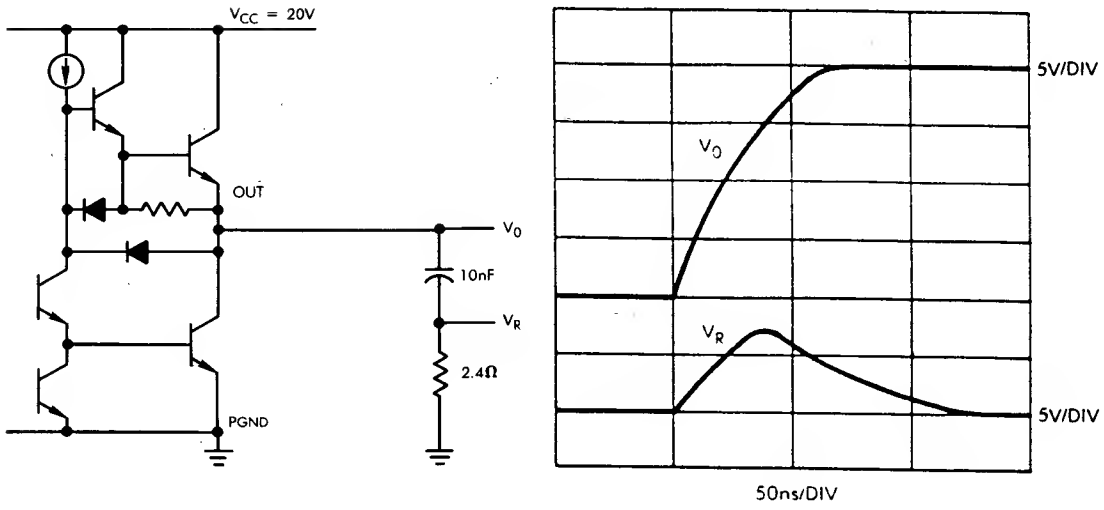


FIGURE 7. OUTPUT STAGE MEASURED PERFORMANCE.

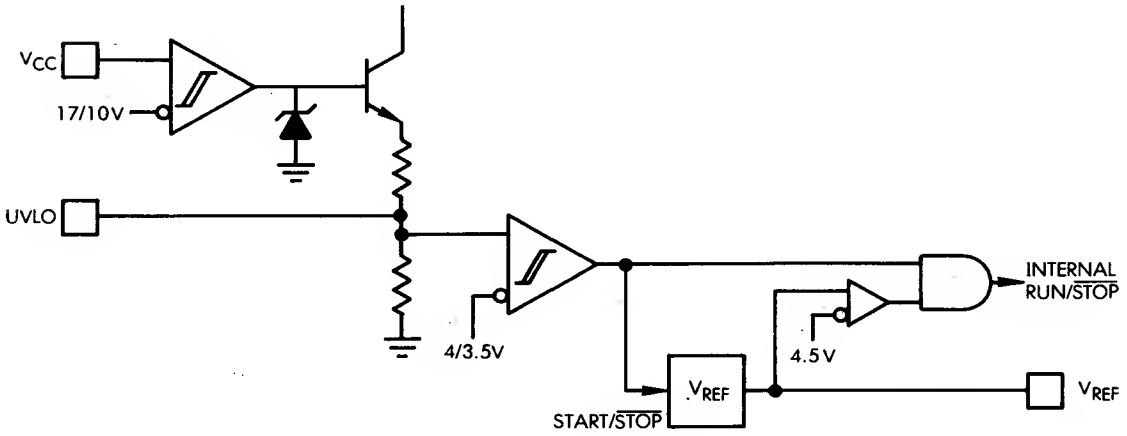


FIGURE 8. UVLO DETAILED BLOCK DIAGRAM

flip flop is preset to select ouput A, the soft-start capacitor is discharged, and the fault latch is reset.

Application of the UVLO features is simple. With no connection to the UVLO pin, the behavior of the UVLO block is dominated by the V_{cc} comparator and is suited for off-line usage. DC to DC applications can be made by two external resistors, one from V_{cc} to UVLO and the other from UVLO to ground. This exploits the 4V hysteretic threshold of the second comparator. Keep in mind that the UVLO pin has an input impedance of 23 kohm when selecting the two external resistors. Operation from a 5V supply is achieved by tying UVLO, V_{cc}, and V_{REF} all to the external 5V supply. The UVLO pin can also be used to disable the chip at any time by pulling it below 3.5V. The UVLO pin will source no more than 1.5mA when pulled to ground.

FAULT MANAGEMENT AND RESTART SEQUENCING

The fault comparator and latch along with the soft-start and restart delay functions are shown in (figure 9). When the chip is powered up, UVLO resets the fault latch and discharges the soft-start capacitor, C_{SS}. The restart delay capacitor, C_{RD}, is also discharged since the latch is reset. After UVLO, C_{SS} is charged by an internal 5μA current source. The voltage at the soft-start pin is used to modify the upper clamp voltage of the error amplifier. In this way, a slow frequency ramp is obtained from zero to the point where the control loop takes over.

The chip is designed for easy implementation of a hic-up style of fault management. The fault comparator will sense signals with a common mode range of −0.3 to 3.0V. If (hopefully never in your application) the input to the fault comparator causes its output to go high, the fault latch is set. Immediately the one-shot is cleared and the outputs turn off. C_{SS} is also discharged. C_{RD} is then allowed to be charged by an internal 5μA current source. This is the zero power dissipation time in the hic-up cycle. Until the restart delay capacitor charges to 3V, the fault latch cannot be reset. When both the fault comparator output is low and C_{RD} is over 3V, the fault latch is reset. At this point in time, C_{RD} is discharged and C_{SS} is allowed to soft-start the chip. If the cause of the original fault is still present, the chip will continue to hic-up until the fault condition is removed, when normal operation will resume.

Note that the internal 5μA sources are not tightly controlled. However, if either soft-start or restart delay time is critical, a 50k resistor to V_{REF} will provide a precise current that is sufficient to swamp out any inaccuracies of the internal source.

Two variations of the hic-up are possible. Selecting a value of zero for C_{RD} will cause the chip to immediately attempt to restart upon removal of the fault signal. If, on

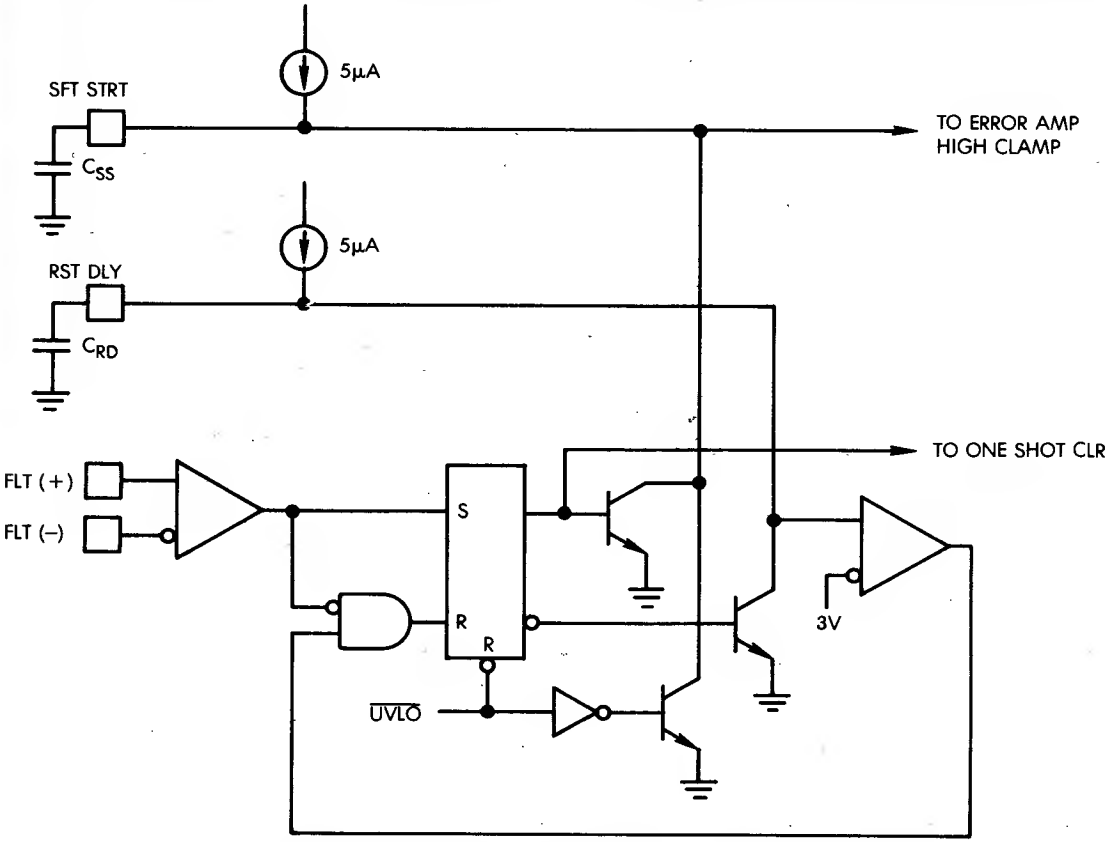


FIGURE 9 FAULT MANAGEMENT AND RESTART SEQUENCING BLOCK DIAGRAM.

the other extreme, fully latched fault behavior is desired, then the restart delay pin (RST DLY) can either be grounded or tied to the open collector output of an external logic gate. This uncommitted comparator could be used for this application. When Restart Delay is held low, then the only ways to reset the fault latch and reinitiate operation of the chip are to remove V_{CC} (UVLO will clear the latch) or release RST DLY, allowing it to exceed 3V.

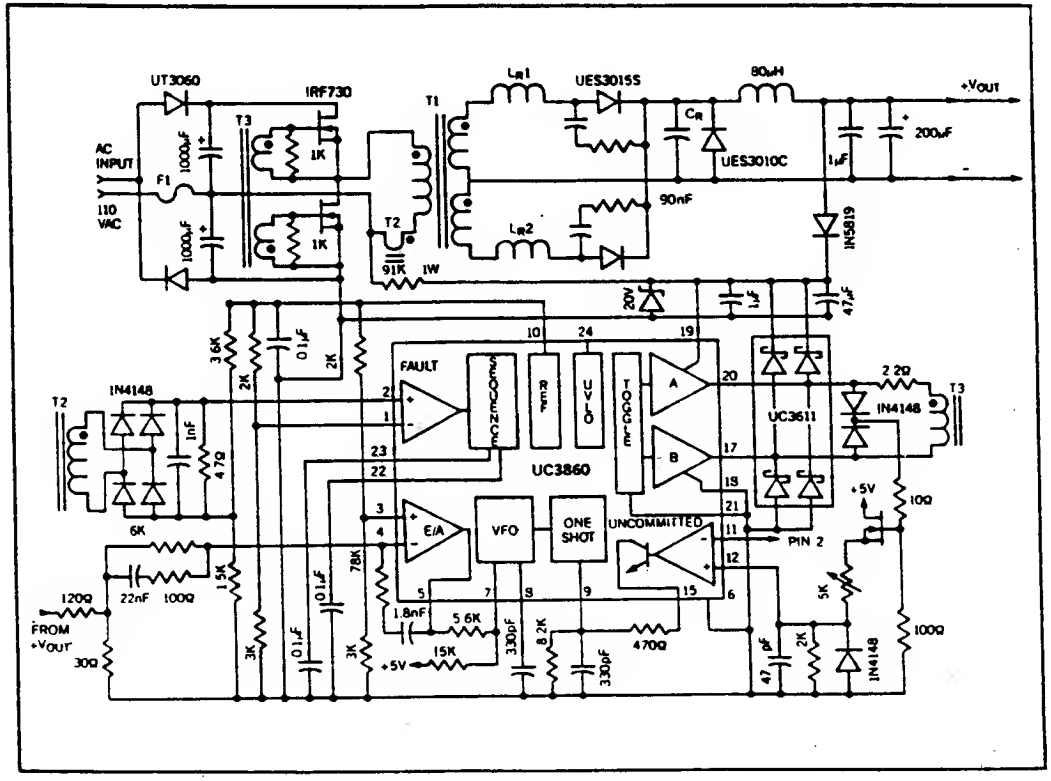
UNCOMMITTED COMPARATOR

The uncommitted comparator is similar in design and speed to the fault comparator except its output drives an open collector npn transistor. This output can be used in a variety of applications. One would be to shunt the RC pin with a second resistor causing a reduction in one-shot pulse width. The input common mode range is identical to the fault comparator, -0.3 to 3.0V.

SUMMARY

The UC1860 control chip has been designed with the necessary features to implement the control function in resonant mode power conversion circuits operating at frequencies up to 3 MHz. While some publicized applications have been considered in the design of this chip, its versatility should accommodate many specific adaptations of resonant mode power systems as well.

150 Watt Quasi-Resonant Power Supply



UC3860 RESONANT CONTROL IC REGULATES OFF-LINE 150 WATT CONVERTER SWITCHING AT 1 MHZ

ABSTRACT

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms in addition to transferred charge and energy will be analyzed as functions of time, and input/output conditions. Specific and generalized equations are given for this example, also applicable to other topologies by those skilled in modern power supply design.

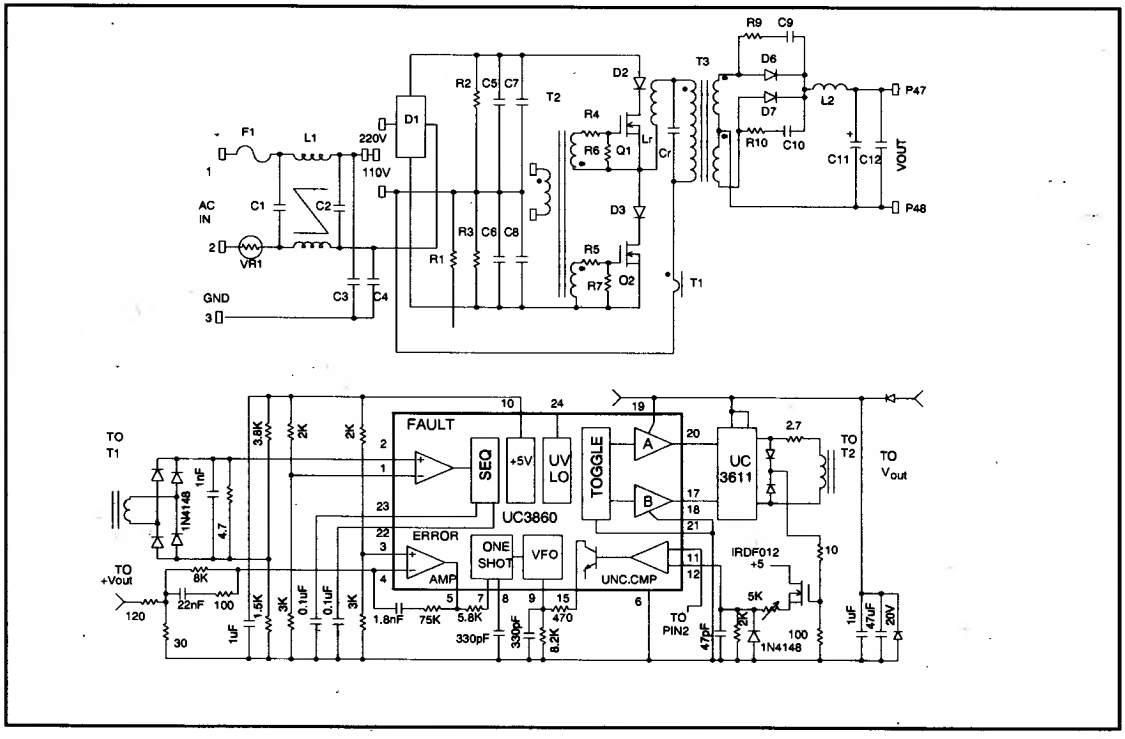
INTRODUCTION

The thrust towards resonant mode power supply designs has been fueled by the industry's demands for increasing power densities and high overall efficiency. Coupled with the additional requirements for low EMI, many designers are exploring the most likely candidate for todays sophisticated, high frequency power supplies; resonant mode power conversion.

amperes of load current, it operates from a 110/220 AC input, or 220 to 380 VDC at high efficiency.

DESIGN CONSIDERATIONS AND OVERVIEW

Although several basic topologies deserve consideration in this off-line application, only the Half Bridge configuration offers numerous key advantages. As opposed to the single-ended Forward converters, the half bridge provides bidirectionial utilization of the transformer, thus eliminating the need to incorporate dissipative or complex flux reset mechanisms. In addition, the primary switched voltage is one-half that of its single ended or full-bridge counter-part, significantly reducing the turn-on losses. As a reminder, zero current switching minimizes ONLY the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge results in lower turn-on losses due to the lower voltage.

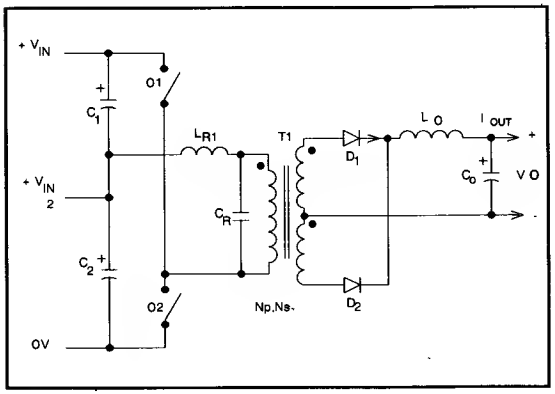


While a bewildering selection of possible resonant mode topologies and configurations exist, this paper will focus on the quasi-resonant half bridge topology. Primary side resonance and zero current switching will be incorporated into the design, with the control circuit essentials performed by the UC3860 resonant mode control IC.

Described in the text is a 150 watt off line converter switching at maximum frequency of 1 megahertz resulting in an effective 500 kilohertz utilization of the main transformer. Delivering 15 volts at 10

Primary side resonance will be utilized in this design, but not as an attempt to minimize the core size. Instead, this technique will reduce the peak secondary currents and rectifier losses. transferrring them to the primary side where the diode voltage drop is less significant, thus enhancing overall efficiency. Additionally, this design can be compared to a previous example [ref. 1] which incorporated secondary side resonance and operated over similar line, load, frequency and power variations.

Half cycle conduction in both design examples accomplishes a undirectional current flow at each of the primary switches. Unlike its full counterpart, all the energy stored i n the resonant capacitor must be transferred to the output, without returning the excess back to the primary storage capacitors.



The UC3860 resonant control IC will adjust the conversion frequency to regulate the fifteen volt output over all line and load combinations. Zero current switching is facilitated by modulating the programmed maximum on-time with the controller's uncommitted comparator. In addition, overload protection is provided by means of a programmable restart delay circuit (hiccup) which reduces the conversion retry rate following a fault detection.

DESIGN SPECIFICATIONS

An off-line 150 watt, single output design has been selected as a typical application. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations.

INPUT VOLTAGE

110 VAC INPUT = 85 MIN, 132 MAX (VAC)

220 VAC INPUT = 170 MIN, 270 MAX (VAC)

DC INPUT = 220 MIN, 380 MAX (VDC)

AC LINE FREQUENCY = 50 HZ MIN

OUTPUT VOLTAGE = 15 VDC

OUTPUT CURRENT = 10 AMPS MAXIMUM CONTINUOUS, 2.5 AMPS MIN

LINE REGULATION = 15 MILLIVOLTS

LOAD REGULATION = 15 MILLIVOLTS

OUTPUT VOLTAGE RIPPLE=

100mV (Pk-Pk), DC-20 MHZ

EFFICIENCY = 75% TYP. AT FULL LOAD

TOPOLOGY FUNDAMENTALS AND OVERVIEW

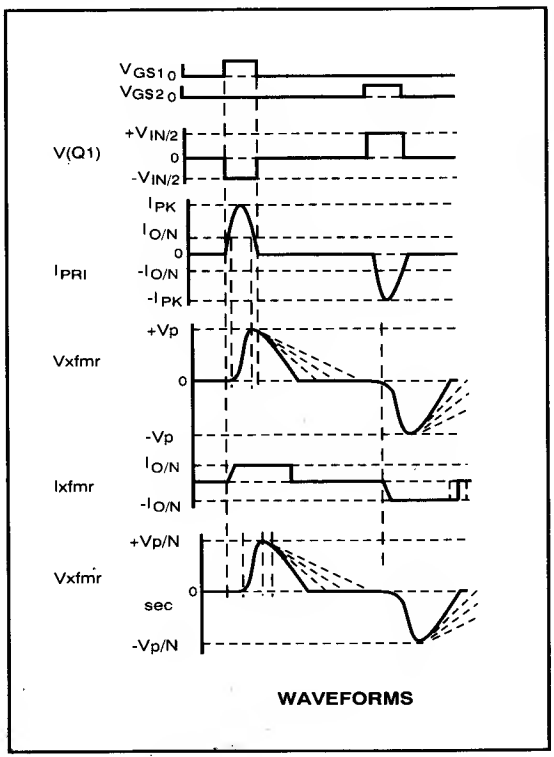
The general circuit diagram for a quasi-resonant half bridge converter using primary side resonance is shown with the corresponding waveforms. Transistors Q1 and Q2 are alternately driven from the control circuitry at a repetition rate determined by the UC3860's error amplifier output voltage and turned off at zero current by the detection circuitry..

Transistor Q1 turns on at time t(0), connecting the series resonant L C tank across the bulk storage capacitor C1, with a voltage potential of +Vin/2. The primary current ramps up linearly at the rate of +Vin/(2*Lr) from zero to Iout/N which is intersected at time t(1). During this interval dt(1-0) all primary current is delivered to the output, and no voltage is across the resonant capacitor Cr.

Beginning at time t(1), primary current can be expressed by adding the two individual components; the "constant" output current Iout/N, and the sinusoidal current (Ir) flowing through the resonant capacitor. The peak resonant current is determined by the iput voltage (+Vin/2) divided by the characteristic tank impedance, Zn. Primary current rises to its peak of Ir plus Iout/N, and decreases sinusoidaly. It intersects the output current (Iout/N) again at time t(2), and crosses zero at time t(3) when the transistor switch is turned off.

In a sinuosidal manner, the resonant capacitor voltage begins its rise at time t(1) and continues to its peak at time t(2). The voltage then decreases until time t(3) where it then begins a linear discharge at the rate of Iout/Cr. Zero voltage is reached at time t(4) when all stored charge in the resonant capacitor has been transferred to the output. This waveform is also the transformer primary voltage, and is reflected to the secondary side by the turns ratio N.

Secondary current has a linear leading edge until reaching its plateau of Iout, assuming a negligible magnetizing current for the output inductor. The resonant capacitor provides a constant current to the output until its charge is totally transferred. At this point, the energy is stored in the output LC section provides a regulated output until the next cycle is initiated. Consecutive switching cycles will repeat the conversion process and corresponding waveforms.

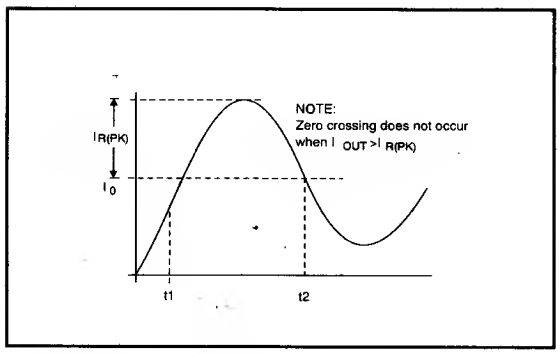


WAVEFORMS

QUASI-RESONANT CIRCUIT LIMITATIONS

In order to facilitate zero current switching, the peak resonant current component I(r) must always be greater than Iout, or the zero inersect will not be reached. Specifically, the output impedance (Zo) must always be greater than the characteristic tank impedance, (Zn). This relationship also specifies the minimum input voltage (Vin min) and maximum output current (Iout) limits for proper circuit operation.

The ideal ratio of the full output current (Iout max) to the minimum resonant peak current Ir(peak) min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents, and losses. A twenty-five percent overload current will be used as a guardband in this design. Typical of many current limit thresholds, it corresponds to an 0.75:1 ration of Iout(max) to Ir(peak)min.



Being a Buck derived topology, the secondary input and output volt-second products must be equal, thus defining Vin (secondary) minimum. The resonant tank inductor and capacitor can be transposed to the secondary also, and calculated knowing Vin min(sec), F(res) and Z(o)min. Once the transformer turns ratio has been determined, these can be appropriately scaled to the primary side.

The resonant L-C components are now uniquely defined by:

$$L(r)sec = \frac{.75 * Vsec\,(min)}{2 * Pi * Fres * Iout} = \frac{0.12\,Vsec\,(min)}{Fres * Iout\,(max)} = 175nH$$

C(r)sec = 1 [(2*Pi*Fres)^2*L(r)=91nF

Z(r)sec = (L(r)/C(r))$^{0.5}$ = 1.39 ohms,

and Fres = 1.25 MHz

TRANSFORMER TURNS RATIO

The determination of the transformer turns ratio for this design will begin similarly to that of conventional square wave converters. Obviously, the required output volt-second product must first be satisfied with the most difficult condition being low line and full load. A topology coefficient, K(t) is introduced to specify the maximum ratio between the conversion (switching) frequency and the resonant tank frequency. This is somewhat analagous to maximum duty cycle is a square wave converter. As K(t) approaches unity, the utilization is maximized and turns ratio is optimized.

Charge is taken from the bulk storage capacitors during each cycle and stored in the resonant capacitor. The output load discharges this at a rate determined by the output currrent, and the discharge time varies inversely with load current. At full load, the minimum discharge time is reached, reduceing the topology coefficient, K(t), to 0,8 in this application.

To satisfy the required output volt-second product of this Buck derived converter at low line:

$$Vout = \frac{Vpri * K(t)}{2 * N}, \text{ or } N = \frac{K(t) * [Vp\,(min) - Vloss]}{2 * (Vo + Vd + Vloss)} = 5.1{:}1$$

More specifically, the turns ratio can be calculated by examining the total charge transferred per cycle, Q(t). This varies as a function of Vin, Iout and Vout, assuming C(r) is fixed and zero current switching. [ref 2] Using the specified parameters for this design, the relationships are combined and the quadratic equation is solved, resulting in a turns ratio (Np/Ns) of 5.1:1 also. The design will proceed using a 5:1 ratio for simplicity.

$$N^2\left[\frac{Lrs * Io}{(Vo + Vd)} - Tc\right] + N\frac{(Vpri - Vx)}{4 * Fr * (Vo + Vd)} + \frac{Crs * (Vp - Vx)^2}{2 * (Vo + Vd) * Io} = 0$$

where Tc= 1/Fconv(max) = 1us; Vx= Vloss primary MOS switch

Vd=Vrectifier (output); Io=Iout maximum

and Vpri=Vp(minimum)

MAIN TRANSFORMER DESIGN

Off-line transformers lend themselves to low, wide bobbin windows, typical of the ETD geometry. This shape window provides adequate room to accomodate the creepage and clearance distances required for international safety specifications. Transformer losses will be held around one-percent of the total input power, or approximately 2 watts with a temperature rise not to exceed 40 degrees Centigrade. A core size is selected with a thermal impedance R(t) in the neighborhood of 40°C/2W, or 20°C/W. The precise size will be calculated using the area-product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} * 10^4}{120K2f}\right]^{1.58} * (K_h f + K_{ef}{}^2)^{0.66} \quad cm^4$$

WHERE:

Pin = Input Power - 180 Watts

K = Winding Factor = 0.163 for a half bridge

f = Transformer Frequency = 500 KHZ

Kh = Hysteresis Coefficient = 4*10^-5 for 3C85

Ke= Eddy Current Coefficient = 4*10^{-10} for 3C85

A calculated area-product of 0.543 cm^4 steers the selection towards the ETD-34 geometry and size, and 3C85 material. Since the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

Calculating the volt-second product for this primary side resonant design is more difficult than for that of its secondary side counterpart. Integrating the complex voltage waveform over the conversion period is the most exact method, as detailed in the charge transfer equations [ref2]. A less precise, yet fairly accurate technique is to assume a triangular voltage waveform, breaking the period into on-time and off-time sections. Addition of these geometric areas (V*t) results in an estimate of the actual primary volt-second product. Core losses will need to be analyzed over the full range of line, load and conversion frequency ranges. The minimum number of primary turns will be calculated using low line conditions, and the cross sectional core area of 0.971 cm^2. A total flux density swing of 1 kiloGauss (per manufacturers data) is recommended not to exceed the allocated temperature rise.

$$Np\,(min) = \frac{PrimaryV * t\,product * 10^4}{FluxSwing * CoreArea}$$

9

Using low line condition and 10V MOS drop.

$$Np\,(min) = \frac{0.5*200*10^{-6}*10^{4}}{0.100\ T*0.971\ cm^{3}} = 10.3\,Turns$$

(Use 10 Turns)

The actual core power density is calculated from the following equation, allowing a 20 degree temperature rise due solely to core losses.

$$Power\ Density = \frac{T_r}{R_t \cdot Vol} = \frac{20^{\circ}C}{19 \cdot 7.64} = 138 mw/cm^{3}$$

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19 degrees C per watt, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between core and copper loss can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accommodate fewer turns, or less copper.

It has already been established in a previous section that the turns ratio for this design be 5:1, Npri: N sec. Minimization of the leakage inductance is obtained by "sandwiching" the secondaries between the primaries, or using a split primary winding technique.

In this example, one-half of the primary number of turns will be wound first, closest to the core center leg. Then, the corresponding secondary is wound directly above its primary, followed by the other secondary. The final winding is the remaining primary half, with good coupling to its corresponding secondary as shown in the following figure.

WINDING ORIENTATION

Copper strap or foil will be utilized for each winding to minimize "build-up" which increases the distance between windings, hence leakage inductance. The necessary primary and secondary copper areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

PRIMARY RMS CURRENT, I pri(rms) = 2.8 AMPS RMS

SECONDARY RMS CURRENT 1sec(rms) - 7.1 AMPS RMS (EACH WINDING)

PRIMARY CONDUCTOR AREA Axp = Ipri(rms)/450 A/cm3 = $6.33*10^{-3} cm^2$

SECONDARY CONDUCTOR AREA Axs = 1sec(rms)/450A/Cm3 = $15.8*10^{-3} cm^2$

PRIMARY INDUCTANCE, Lpri = Al*Np^2 = 190 uH

SECONDARY INDUCTANCE, Lsec = Al*Ns^2 = 7.6 uH (each)

The primary conductor area is approximately equal to that of an AWG #19 wire, while the secondary area is closest to an AWG #14 wire. From Eddy Current calculations is can be seen that the depth of penetration at 500KHZ is $10.6*10^{-13}$ cm, or about the thickness of an umber 37 AWG wire. The most practical technique to minimize the AC loss in a transformer winding is to incoporate copper strip, or foil, as in this design. Its width is determined by the bobbin width and safety spacing requirements of 8 mm per winding as shown.

An 8 millimeter primary to secondary spacing between the winding ends will be subtracted from the bobbin width of 2.1cm, leaving 1.30 cm for the copper strap width. Allowing for tolerances, standard half-inch (0.500") width foil will be utilized in this design.

Standard 2 "mil" (0.002 in) foil will be used for the primary, which is slightly larger than the required thickness of 1.872 thousandths of an inch. The calculated secondary thickness exceeds the depth of penetration, so twin foils each of half the required thickness (0.0085 cm) are mandated. Each of the three "mil" (0.003") foils will be thinly insulated from the other.

The resistance and power loss of each winding is summarized:

R pri = $2.29*10^{-6} * 5.99 *10$ T/$6.18 *10^{-3}$ = 22.2 milliohms.

R sec = $2.29*10^{-6} *5.99*2$T/$21.91 *10^{-3}$ = 1.25 milliohms

Winding power loss = 1 rms^2 (winding) * Resistance (winding

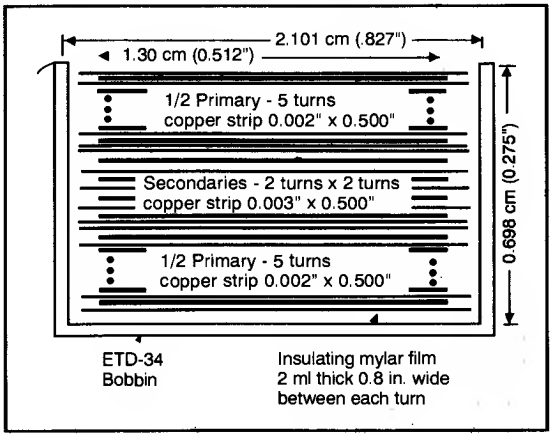
P loss pri = 2.8^2 * 0.0222 = 174 milliwatts (each wdg)

P loss sec = 7.1^2 * $.125*1^{-3}$ = 63 milliwatts (each wdg)

P loss copper = 2*(174 + 126 mW) = 0.60 watts

Transformer power loss = copper + core loss = 1.5 watt total

Temperature rise = R(0) * Ploss total = 19°C/W * 1.5 = 28.5°C



DESIGN PROCEDURE AND SUMMARY

The resonant components can now be transformed to primary side values using the caluclated turns ratio N.

L(r)p = L(r)s * N^2 = 4.4 uH

C(r)p = C(r)s / N^2 = 3.6 nF

Z(r)p - [(L(r)p / C(r)p)$^{0.5}$] = 35 ohms

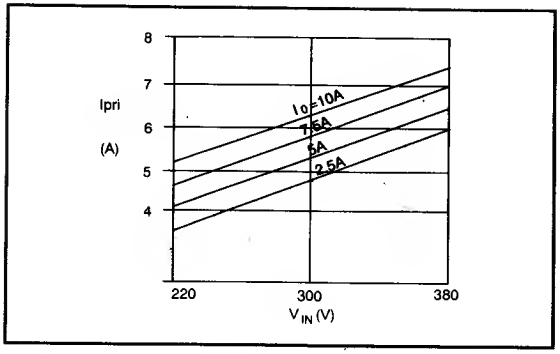
Additionally, the peak primary current and rms currents at the transistor switch, transformer primary and secondary rectifiers are calculated by the following relationships:

I(p)pk = [Io(max)/N] + Vp(max)/(2*X(r)p) = 5.2A @220V, 7.4A @380V

I(p)rms = I(p)pk*[Ton/(2*Tconv()$^{0.5}$ = 2.85 Arms at XFMR primary (assume pulsed sinusoid) = 2.01 Arms at each switch

I(s)rms = I(o)max*[(Ton/Tconv)0.5] = 7.8Arms at XFMR secondary = 5.5Arms per rectifier

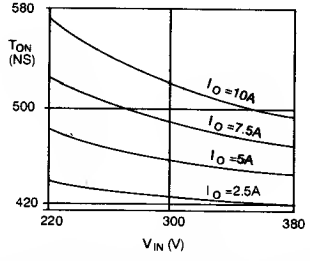
The selection of semiconductors, rectifiers, heatsinking requirements and wire gauges follow standard design practices. For the purpose of this paper, no elaboration is included, however is detailed in references 1 and 2. Using this design equations listed previously and in the Appendix, these parameters can be calculated and plotted over the line and load ranges specified, and are summarized in the following graphs:



TIMING CONSIDERATIONS

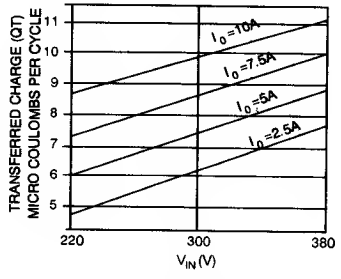
The operation of this quasi-resonant circuit has been described as requiring a variable frequency, FIXED on-time control pulsetrain. In actuality, the on-time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented in chapter five, the on-time is calculated and plotted for the ranges of Vin and Iout.

ON-TIME vs. Vin AND Iout



The charge transferred from the primary to the secondary per cycle is a function of both Vin and Iout. Using the equations presented previously in section 5, the results are graphically represented in the following figure.

Transferred Charge vs. Vin and Iout

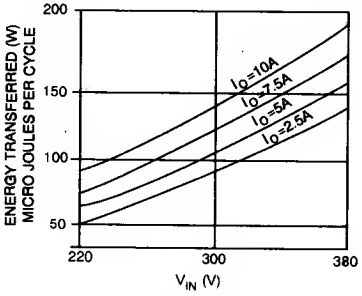


For the selected values of voltage and current shown, the average change required in voltage or output current per micro Coulomb transferred have been calculated.

AVERAGE dV/uC = 5.935 V/uC; and the average dI/uC = 2.086 A/uC

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by Vin / 2 to convert from charge to energy, with the results shown below.

ENERGY TRANSFERRED PER CYCLE



The conversion period is obtained by dividing the energy transferred per cycle by the output power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for various input voltages and output currents below.

CONVERSION FREQUENCY

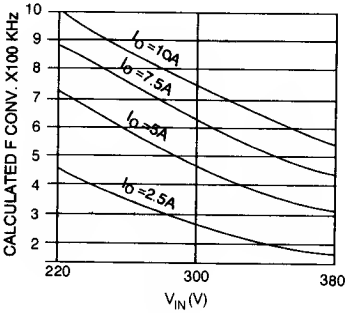
The control circuit adjusts the conversion frequency to maintain a constant output voltage of V out over changing line and load combinations. Maximum conversion frequency will occur at low line and full load, where, by design, the frequency equals the resonant tank frequency divided by K(t). Minimum frequency will occur at high line (Vpri max) and light load (Iout min), and the following equation can be used to estimate the conversion frequency for various line and load possibilities.

$$Tconv = \frac{vpri}{2*N*Io*Vo}\left[\frac{2*N*Lrs*Io^2}{Vpri} + Vpri*\frac{Crs}{N} + \frac{Io}{2*Fr}\right]$$

which can be expanded to account for losses in both the primary switches (Vx) and output rectifiers (Vd) and reduced to:

$$Tconv = \frac{Lrs*Io}{Vo-Vd} + \frac{Crs*(Vp-Vx)^2}{2*N^2*Io*(Vo-Vd)} + \frac{Vp-Vx}{4*N*Fr*(Vo-Vd)}$$

CONVERSION FREQUENCY vs. Vin & Iout



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OUTPUT FILTER DESIGN

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHZ equating to 90 uH. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. A 1.3" o.d. toroidal core of high frequency material was utilized, available as a standard product from Pulse Engineering.

For the output capacitance, two 100 uf electrolytic capacitors were used in parallel to achieve an ESR value of 3 to 15 milliohms — a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers. A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolythic capacitors are used for this application.

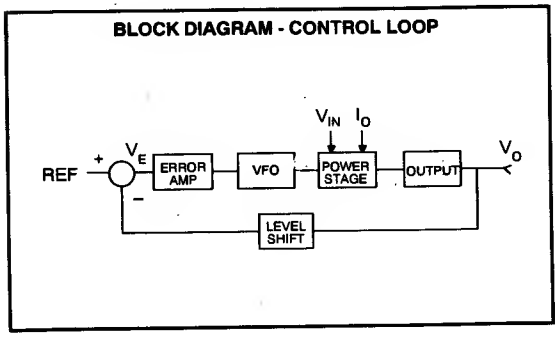
THE UC3860 RESONANT MODE CONTROL IC

The versitile UC3860 resonant mode controller easily implements fixed on-time, frequency modulated control schemes while providing various user programmable features and unique fault protection. Specifically, this 3 MHz device includes dual 3 amp peak totem pole output drivers and precision clamps on the 5 MHz error amplifier output to accurately control minimum and maximum frequency. In addition, an uncommitted comparator is included for use with zero current switching techniques, and programmable fault thresholds and logic for reduced losses during overload conditions. Preset undervoltage lockout thresholds of 17/10 volts are optimized for off-line designs, but are easily reprogrammed by the user for other applications.

Each of the UC3860 functions are utilized in this design and have been previously highlighted in the references. Zero current detection and switching is performed by connecting the uncommitted comparator's output to the one shot timing network, a technique which allows a programmed maximum on-time that can be modulated as zero current is crossed. Any propagation delays can effectively be "nulled-out" with the addition of anticipator circuit detailed in references 1 and 2. A programmable restart delay following the receipt of a fault condition, often referred to as "hic-cup" has been incorporated in addition to soft start, which gradually increases the conversion frequency in a resonant converter. The UC3860 provides complete regulation and control for this 150 watt design over all line and load combinations.

CLOSING THE LOOP

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.



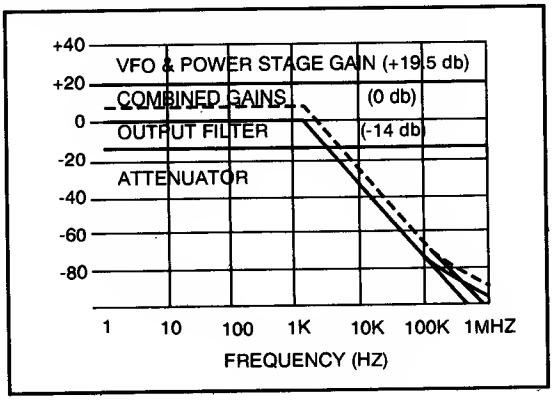
POWER STAGE

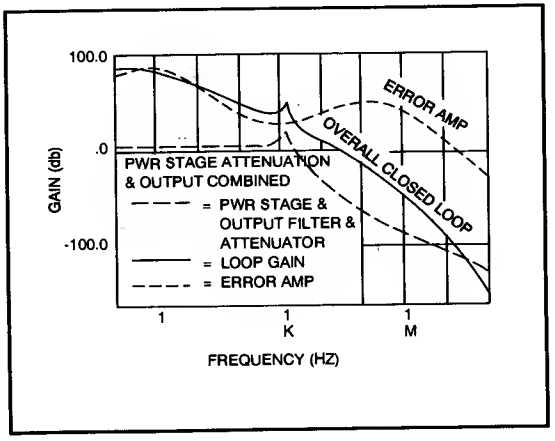
The small signal gain of the power stage will be approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch on-time is constant, and any changes in frequency directly effect the off-time, or resonant capacitor discharge time. Additionally, both Vin and Iout are assumed to be constant during the interval of interest.

Tabulated below at several points of interest are the values for this gain, obtained from the results of previous sections for work done in the references. The gain of the power stage (in volts per hertz) varies significantly over the input and output ranges, and the highest value will be used to approximate the worst case condition.

V IN sec(V)	I OUT (A)	Win uJ/cyc	F conv KHZ	GAIN Vusec	GAIN (db)
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	10.7	20.6
22	7.5	78	900	9.65	19.7
38	7.5	185	450	11.3	21.1
22	10	91	1000	9.55	19.6
38	10	205	560	11.8	21.5

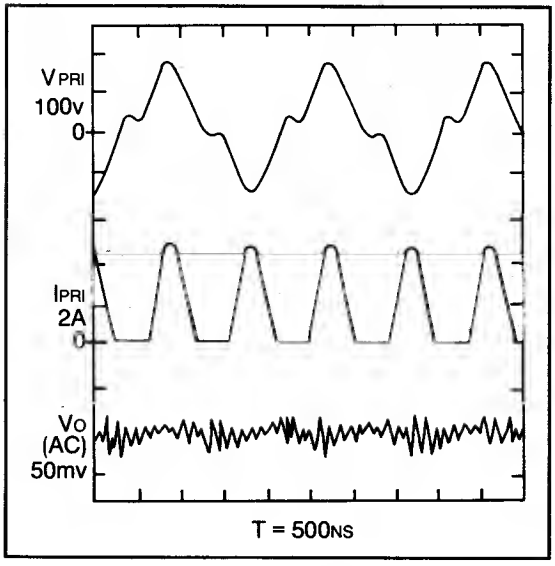
A slightly greater than worst case value of 23 volt-microseconds will be used for the power stage. Multiplying this by the VFO gain of 0.4 Mhz/v results in an combined gain of 9.2 Vout / Vea out.





POWER SUPPLY PERFORMANCE

This 150 watt quasi-resonant supply performed flawlessly over its specified parameters, attaining the overall full load efficiency goal of 80%, however, only at low line. A decrease to 75% was seen as high line was approached, an indication that more attention to high dV/dt losses should be exercised. Nevertheless, low switching noise, quasi-sinusoidal power waveforms and substantially reduced EMI are worthwhile benefits, especially over conventional square wave converters. The relavent primary voltage and current, in addition to secondary voltage waveforms are displayed. These plots were obtained using a 250 MHz bandwidth digitizing scope, UHF measurement techniques and no bandwidth limiting or waveform averaging to distort the high frequency components.



Construction of the power conversion stage was accomplished using the Unitrode UC3860 demonstration kit printed circuit board, with ample facilities to accomodate a variety of quasi-resonant topologies and configurations. The control section was built using the UC3860 evaluation kit p.c. board, and interconnections to the gate drive and current sense transformers made with 75 ohm coaxial cables. An auxiliary winding from the main transformer and opto-coupled feedback were later added to this design for complete primary to secondary isolation.

SUMMARY AND CONCLUSIONS

The ultimate blend of high power density with high efficiency and low noise is realizeable today using quasi-resonant techniques, conventional topologies and existing components. In most applications, the upgrade is quite simple, as many of the devices go unchanged in the process. The control circuit, on the other hand, requires a far more sophisticated controller than for its square wave predecessors. Additionally, as switching frequencies are further pushed towards and beyond a megahertz, the needs for even higher performance and higher speed control logic become increasingly obvious. The UC3860 resonant mode controller exceeds these requirements, simiplifying and condensing the control circuit design process to resistor and capacitor value selections.

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4. INTERTEC COMM. PRESS, "Recent Developments in Resonant Power Conversion ", 1988-various authors and papers

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NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS

Bill Andreycak
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ABSTRACT

Although touted as a high impedance, voltage controlled device, prospective users of Power MOSFETs soon learn that it takes high drive currents to achieve high speed switching. This paper describes the construction techniques which lead to the parasitic effects which normally limit FET performance, and discusses several approaches useful to improve switching speed. A series of drivers ICs, the UC3705, UC3706, UC3707 and UC3709 are featured and their performance is highlighted. This publication supercedes Unitrode Application Note U-98, origionally written by R. Patel and R. Mammano of Unitrode Corporation.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFETs have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process, opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extemely fast switching. Not only is there no storage time inherent with MOSFETs, but the switching times can be user controlled to suit the application. This, or course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFETs are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSEFT can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell - a high power device such as the IRF 150 would have ~ 20,000 of these cells all connected in parallel.

In operation, when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N-drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N-drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

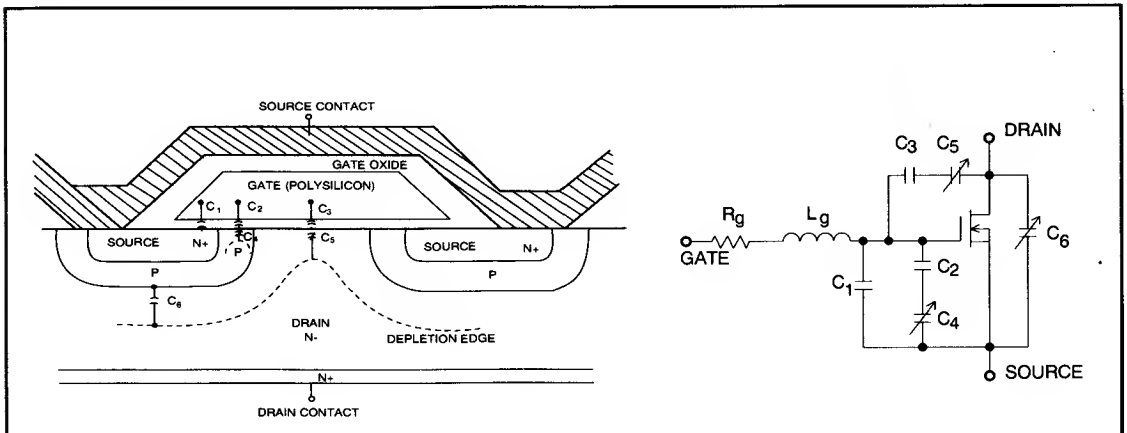

FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

In the equivalent model, the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is dielectric capacitance and is fixed while C4 is due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inducitve switching of a large class of applications and is implemented here with a IRF-510 FET, which is a 4 amp, 100V device with the following capacitances:

Ciss ≈ C1 + C4 + C5 = 135 - 150 pF

Crss ≈ C5 = 20 - 25 pF Vgs = 0V

Coss ≈ C5 + C6 = 80-100 pF

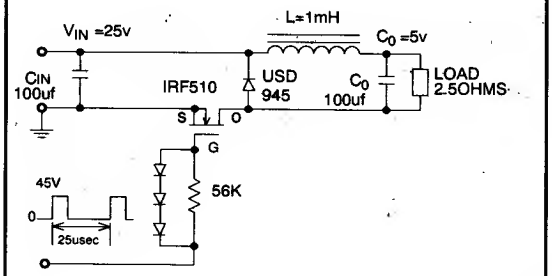

FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration, the load portion of the circuit is established with Vin = 25V. Io = 2A. and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

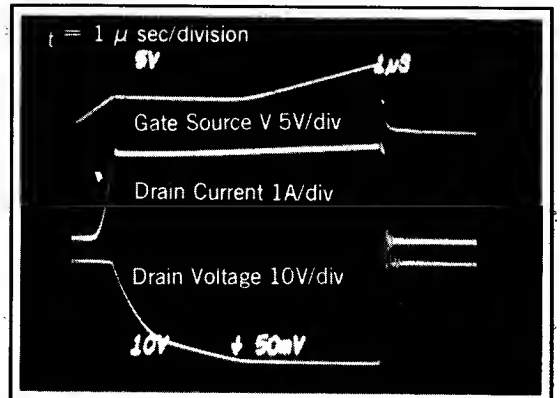

FIGURE 3-FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise tiime is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a significant jump when the drain-gate potential reverses polarity.

6. Unless limited circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold. C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transfered from the free-wheeling diode to the FET.

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

9

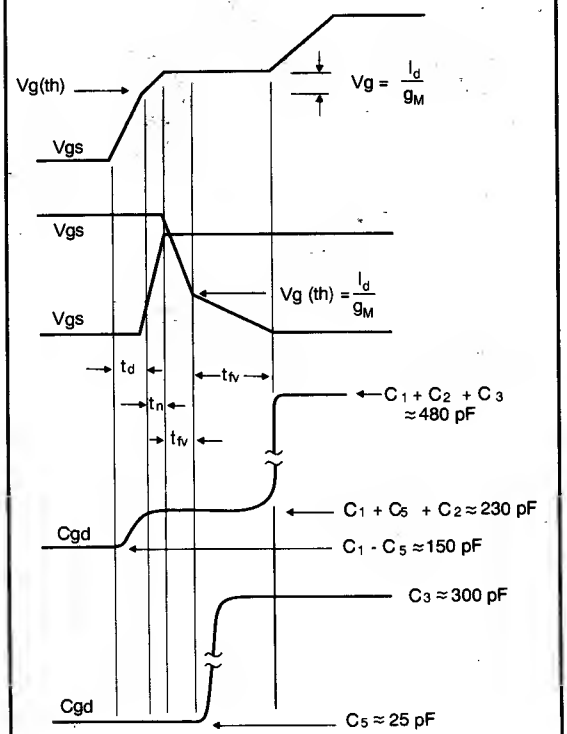

FIGURE 4 - Parasitic CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

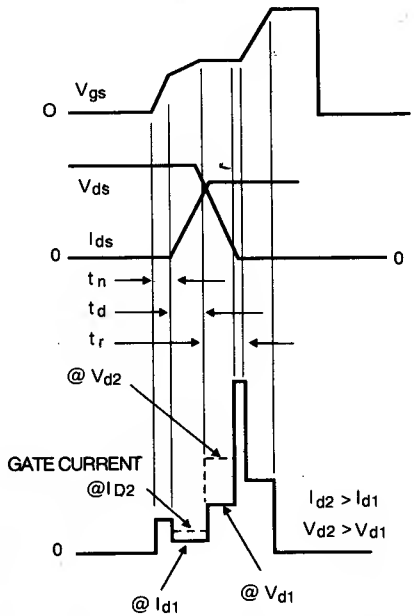

FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

AN OPTIMUM GATE DRIVE

In most switching power supplly applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements

1. An initial fast pulse to get the gate voltage up to threshold.

2. A lesser amount to slow the drain current rise time. This value however, will also be a functiion of the required drain current.

3. Another increase to get the drain voltage to fall rapidly wlth a large current pulse added when the drain gate potential reverses.

4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approximated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \qquad \text{where we define } ton = td + tn + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg\,(th) - \frac{Id}{g_M}] - Crss\,[V_{DD} - Vg\,(th)] - Crss\,V_g\,(th)$$

While directly connecting the FET gate to the output of the driver is straightforward for testing purposes, it does not represent the "real" application which may include several inches or wire or printed circuit board traces. Here, wiring inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. Extreme examples of this can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings.

Additionally, negative transitions (below ground) at the deriver output can raise havoc with the internal circuitry, leading to undesireable performance. While this is more of a concern with PWMs, (which use low level analog input signals) it will also detract from the drivers peak performance. Both of these conditions can easily be avoided by Schottky clamping the circuit to the auxiliary supply rails.

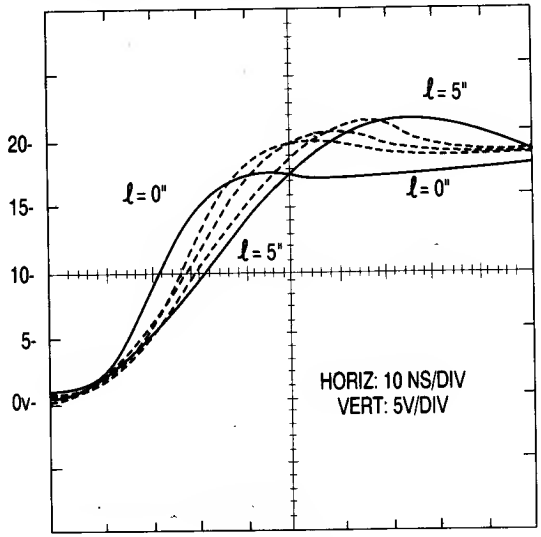

Figure 18

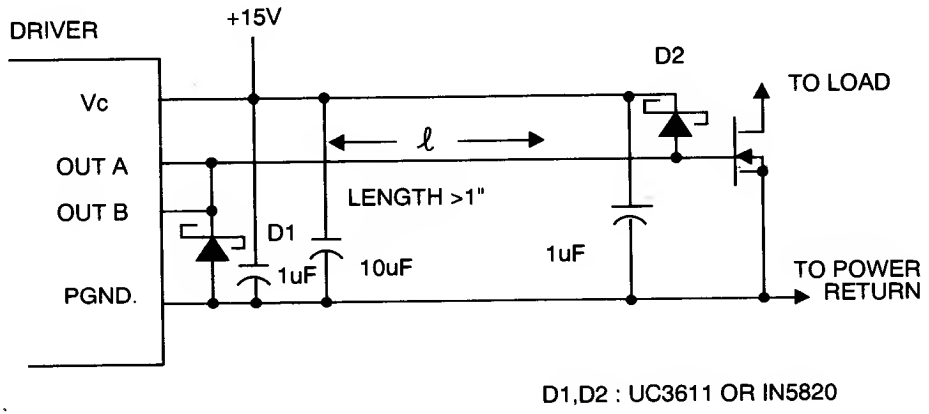

Figure 19

available FET die (a size "6") at the time of this writing whose specifications were listed previously.

The typical values of each charge will later be used in conjunction with the measured driver performance to estimate the actual peak current delivered during each interval of turn-on. The tests shown were conducted at room temperature with the FET located directly at the IC output pins to nullify any effects of series inductance. Additional tests and measurements will demonstrate the effects of circuit inductance on gate driver performance.

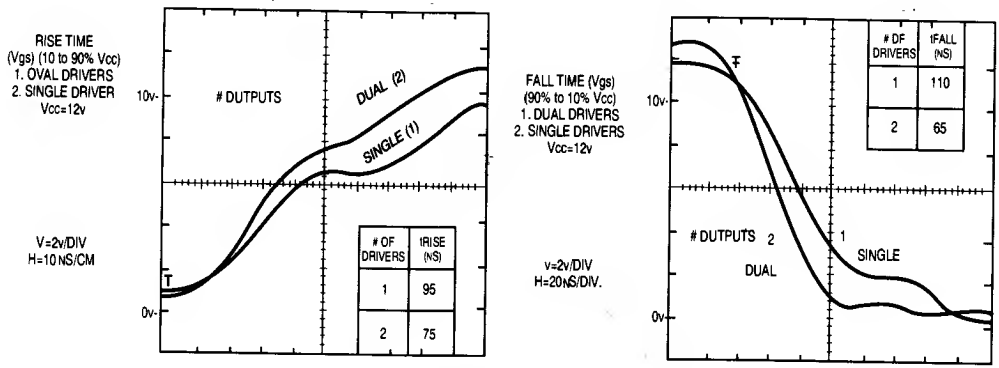

Figure 17

AVERAGE DRIVER CURRENTS DURING TURN-ON & TURN-OFF INTERVAL

EQUATIONS: $Q = CV$; $Q = IT$; $i_{AVG} = \frac{C.V}{T}$

During the transitions between 0 & 10V over Tr & Tf intervals

SINGLE OUTPUT

LOAD	RISE	FALL
C = 2.2NF	0.49A	0.67A
C = 10NF	1.43A	1.43A
IRFP460	1.26A	1.10A

DUAL OUTPUTS

LOAD	RISE	FALL
C = 2.2NF	0.63A	0.88A
C = 10NF	2.0A	2.22A
IRFP460	1.6A	1.85A

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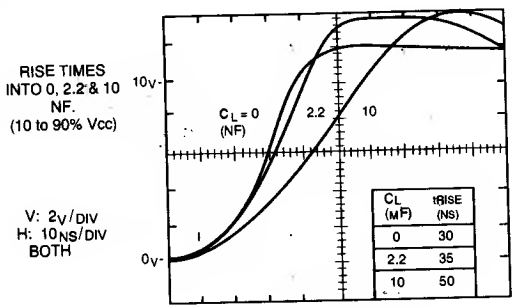


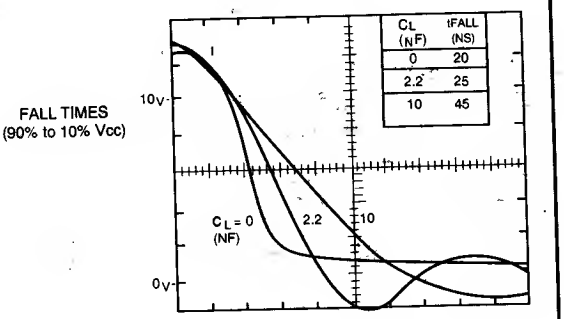
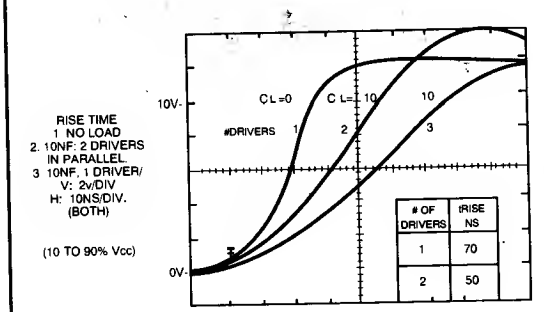


Figure 14



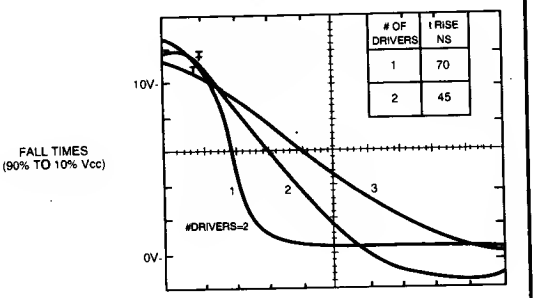


Figure 15

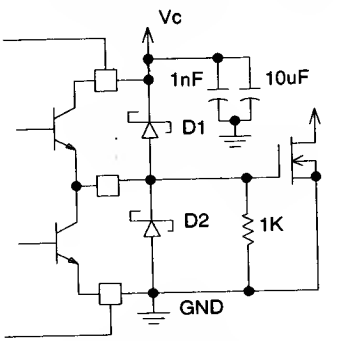
The peak current of each totem-pole output, whether source or sink, is 1.5 amps. However, on dual output versions like the UC3706, UC3707 and UC3709, both of the outputs can be paralled for 3 amp peak currents. In close proximity on the same die, each output virtually shares identical electrical and thermal characteristics. Saturation voltage is high at this current level but falls to under 2V at 500ma per output. Examples of typical switching characteristics are displayed.

It should be noted that while optimized for driving power MOSFET device, the UC3705 /06 /07 /09 ICs perform equally well into bipolar NPN transistors. In a steady-state off condition, the output saturation voltage is less than 0.4 volts as currents to 50 milliamps.

DIRECT COUPLED MOSFET DRIVE

The circuit of figure 17 shows the simplest interface to a power mosfet, direct coupling. In this example, an IRFP460 will be used to demonstrate the typical rise and fall times obtainable with a single 1.5 amp peak totem-pole driver. Further testing will include paralleling both outpus of a dual driver for a 3 amp peak capability. The IRFP460 device was selected, being the largest commercially

POWER MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODES

Figure 16

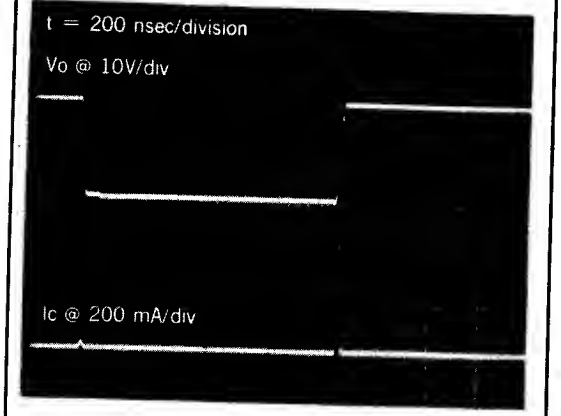


Figure 11

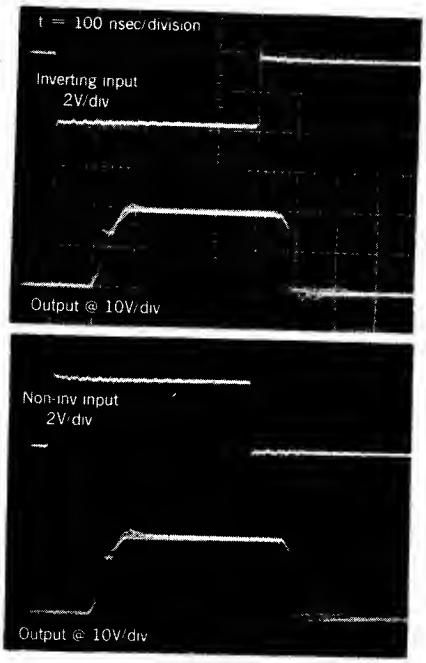


Figure 12

The overall transition time through the UC3706 is shown in figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20 nSec delay in turning off when the non-inverting input is used. Here, and in further discussions note that ON and OFF relate to the driven output switch, i.e., On is with the output HIGH, and vice versa. The shutdown, inhibit and protective functions all force the output LOW when active.

Note that the typical rise and fall times of the output waveform average 20 nsec with no load, 25 nsec with 1 nF, and 35 nsec when the capacitive load is 2.2 nF at room temperature. Multilayer ceramic capacitors are used in this test and located as physically close to the IC output as possible to minimize lead and connection inductance.

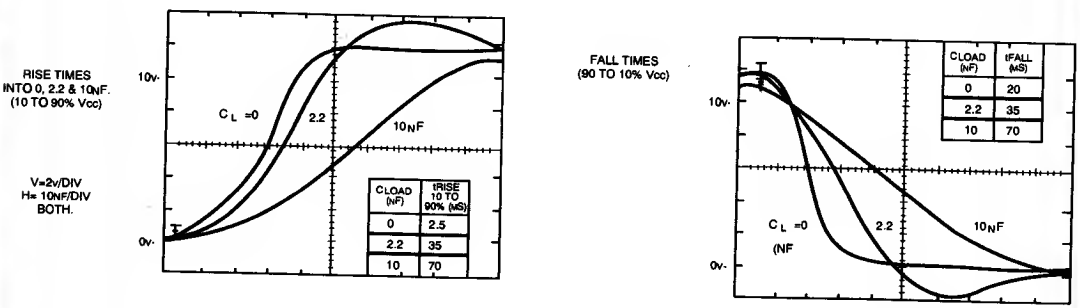
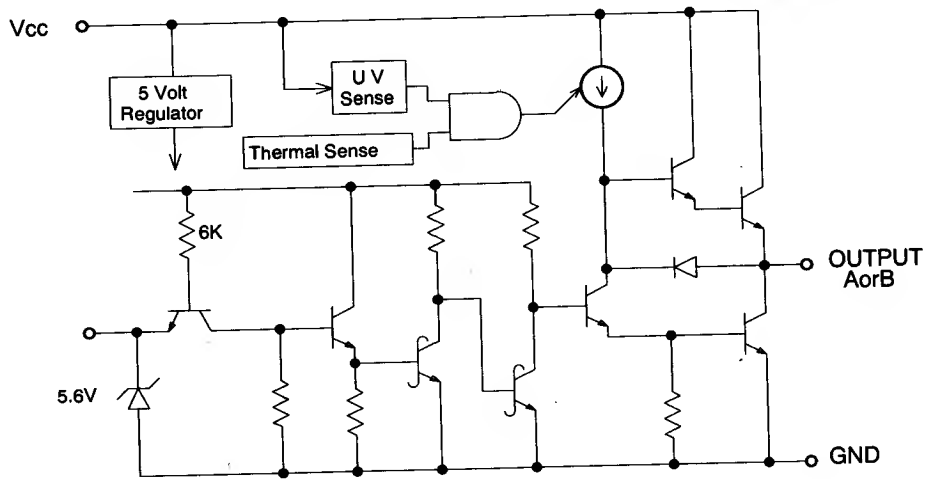


Figure 13

UC3709 Block Diagram



NOTE: One Output Shown

Figure 9

DRIVER FEATURES

- 1.5 Amp Peak Output Current (Per Output)
- 40 Nanosecond Rise & Fall Times into 1NF
- Low Cross Conduction Current Spike
- 5 to 40 Volt Operation
- High Speed Power MOSFET Compatable
- Thermal Shutdown Protection

	DUAL OUTPUTS	INVERTING INPUTS	NON-INVERTING INPUTS	SEPERATE V_C & V_{IN}	SEPERATE PGND & SGND	ANALOG SHUTDOWN	DIGITAL INHIBIT	TOGGLE F/F	LATCH RESET
UC3705		X	X	X	X				
UC3706	X	X	X	X	X	X	X	X	
UC3707	X	X	X	X	X	X	X		X
UC3709	X	X							

1.5 AMP PEAK TOTEM-POLE OUTPUTS

The schematic of the UC3706 output drive circuit is shown in figure 10, which is similar to the other devices in this family. While first appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in figure 11 where it can be seen that while maintaining fast transition times, the cross conduction current spike has been reduced to zero when going low and only 20 nsec with a high transition. This offers negligible increase in internal circuit power dissipation at frequencies in excess of 500KHz.

Typical Output Schematic

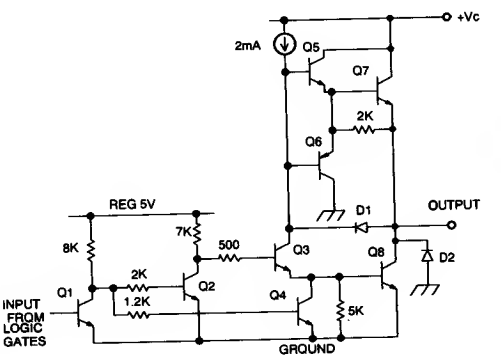


Figure 10

UC3706 Block Diagram

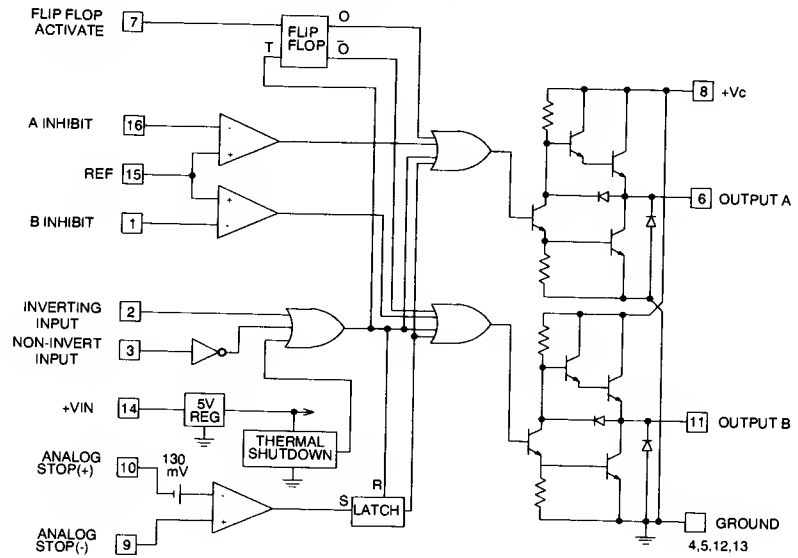


Figure 7

UC3707 Block Diagram

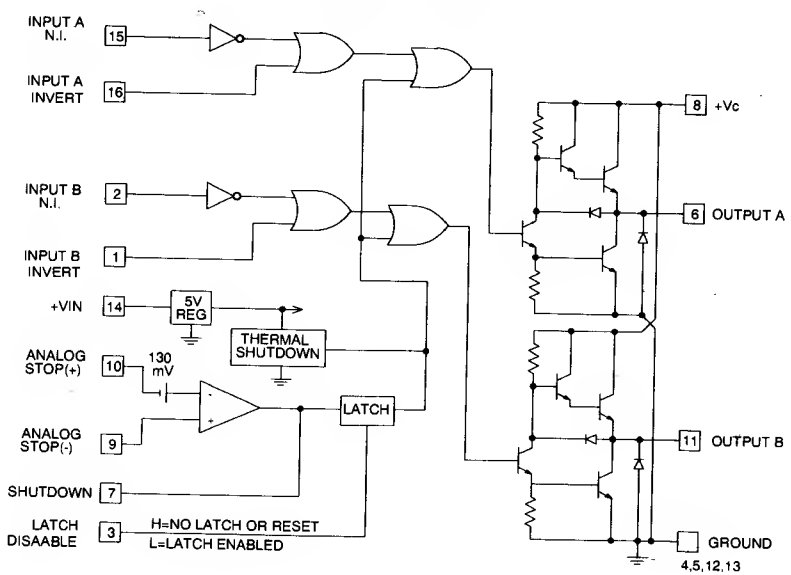


Figure 8

9

effecive gate capacitance over the Qgd interval since there is relatively no change in gate voltage. The important fact, however, is that high peak currents are needed to minimize the FET power loss and transition time.

The remainder of the gate charge brings the gate voltage from VGS (th) to 10 volts. This "excess" charge reduces the FET "ON" resistance to its minimum, and raising the gate voltage above 10 volts has no further effect on reducing the Rds (on). The effective gate capacitance, which is high, can be obtained by dividing the charge input by the change in gate voltage during this region.

Ceff = [Qg - (Qgd+Qgd)] / (10v - VGS (th)) = 40nC/4v = 10nF for the IRFP460

FET DRIVER ICS

In searching for IC's capable of providing the fast transitions and high peak currents required by power MOSFETs, one of the first devices which became popular was the DS0026. While this IC was origionally designed to be dual clock driver for MOS logic, it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all NPN process which minimizes storage delays, and as a result, offers transition times of approximately 20 nsec. Its disadvantages, however, are high cross conduction currents, as well as requiring excessive supply current when the output is in the low (OFF) state. This leads to higher power dissipation and junction temperature than optimum.

This brings us to newer ICs designed specifically as power MOSFET drivers for switchmode power supply applications. Several factors were taken into consideration while developing the new UC3705 /06 /07 /09 series of high current drivers; the most important of which, was to isolate the high power switching noise from the low level analog signals at the PWM. Seperate supply and return paths at the driver to its signal inputs and power outputs further enhances noise immunity. Additionally, several desireable features including an analog shutdown comparator have been incorporated in the UC3706 and UC3707 devices, whereas the UC3705 and UC3709 drivers are optimized for low cost applications which incorporate this function elsewhere in the design. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross-conduction, high speed output circuitry. The corresponding block diagrams and pin assignments are shown in figures 6 thru 9, and followed by the feature selection index.

UC3705 Block Diagram

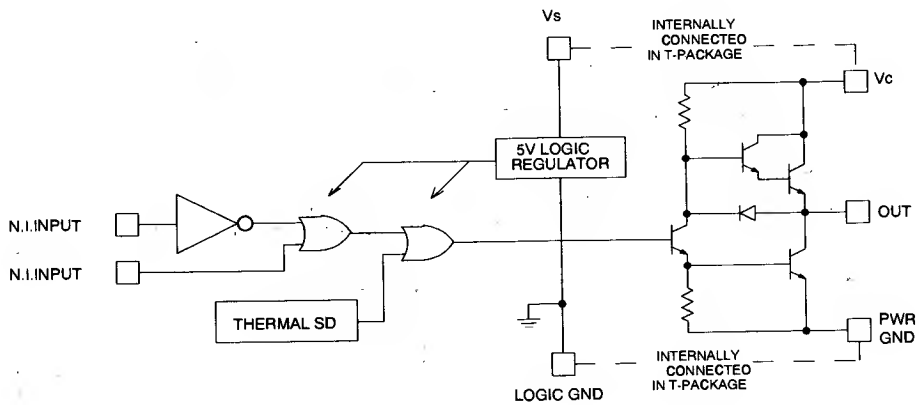


Figure 6

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'=1.5 Ciss. With this assumption.

$$Ip \approx \frac{2}{ton}[Ciss\,(2.5Vg\,(th) + \frac{Id}{g_M}) + Crss\,(V_{DD} - Vg\,(th))]$$

As an example, if one were to implement a 40 V. 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimum drive current for this application would then take 50 nsec to ramp from zero to peak value calculated from

$Ciss = 2000pF$ $ton = 50nsec$
$Crss = 350pF$ $V_{DD} = 40V$
$Vg\,(th) = 3V$ $Id = 10A$

$$g_M = \frac{10A}{2.5V} = 4s$$

$$\text{as } Ip = \frac{2}{50 \times 10^{-9}}\,[2000 \times 10^{-12}\,(2.5 \times 3 + \frac{10}{4}) + 350 \times 10^{-12}\,(40 - 3)]$$

$\therefore Ip = 1.32$ *amps peak*

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

TOTAL GATE CHARGE (Qg)

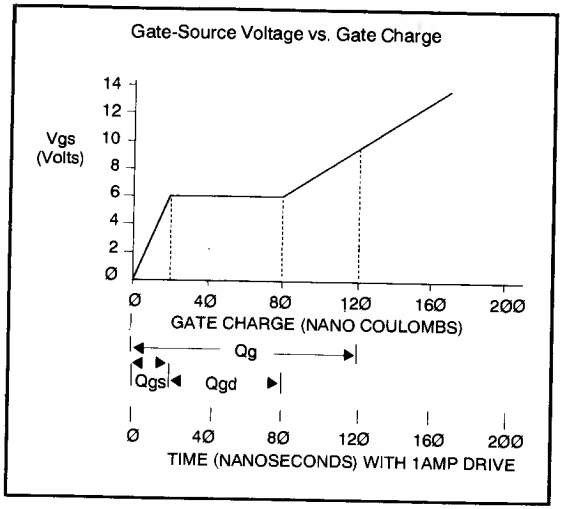
Another approach used to quantify and understand MOSFET gate drive requirements is much simpler than that of examining the instantaneous voltages, currents and capacitances. The term "Total Gate Charge", or Qg specifies the amount of gate charge required to drive the FET gate-to-source voltage (Vgs) from zero to ten volts, or vice-versa. For most high voltage devices, these thresholds correspond to the FET being either completely on or off.

Charge (Q) can be expressed as the product of either current multiplied by time (I*T), or capacitance multiplied by voltage (C*V) in the units of Coulombs. Most contemporary devices have total gate charge requirements in the tens to low hundreds of nano Coulombs, dependent almost entirely on die's geometry. For example, an IRF710 (size 1) FET has a total gate charge requirement of only 7.7 nC whereas the IRFP460 (size 6) demands 120 nC, and both are typical values.

PARAMETER	IRFP 440	IRFP 450	IRFP 460
Qgs (NC)	6.2	11	18
Qgd (NC)	22	43	62
Qg (NC)	42	86	120
Ciss (Nf)	1.3	2.7	4.1

There are two specified parameters contained within the total gate charge expression; Qgs, the gate-to-source charge, and Qgd the gate-to-drain, or "Miller" charge. Qgs is the amount of charge required to bring the gate voltage from zero up to its threshold VGS (th), of approximately 6 volts. Qgd defines the amount of charge that must be input to overcome the "Miller" effect as the drain voltage falls. This occurs during the plateau of the gate-to-source voltage waveform where the voltage is "constant". Excess charge is added to lower the effecive Rds (on) until the gate voltage reaches 10 volts, wher Qg is specified. Further increases above this level do NOT lower Rds (on), so a 10-12 volt driver bias is ideal.

The total charge curve can be examined in sections to define the ideal driver's characteristics. Using a constant current of 1 ampere, the total charge curve (Qg=I*T) in nanoCoulombs also represents the MOSFET turn-on delay, drain current rise and drain voltage fall times in nanoseconds.



First of all, and most importantly, the average capacitive load represented by the FET to the IC driver is NOT the specified MOSFET input capacitance, Ciss. The effecive input capacitance, Ceff, is the total charge divided by the final gate voltage, Vgs(f);

Ceff = Qg(total) / Vgs(f).

Using the total gate charge curve show above, the 460 FET with Vds (off) = 400 volts has an effective input capacitance (Ceff) of approximately 120nC/10v, or 12 nF during the interval of 0 < Vgs < 10v. The specified input capacitance of Ciss = 4.1nF applies only at Vgs=0, and is often mistaken for the driver's actual load.

The Qgs portion of the curve is primarily governed by the driver's ability to quickly turn ON. Therefore, a sharp, fast transition of the totem-pole output from low to high is essential to minimize the delays from 0 < Vgs < VGS (th). In most applications the driver IC is not peak current limited during this interval, since its is more likely to be dV/dT limited. The effective gate (load) capacitance is approximately Qgs / VGS(th), or Ciss.

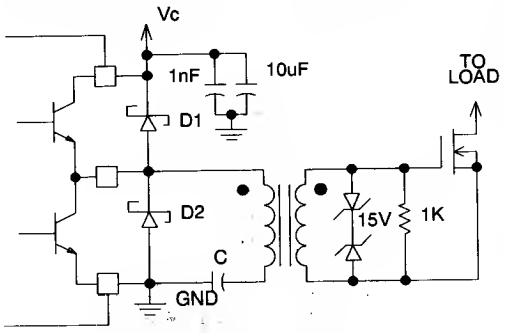
Evident from the charge specifications, most of the popular size FETs used in switch-mode power supplies (sizes 4. 5 and 6) have much larger Qgd demands than their gate-to-source counterpart, Qgs. During this Qgd interval, the gate voltage remains "constant" while gate charge accumulates and the drain voltage collapses. It is also during this period that most drive circuits are simply peak current limit, whether by the driver IC or an external resistor. High peak currents are necessary for fast transitions through this interval, especially when driving large geometry FETs.

Full drain current is flowing at the beginning of the Qgd portion of the Qg curve, and notice that the drain voltage remains high. FET power loss is at its maximum here, and decreases linearly with Vds. A majority of the Qgd charge goes to combat the "Miller" effects as the drain voltage falls from that of its off condition to Vgs, or approximately Vgs(th). The remainder of the charge is used to bring the drain voltage down below that of the gate, decreasing the

ISOLATED GATE DRIVE

In certain applications, the PWM is referenced to the load or secondary side of the power supply and the gate drive is transformer coupled across the isolation boundary to the power FETs. While this technique may work adequately at low switching frequencies, any series circuit inductance, as shown, will significantly degrade switching speeds and performance as the frequency is increased. An improved version of this circuit locates the drivers on the primary side, as close as possible to the FETs, and transformer couples only the low power input signals. Although somewhat more elaborate, significant improvements in turn-on and turn-off switching times are obtained and the FET switching losses are minimized.

TRANSFORMER COUPLED MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODE ARRAY

Figure 20

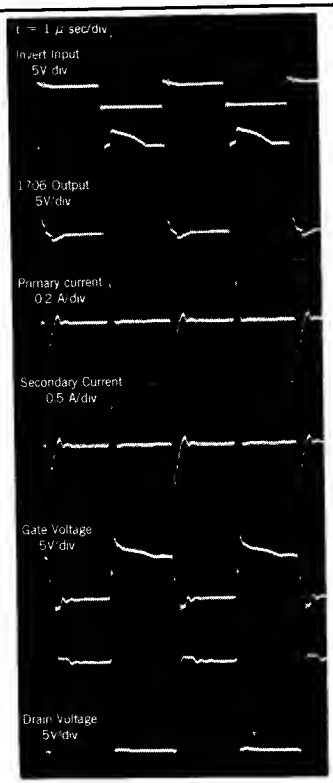


Figure 21

IMPROVED XFMR COUPLED DRIVE CIRCUIT

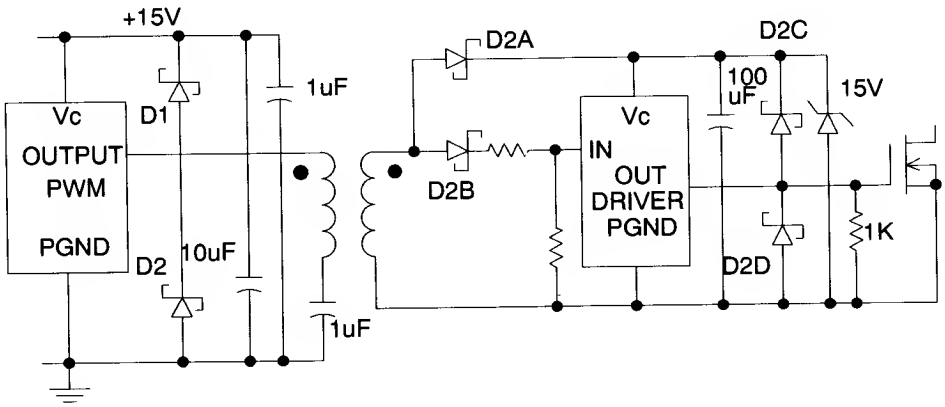


Figure 22

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC3706 can easily be configured for implementing the balanced transformer drive as shown in figure24. Outputs A and B are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC3706 output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back-to-back zeners on the secondaries are necessary to minimize the overshoot causes by the ringing of the gate capacitance with circuit inductances. Waveforms of all significant points within this circuit are shown.

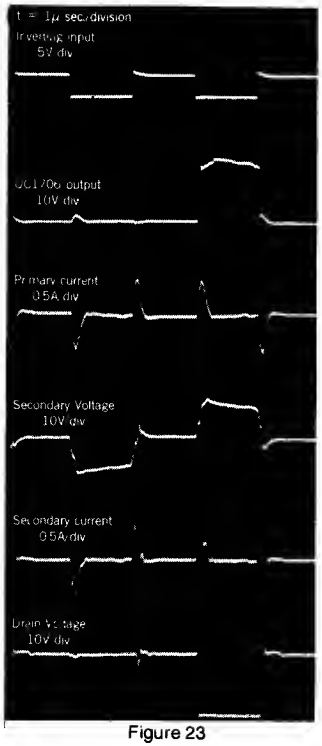


Figure 23

UC 3706 CONVERTS SINGLE OUTPUT PWMS TO HIGH CURRENT PUSH-PULL CONFIGURATION

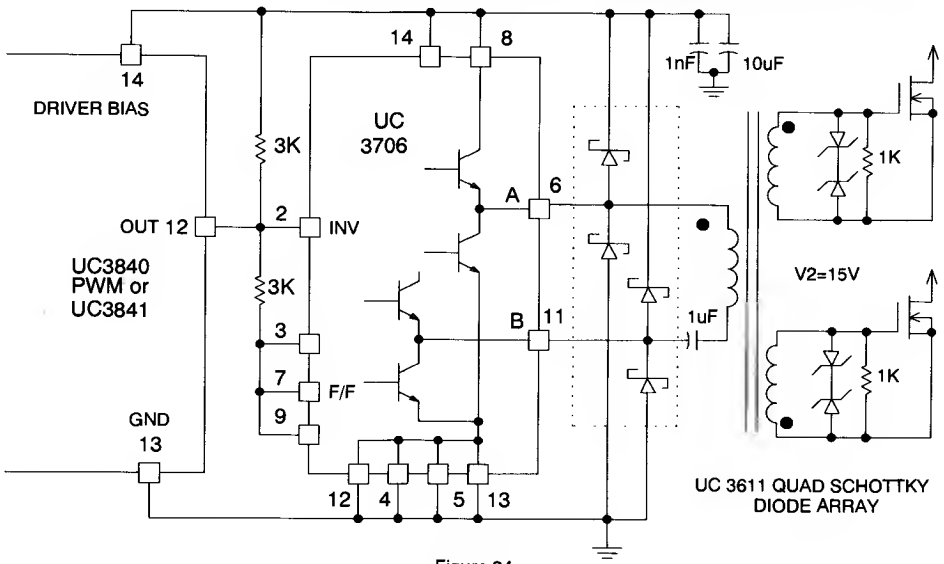


Figure 24

SUPPLYING POWER TO THE DRIVERS

From the block diagrams of figures 6 thru 8, note that the UC3705, UC3706 and UC3707 have two supply terminals, Vin and Vc. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Therefore, Vin can also be used to activate the outputs and no current is drawn from Vc when Vin is low. This is useful in off-line applications where its desireable for the control circuit to have a low start-up current. Several PWM controllers, like the UC1840, UC1841 and the UC1851 feature a Driver Bias output which goes high once the undervoltage lockout threshold is crossed, thus supplying bias to the driver. Adaptations of this technique can be made to work with a variety of other PWMs and control circuits.

USING "SPLIT" SUPPLIES

Many applications utilize a negative voltage rail in the drive circuit to guarantee complete turn-off of power MOSFETs, especially those with low gate threshold voltages, typical of "logic level" input devices. This is easy to implement with any of the UC3705 thru UC3709 drivers by offsetting the input signals with a zener diode equal in voltage to the negative supply, Vee. Although referenced at the driver IC to the Vee rail, these inputs are offset by an equal amount to the PWM controller, simulating a ground referenced input. This technique also offers moderate improvements in FET switching speeds at the penalty of slightly increased effective delay times from the driver inputs. The end results are listed below, which may be beneficial in applications where a tailored gate drive is required to alter the MOSFET switching charcteristics.

POWER MOSFET DRIVE CIRCUIT
USING NEGATIVE BIAS VOLTOGE AND LEVEL SHIFTING
TO GROUND REFERENCED PWMS

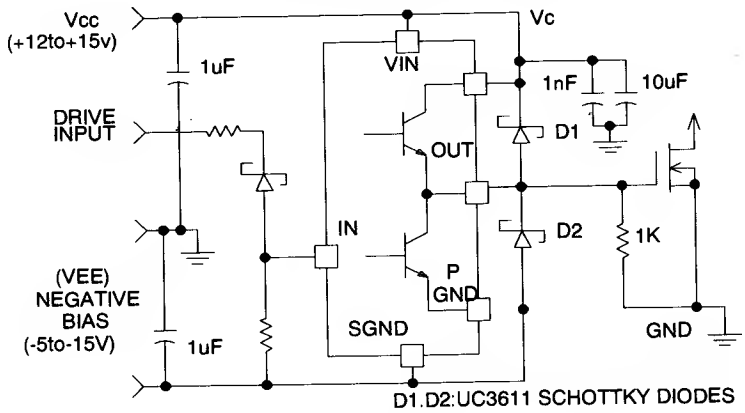
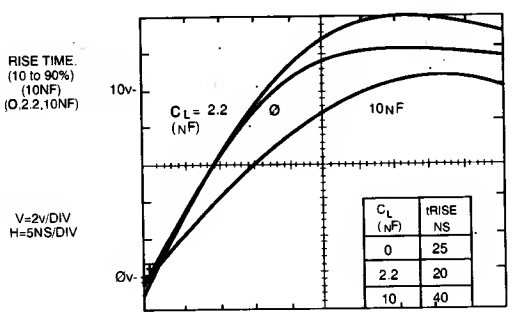


Figure 25



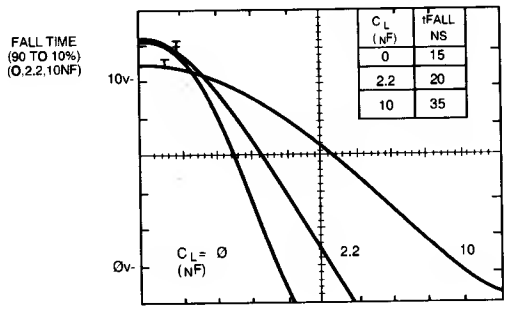


Figure 26

9

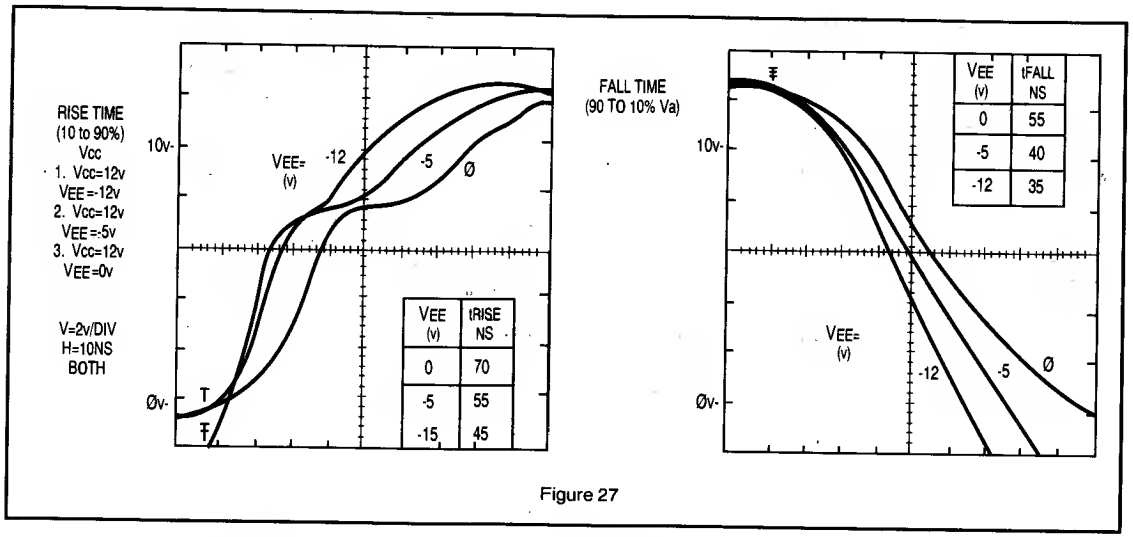


Figure 27

VEE (V)	td Rise to "0" V (NS)	T Rise 0-10V (NS)	Td Fall to begin (NS)	T Fall 10-0V (NS)I	T Delay total (NS)	Tr & Tf total (NS)	T Total tr+tf+trd (NS)
0	56	50	50	45	106	95	201
-5	70	42	50	33	120	75	195
-10	86	34	50	29	136	63	199
-12	93	32	50	28	143	60	203
-15	100	30	50	27	150	57	207

VEE (V)	Delay trd+tfd (NS)	Transition Times tr+tf (NS)
0	Minimum (106NS)	Maximum (95NS)
-15V	Maximum (143NS)	Minimum (60NS)

VEE (V)	Rise	Fall
0	2.4A	2.67A
-5	2.86A	3.64A
-10	3.53A	4.14A
-15	4.0A	4.4A

SUMMARY

This paper has presented an understanding of the dynamics of high speed power MOSFET switching in an attempt to define the optimum gate drive requirements to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed towards achieving these goals. The UC3705, UC3706, UC3707 and UC3709 drivers provide high speed response, 1.5 amps of peak current per output and ease the implementing of either direct or transformer coupled drive to a broad range of power MOSFETs. With these new devices, one more specialized function has been developed to further aid the power supply designer simplify his tasks and enhance power MOSFET switching characteristics.

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DRIVING THREE-PHASE BRUSHLESS DC MOTORS — A NEW LOW LOSS LINEAR SOLUTION

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John J. Galvin, Control Systems Eng, Quantum Corp.

ABSTRACT

A new linear driver for small Brushless DC motors has been developed which has the capability of maximizing the voltage delivered to the motor while additionally providing commutation logic and full control. By using discrete PNP high-side transistor switches in conjunction with integrated saturable NPN low-side drivers, less than one volt total loss can be achieved at currents up to two amps, and complete motor control can be derived from only a five volt power source.

BRUSHLESS DC MOTORS

Although the world has long known of the myriad problems with brush-type DC motors, the development of electronically commutated, or "Brushless" (BDC), motors has not been a simple transition. While Hall Effect sensors have developed to the point where accurate and reliable armature position information can now be readily derived, the problems of amplifying these low-level signals, applying them to the appropriate winding, and then driving that winding with an efficient power transfer still represent a significant challenge. Particularly when this intervening circuitry - none of which was required with brush-type motors - also has to be reliable, very low cost, noise free, and take up minimal space. The problem is further compounded by the need to provide three-phase drive for all but the simplest, specialized motors in order to accommodate bidirectional rotation and wide variations in speed and load.

For complete control of a brushless DC motor, the circuitry must provide at least three functions:

1. Commutation logic to generate the correct phase timing from the Hall sensors. In most cases, this is implemented as a digital decoding function.

2. Power drivers for each of the three output phases. The challenge here is finding a solid state switch as efficient as the old commutator brush.

3. Control circuitry to give the motor some intelligence. This usually means controlling motor current in response to commands based on speed, position, torque, or some other measurable output.

THE SPINDLE DRIVE PROBLEM

Providing the above functions as a spindle driver for rotating memories represents an additional challenge as disk drive users have come to expect the package density and low costs of an integrated driver while at the same time demanding ever higher operating efficiencies to minimize the requirements on power supplies and heat sinks.

While discussing drive efficiency, it is worth noting that disk drives add a further restriction due to the magnetic media and low signal levels involved. This is that the use of switch-mode technology to increase power control efficiency is usually forbidden out of concerns for possible high-frequency EMI noise. Ruling out switch-mode techniques leaves the designer faced with the problem of providing maximum efficiency with linear current control, and thus his quest for power savings can only be directed toward minimizing the drop across the output switches in order to use the highest efficiency motor.

THREE PHASE MOTOR DRIVE

The drive stage for a typical brushless DC motor is shown in Figure I where the motor is shown wound in the "Y" configuration. A "delta" form is equally applicable and would make no difference to the switches. The driving problem is immeadiatly apparent in that there are six separate switches required and two are in series with any current path through the motor. With a 12 volt supply and typical bipolar darlington switches - each with a probable 1.5 volt drop - the maximum voltage to the motor is nine volts and one fourth of the input power is lost in the switches.

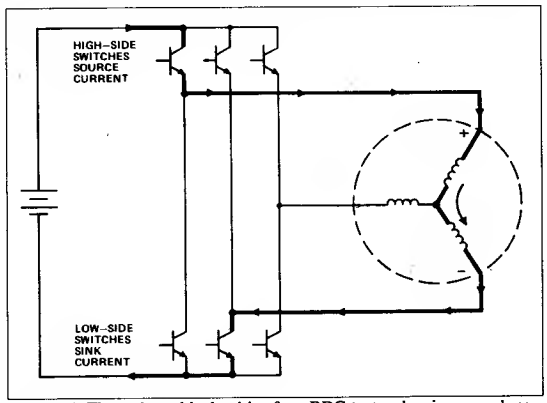

Figure 1: Three phase, bipolar drive for a BDC motor showing one phase of current flow.

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These switch voltage drops have added significance in terms of optimizing the motor design since the maximum current through a given motor is defined by the difference between the voltage applied to the motor and the back EMF generated while it is running. Reducing the voltage drop across the switches allows the use of a motor with a higher torque constant and correspondingly higher back EMF which results in a lower motor current for the same load. Since the power loss in the motor is equal to I^2 times the wire resistance, the gain in overall efficiency is more than proportional. For example, with a three volt switch drop from a 12 V supply, an optimum motor choice might have a back EMF of 8 V and require 4 W of power from the supply to do 2.7 W of work. Reducing the switch drop to one volt would now allow a motor with a back EMF of 10.2 V to be used which, with all other factors remaining unchanged, would require only 3.16 W to do the same work. In other words, a 22% increase in the voltage applied to the motor can result in a 27% increase in motor efficiency. This is in addition to saving 2/3 of the power lost in the switches.

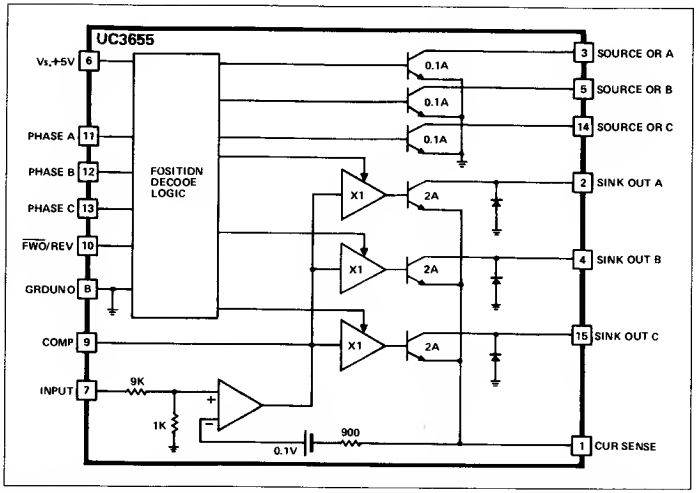

Figure 2: The UC3655 IC provides decode logic, high-current low-side linear drivers under the control of an internal amplifier, and switches to activate high-side, external PNP transistors.

While power MOSFET technology has the potential of offering lower switch losses in discrete form, an integrated monolithic FET structure, while technically feasable, may well be economically impractical. An integrated bipolar transistor scaled for a Vsat of 0.4 V at one amp requires approximately 2000 square mils of silicon, while an integrated DMOS transistor with an Rds(on) value of 0.4 ohms would be closer to 5000 square mils. And it takes six transistors to build a three phase driver. Therefore, a more cost-effective solution would indicate the use of bipolar transistors, but as single saturating switches - not darlingtons.

The low-side switches of Figure 1 are easily integrated in this form as power NPN transistors with their base currents derived efficiently from a five volt power supply. The high-side devices are more of a problem, however, as these need to be PNP transistors to achieve the same low-sat performance, and isolated power PNP transistors are still not compatible with an integrated bipolar process. Thus the decision made for the motor driver described herein was to supply the PNP's as external, discrete saturating switches while the rest of the control circuitry was integrated into a single power IC. The result is the UC3655 illustrated in the block diagram of Figure 2.

THE UC3655 LINEAR BDC MOTOR DRIVER

This device achieves efficient operation by allowing the external PNP's to be selected for the specific application, while internally generating a switched base drive of up to 100 mA - adequate for motor load currents of at least 3 Amps. Because the PNP's are always driven into saturation, their power dissipation will usually be low enough to require no special heat sinking and, in many cases, they may not even need power packages. The only specification of significance for these devices is their saturation voltage for a given base drive. While bipolar PNP transistors are used throughout in this paper, it should be clear that this is a cost consideration and P-channel FET devices could be used as well with the benefit of reduced drive power losses.

The current-limited darlington circuit used for each of the three PNP drivers is shown in the upper portion of Figure 3. This driver is activated by the digital signal from the Channel Select Logic which is defined to allow only one PNP to be on at a time. Note that the total supply current for this stage is a constant 100 uA from the five volt supply for each output.

Each of the low-side motor drivers shown in Figure 3 are, of course, integrated power NPN transistors scaled for a maximum output current of three amps with a very low saturation voltage

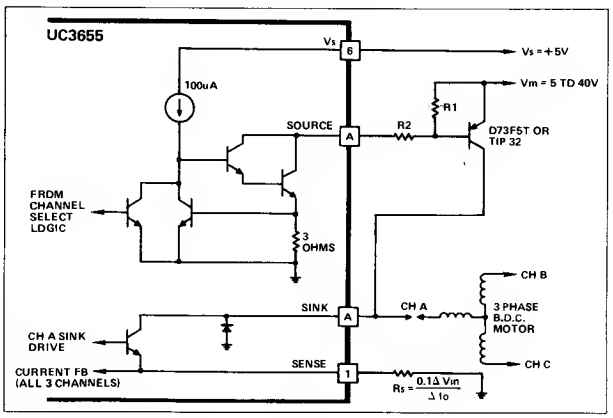

Figure 3: Interfacing the UC3655 to a BDC motor.

drop. At full load, these transistors may need a base drive of up to 50 mA which must come from the five volt supply; however, since they are also used as the means to control the motor current, the action of the control amplifier reduces the base drive as it commands less motor current. The overall schematic of both the amplifier and one of the three low-side drivers is shown in Figure 4.

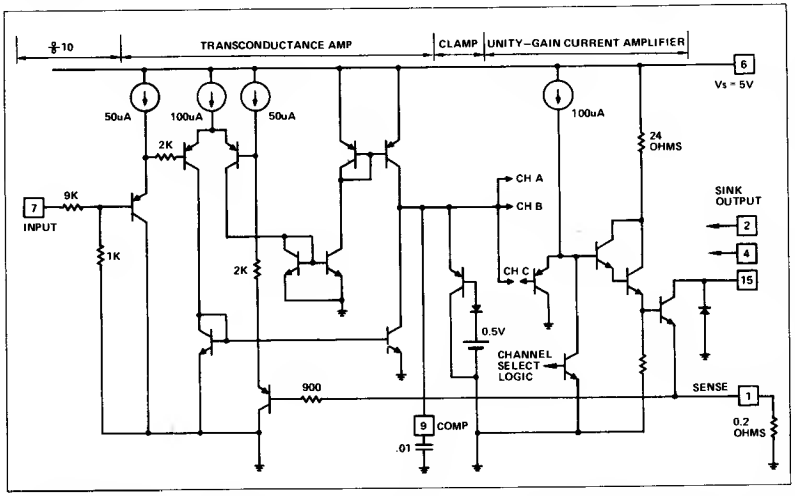

Figure 4: Control of the motor's current requires the four functions shown above, plus the decode logic to define which of the three outputs is active.

This circuitry includes an internal feedback loop to configure the transfer function as a transconductance amplifier controlling motor current from a voltage command. For full control, four functions are included:

1. An input divide-by-ten attenuator to scale a four volt input command range on Pin 7 to a 400 millivolt range across the current sense resistor connected to Pin 1.

2. An amplifier to provide voltage gain. This is also a transconductance type so that the feedback loop may be easily stabilized by a single capacitor from its output on Pin 9 to ground. There is a 100 mV offset built in so that, in conjunction with the input divider, zero output current is commanded with a one volt input.

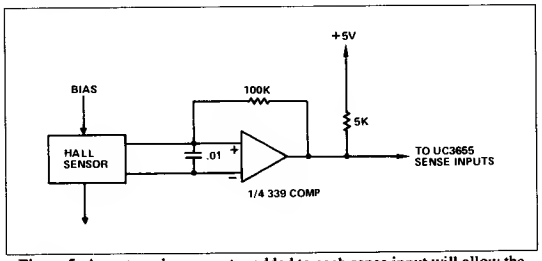

Figure 5: An external comparator added to each sense input will allow the use of low-level, analog Hall sensors.

3. A unity-gain output stage (to the sense resistor) provides the high current output drive with a high input impedance so that the transconductance amplifier is not unduly loaded. Note that the analog command input is gated by the Channel Select Logic so that only one output is on at a time with the other two drivers draining only 100 uA apiece from the supply.

4. A clamp on the output of the transconductance amplifier limits the voltage drop across the sense resistor to approximately 500 mV and thereby provides some measure of over-current protection.

The remaining portion of the UC3655 consists of the decode logic to generate the proper output switch timing from the Hall sensor position indicators. This logic is easily mask programable for other than the standard 60 degree output phasing. The input circuitry to these Channel Select stages has a high impedance, stabilized threshold of 1.5 V and is designed for single-ended, digital-output Hall sensors. For maximum flexibility, pull-up resistors are not included but in niosy environments, should probably be added externally. Where analog, two-terminal Hall sensors are used, the comparator circuit of Figure 5 can be used at each input to give fast, clean transitions.

A fourth input to the decode logic is the direction function addressed through Pin 10. This input circuitry, shown schematicly in Figure 6, has three states:

1. A low input pulls REV low and FWD high, setting up the decoding for a forward rotation.

2. A high input reverses the states of REV and FWD, which the logic decodes as a command for the opposite direction of rotation.

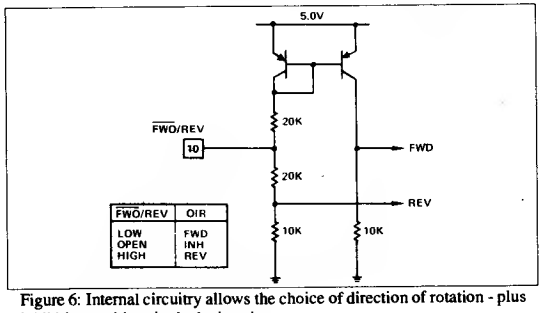

Figure 6: Internal circuitry allows the choice of direction of rotation - plus inhibiting - with a single device pin.

3. If the input is open - or connected to a voltage between 1.8 and 3.2 volts - both FWD and REV are high which the logic defines as a coast condition with all six outputs off.

All outputs are also inhibited if the three Hall inputs are all in the same state, either high or low.

While no braking function is built into the UC3655, it is entirely feasible to provide a rapid deceleration by switching the direction command from FWD to REV with the only precaution being to allow the output transistors to turn off while the command is passing through the INH region. Typically, this might require a 10 usec delay which is easily accommodated with either digital or analog techniques.

It can be seen from the block diagram of Figure 2 that the only supply voltage connection to the UC3655 is a single 5 volt source. From this supply, the quiescent current is less than 10 mA with the outputs inhibited and increases with motor current to approximately 25 mA with a two amp load. The motor voltage is defined by the supply used for the emitters of the PNP transistors and can range from 5 V to 40 V. Note that with this design, a 5 V supply could deliver more than 4 V to the motor - a difficult task for any other integrated circuit topology.

Finally, this device includes the protection of undervoltage lockout, with a threshold of 4.2 V, and thermal shutdown when the junction temperature rises above 150°C. Since the UC3655 is a linear driver, the potential for high dissipation is possible but a Multiwatt power package with adequate heat sinking will accommodate up to 25 watts. For smaller motors, a power 28-pin surface-mount, PLCC configuration with 4 watt capability will be offered.

INTERFACING TO THE MOTOR

The schematic of Figure 3 illustrates the added components necessary to interface the UC3655 to a typical BDC motor with the other two outputs identical to that shown. While resistor R1 serves merely to speed the turn off of the PNP transistors, R2, while optional, serves two functions: It can reduce the PNP base current to less than the internally limited 100 mA, and it absorbs the PNP base drive power losses which would otherwise add to the IC package dissipation.

In driving a BDC motor, there is no concern for cross-conduction current flow where both an NPN and a PNP experience overlapping conduction during switching transitions. This is because the commutation logic never switches any output from low to high or vice versa - there is always an off state in between. The inductance of the motor does force current transients when any transistor turns off, however. When a PNP turns off, residual current transfers to the internal diode at that output, pulling the output slightly below ground potential. When an NPN turns off, the transient current then flows through the PNP in the reverse direction, pulling the output voltage momentarily above the motor supply. Most PNP transistors will readily accept this as long as the voltages are low, but it should be evaluated for each application. Of course, the body diode of a P-channel FET provides this current path inherently.

Typical waveforms for voltage and current at one output are shown in Figure 7. While the voltage always switches to Vm on the high side due to the saturated PNP's, the value on the low side will be determined by the motor resistance and the commanded current. The large negative glitch occurs when the active PNP turns off; the tall spike above Vm occurs with turnoff of the NPN. The two short negative transients which occur while the current sinking NPN is on are caused by state-changes on the other two outputs momentarily interrupting current flow.

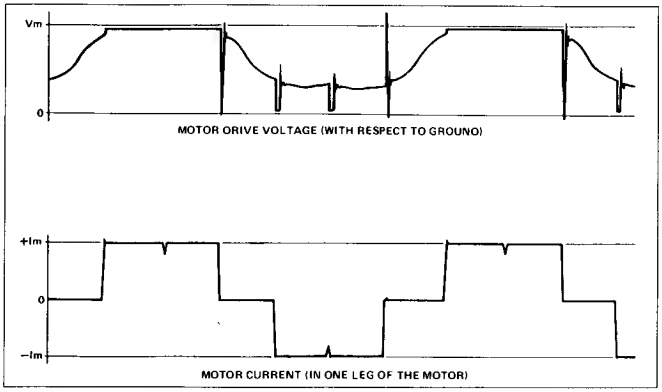

Figure 7: Voltage and current waveforms experienced at each output of the UC3655.

For disk drive or other applications where EMI noise generation at phase changes could be a problem, some slope control should be used on the outputs. While there are several ways to accomplish this, one effective technique is with R-C snubbers as shown in Figure 8. The circulating currents which will flow in these snubbers control the output rise and fall times and significantly reduce the higher frequency harmonics without contributing additional stress to the drive transistors.

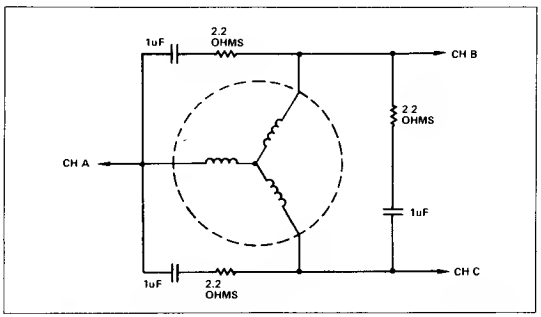

Figure 8: These three sets of R-C snubbers will help to reduce EMI noise.

ALTERNATE CONFIGURATIONS

Although the primary goal in developing the UC3655 was the implementation of a linear, current controlled BDC drive, that is not the only way this device may be used. The benefit of very low saturation voltage drop across the conducting switches has obvious advantages for efficient motor drive without linear control. The internal transconductance amplifier can be disabled by merely connecting the input terminal to the 5 V supply which will pull the compensation terminal up to the internal clamp level and allow the NPN low-side transistors to be switched fully on through the action of the decode logic. Current limiting may still be included by appropriate selection of the sense resistor, or for maximum voltage to the motor, the sense terminal may be connected directly to ground.

In this configuration, the circuit is only utilizing the position decode and output drive circuitry, and the motor will run open loop with its speed (or torque) determined solely by the motor voltage. This suggests another method of control. Since the UC3655 operates with only a 5 volt supply and is unaffected by the motor voltage, Vm, on the PNP emitters, controlling Vm will control motor speed. This can be done with either a linear or switch-mode regulator with the regulator control loop used to control the motor rather than hold the output voltage constant. An example of switching regulator control is shown in Figure 9 where an L296 PWM power supply IC is used as a 100kHz buck regulator. This circuit offers several advantages over other control techniques:

1. Since all power devices are used as switches, overall efficiency can be higher than with a linear approach.

2. The PWM frequency is converted back to DC before it gets to the motor minimizing the potential for harmful EMI.

3. High switching frequencies can be used in the regulator to keep the filter components small but with only ripple current through the motor, internal AC losses there are minimized.

4. A boost configuration could also be used to raise the motor voltage above the supply for faster response, lower currents, and a potentially significant increase in efficiency.

There are also some disadvantages:

1. The added complexity and components of the PWM regulator,

2. The additional switch in series with the motor.

PULSE WIDTH MODULATION OF MOTOR CURRENT

If the application will accept direct switch-mode control of motor current, this approach is also possible with the UC3655. Figure 10 shows the use of a UC3843 Power Supply PWM IC as the control element. Since this device has a very low impedance output drive, it will override the output of the UC3655's control amplifier and apply the PWM signal to whichever output has been activated by the decode logic. To keep switching and motor losses low, the frequency should be limited to the 20-40 kHz range.

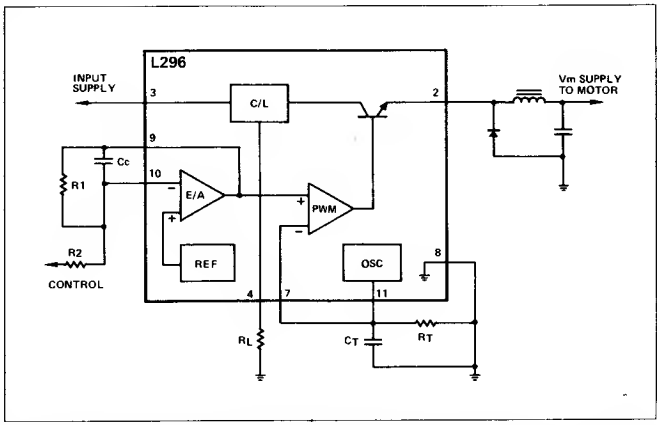

Figure 9: The L296 Buck Switching Regulator will efficiently control motor speed with the internal control loop disabled, by controlling the motor voltage instead.

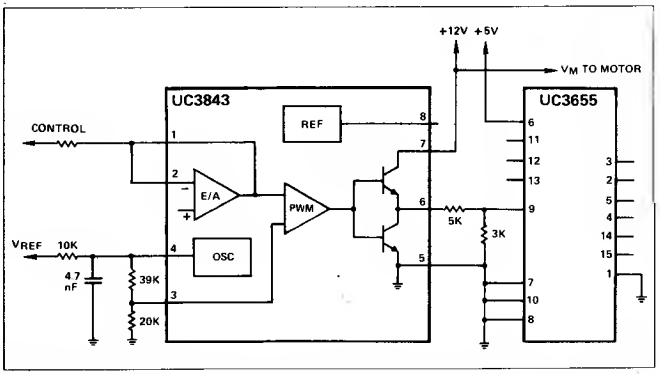

Figure 10: The UC3843 PWM Power Supply Chip can be used as a switch-mode controller for motor current by overriding the UC3655's internal amplifier with a PWM command.

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PHASE LOCK LOOP SPEED CONTROL

In many applications where very accurate speed control is required - disk drives, for example - a phase lock loop, locked to a crystal frequency reference, is often utilized. The UC3633 PLL chip has been designed to supply this capability and its use with the UC3655 is shown in Figure 11. In this circuit, a 4.9125 MHz crystal is divided down and compared with a signal from one of the motor's Hall sensors to force rotation at exactly 3600 rpm, +/- 60 ppm. This figure shows the UC3655 used in its conventional linear control mode, but the UC3633 is equally applicable to the other modes of operation discussed above. For further information on the UC3633, refer to Unitrode's Application Note U-113.

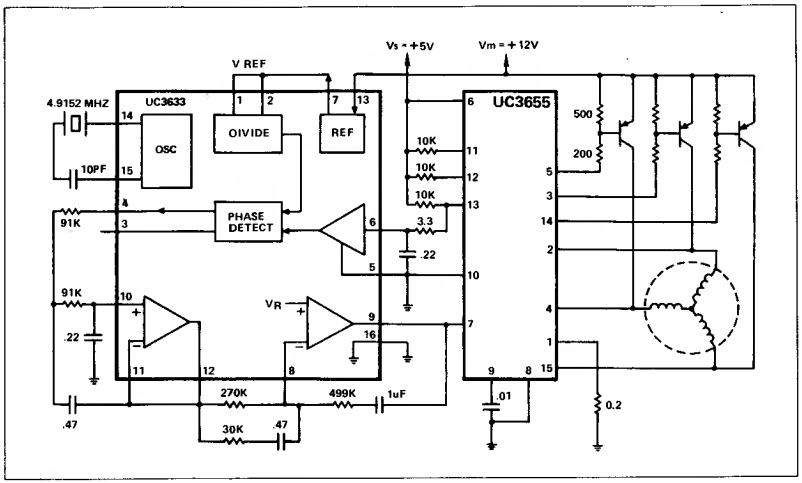

Figure 11: A UC3633 Phase Lock Loop IC can be used with the UC3655 to provide crystal-controlled speed accuracy.

SENSORLESS DRIVE

Finally, with the utilization of a microcontroller it should be possible to implement a drive system without the need for Hall position sensors and thus gain significant cost savings in the motor. Utilizing techniques developed for synchronous and stepper motors, commutation could be done "open loop" without angular position feedback but since the actual commutation point is not likely to occur at the optimum point, motor efficiency will be poor and will vary with load. One approach to solving this problem is the use of a single sensor to generate a reference point, and a digital PLL locked to this reference to generate the correct commutation timing. While this can yield commutation accuracy even higher than that obtainable with a typical sensor-type motor, the obvious disadvantage is increased cost over a completely sensorless design.

By using the back EMF generated by the motor, a signal proportional to the torque angle (commutation error angle) may be derived which can be used to correct the timing. However, simply forcing the commutation generator to deliver the correct timing will not control the speed of the motor. If instead, this signal is used to control the motor current by the approach shown in Figure 12, the commutation points are still generated open loop but, instead of forcing the commutation generator to follow the motor, the motor now follows the commutation generator. If the motor leads or lags, drive current is modified to force the torque angle to be optimum, yielding a PLL motor control system requiring no position sensors.

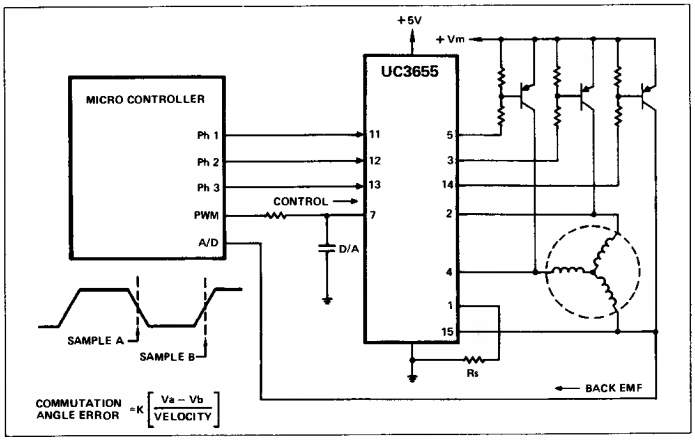

Figure 12: This approach to sensor-less control digitizes the back EMF on one motor phase and computes the commutation angle error from measurements made during the middle of the "off-time".

A NEW LINEAR REGULATOR FEATURES SWITCH MODE OVERCURRENT PROTECTION

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George Harlan, Power General

ABSTRACT

This paper presents a new linear regulator control circuit which, in addition to offering benefits such as low input-output differential and a precise reference voltage, features a unique and innovative approach to overload protection. By using duty-ratio, switch-mode protection, this circuit eliminates both the high internal dissipation of constant current limiting and the latch-up tendencies of limiting with current foldback.

THE CURRENT LIMIT PROBLEM

As an opening statement, let us offer as a "given" that all linear power supplies need some form of over-current protection. Traditionally, this protection consists of configuring the supply to control current - rather than output voltage - once an established threshold of maximum current has been exceeded. The method of current control can usually be classified as either "constant-current" or "current-foldback" current limiting and, while simple to classify, choosing between these two methods is often less than satisfying.

The protective method most acceptable to the user is constant current limiting with a characteristic as shown in Figure 1. With the knowledge that a power supply will only deliver a maximum current regardless of what he might do to it, the user's job of scaling his cables, switches, connectors, and other components associated with the power inputs to his system is greatly eased. He knows that no matter how non-linear his load may be, he can count on a regulated voltage whenever his current drain is within the supply's rating. Further, he knows that the maximum rated current is always available to meet any demand asked of the supply.

The "benefits" of constant current limiting are another matter to the power supply designer, however. For example, a regulator designed to deliver 12 Volts at a maximum load current of 5 Amps would probably start with a bulk input voltage of approximately 15 Volts and a constant current limit of 5.5 Amps. Under maximum rated load, the internal dissipation of the regulator is 3V x 5A or 15 watts but with a short to ground, this dissipation jumps to 15V x 5.5A or more than 80 Watts! This means that the thermal management and heat sinking must be sized for the short circuit condition resulting in a massive overkill in terms of volume, complexity, and cost with respect to normal operating conditions.

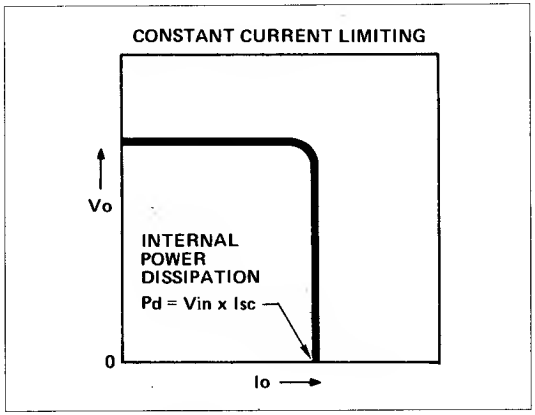

Figure 1: Constant current limiting.

A common solution to this problem is to design a current limiting scheme as illustrated in Figure 2. Here the protection is actuated at 5.5 Amps when the output voltage is at 12 Volts but the allowable current then "folds back" as the output voltage falls due to increasing overload, until it reaches some much lower value - say one Amp in this example - with a shorted output. Now the dissipation with a short circuit is close to the same as it was with rated current and our designer's thermal problems are solved.

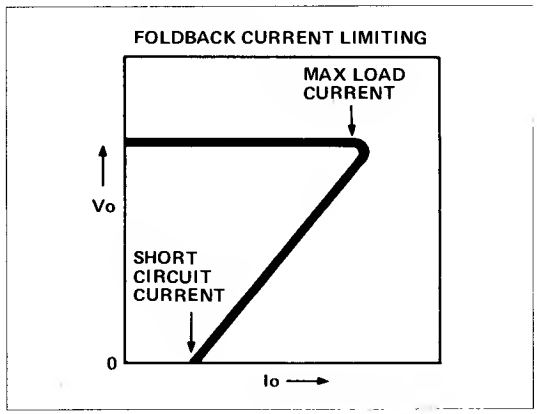

Figure 2: Foldback current limiting.

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But what about his customer? His load may be complex, non-linear, and often not even well understood. Figure 3 shows typical load characteristics for digital and analog circuitry but an actual system may include all of these plus motors which need to be started and capacitors which need to be charged. Any protection scheme which allows the static load line to intersect the foldback current curve as shown in Figure 4 is potentially subject to latch up because the load draws more current than the regulator can supply at the voltage where the curves cross.

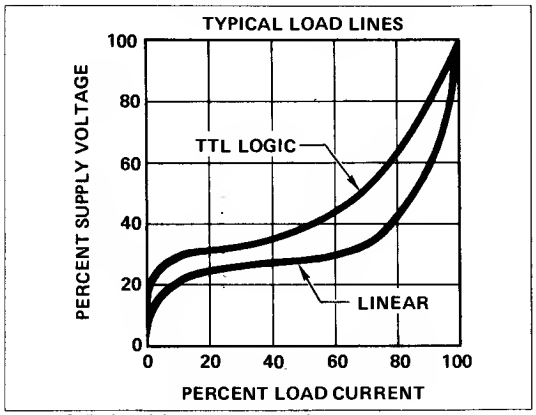

Figure 3: Typical digital and analog load lines.

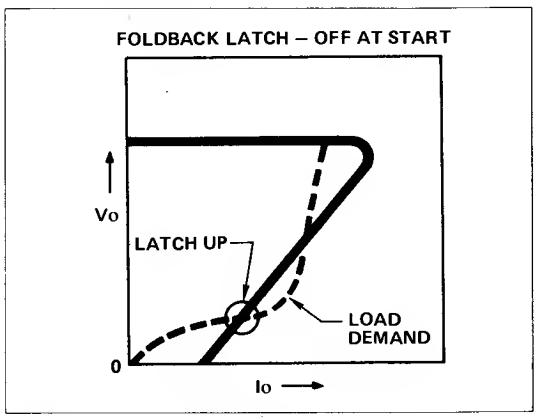

Figure 4: Latching at start-up with foldback.

An application particularly susceptible to latch up due to foldback current limiting occurs when two supplies are used to provide positive and negative voltages to a load where there is a path for "rail-to-rail" loading. As the regulators turn on, their output capacitors are charged at rates determined by the values of the capacitors and the amount of current each regulator can provide as its output rises up the foldback curve. Since these curves are unlikely to be perfectly matched, one output will dominate the other. As the faster one's output voltage increases, it provides more current through the common load. This forces the slower one back down the foldback curve where it provides less current, compounding the problem and ultimately latching when its output is driven past zero to a reversed polarity. Thus a foldback-limited regulator, which might be stable when used by itself, may latch when used as one-half of a dual-polarity system due to this "turn-on slew rate" phenomenon.

So what we have concluded is that while the power supply designer needs to incorporate foldback current limiting to reduce power dissipation, his customer needs constant-current limiting to insure reliable starting. It is the contention of this paper that what they both really need is duty-ratio protection.

DUTY-RATIO OVERCURRENT PROTECTION

Duty-ratio protection can be simply described as a constant current limiting regulator with a timer. The timer's function is to turn the regulator's power stage OFF and ON with an established duty cycle ratio such that the high internal power dissipation of constant current limiting is reduced by the duty ratio to a much more manageable average value.

Referring back to our earlier example of a 12V, 5A regulator, consider setting the constant current limit at 5.5 amps but additionally establish a duty ratio for the timer at 1 to 20 for "ON" to "OFF". If we set the "ON" time sufficiently long to charge whatever capacitance might be on the output, the regulator will power up with the constant current characteristic, insuring start-up regardless of the loading. In the event of an overload or short circuit (defined in this device as remaining in current limiting for a period of approximately 2 x Ton), the regulator will periodically shut down for a time equal to 20 x Ton and then continue to cycle in a 1 to 20 duty cycle until the fault is removed. Although the peak power during Ton might be 80 Watts, the average fault dissipation at this duty ratio is only 4 Watts - less than the normal 15 watt operating power loss, and we have thereby satisfied both the designer and his customer.

INTRODUCING THE UC1833 / UC3833

The block diagram of this new linear regulator control IC is shown in Figure 5. This circuit can be used in many different ways but its primary intent is as a high-efficiency regulator implemented with an external PNP pass transistor as shown in the figure. The circuitry in the right half of the UC1833 block generates the voltage error signal used to activate an NPN Darlington driver which, in turn, drives the base of the PNP pass device. This common-emitter pass transistor configuration allows this type of regulator to operate with a minimum input-output differential of well less than one Volt, even at high loads.

Duty-cycle current limiting is accomplished with the circuitry on the left half of the block diagram, where an Amplifier and a Comparator are seen, both monitoring the voltage drop across a single current sense resistor. The Comparator has an input threshold of 100 mV and, when activated, initiates a timer to alternately clamp and release the base of the driver to ground thereby switching the output of the regulator from Vout to Zero with a low duty ratio.

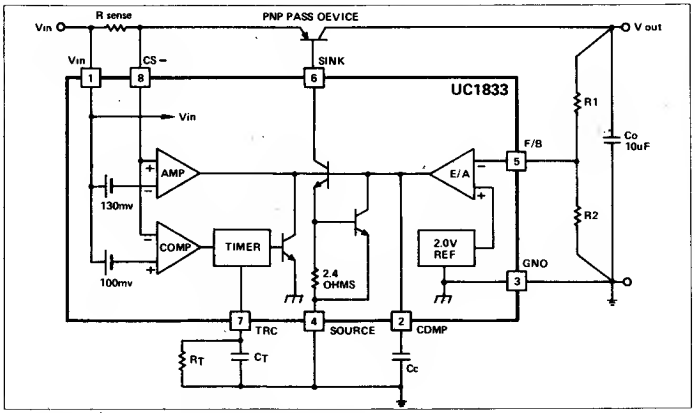

Figure 5: The new UC1833 / UC3833 linear regulator.

The Amplifier part of the current sense circuitry has an input threshold of 130 mV and overrides the output of the Error Amplifier to control the driver - when enabled by the ON-time of the timer - to regulate the supply's output current to a maximum amount determined by 130 mV divided by the value of the sense resistor. The 30 mV differential between the thresholds of the Amplifier and Comparator insures that current limiting can never occur without prior initiation of the timer.

OVERLOAD PROTECTION CIRCUITRY

The operation of the overload protection circuitry can be better understood by referring to the simplified schematic of Figure 6.

The current sensing portion of this circuit is to the left of this figure where the current-sense Comparator and Amplifier are shown sharing the same input sense pins. Note that their offset voltages are derived by a constant current through R1 and R2 in series rather than independently as shown in the more simplified earlier block diagram. By adding 30 mV to the 100 mV offset of the Comparator, the Amplifier's offset will more accurately track that of the Comparator should any variations occur, and the criteria to have the Comparator always activate first is assured.

A characteristic important to current protection is the accuracy of its threshold as any tolerance represents a window of undefined operation which works to the disadvantage of both designer and user of the power supply. Recognizing this, the UC1833's thresholds are derived from its precision reference resulting in a Timer activation threshold guaranteed to 5 percent over all operating conditions.

The output of the Current Amplifier connects into the output stage of the Error Amplifier where it can easily take command when activated. The compensation capacitor must compensate both the voltage and current feedback loops, and since the current loop must override the voltage control, its gain will be higher making the current loop the more difficult to stabilize. To evaluate the current loop, grounding the Timing pin will disable the Timer and allow continuous constant current operation. This can be useful either as a temporary measure while designing the current compensation network, or permanently to implement a constant-current limited power supply.

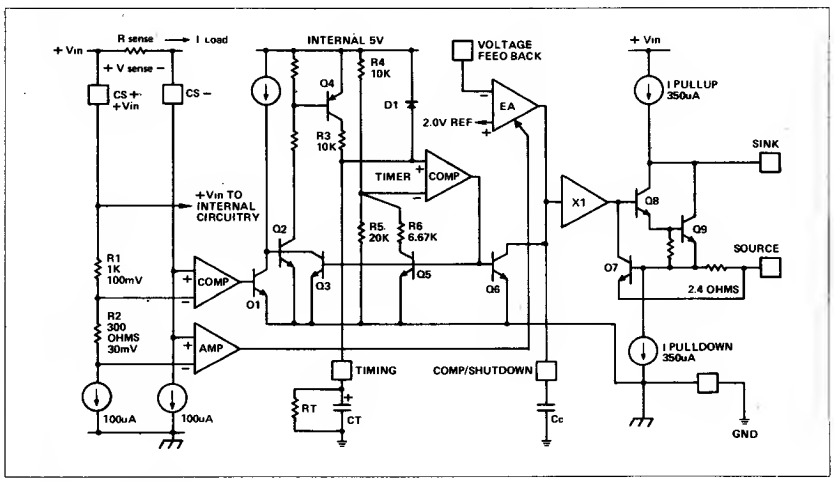

Figure 6: A simplified schematic of the UC1833 control circuitry.

The Current Sense Comparator is phased such that its activation turns off Q1 which turns on Q2 and Q4 to start the timing cycle. The timer is a gated astable relaxation oscillator with ON and OFF times independently programmed using an external resistor and capacitor, RT and CT. The external components work in conjunction with an internally switched 10k timing resistor shown in the schematic as R3. With RT much greater than 10k, the ON time is defined by R3 and CT, while RT and CT determine the OFF time. The thresholds for the Timing Comparator are set at 1/3 and 2/3 of the internally regulated 5 V source by the values of R4, R5, and R6.

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Timing waveforms during an overload cycle are shown in Figure 7 where the upper graph shows the output current from the regulator, the center one plots the voltage on the timing components, and the regulator's output voltage is shown in the lower graph. Following the sequence of events as drawn in the figure, when the load current ramps up and crosses the 100 mV Comparator threshold, the initial ON time begins. This initial period is about twice the duration of successive ON-times as the timing capacitor starts its charge from zero initially, while subsequent ramps begin from the lower Comparator threshold. While the timing capacitor is charging, the regulator current is limited by the action of the Current-sense Amplifier to maintain a level of 130 mV across the sense resistor. While in current limiting, the regulator's output voltage falls to whatever value that current will allow across the faulted load impedance.

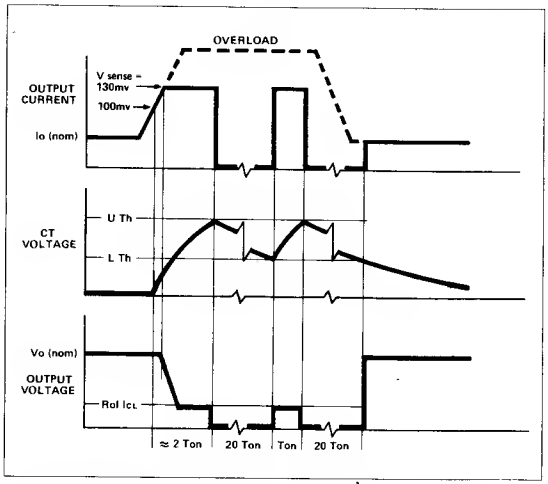

Figure 7: Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

The ON-time continues until the internal 10k resistor charges the timing capacitor to the upper Timer threshold. At this point, both the ON-time of the regulator and the charging of the timing capacitor are terminated, and the capacitor now discharges through RT, while the regulator is held OFF until the voltage on CT reaches the lower threshold, at which point the cycle repeats. If the load fault is removed during an ON-time, the Timer is immeadiatly disabled allowing the regulator to recover and the timing capacitor to discharge back to zero. If the fault is removed during an OFF-time, the Timer must complete that cycle of capacitor discharge before allowing the regulator to turn back on. In special applications requiring an extended ON-time, the correspondingly long recovery may be accelerated by interrupting the input voltage, as the falling internal 5 V source will discharge CT through D1 and an equivalent 1k impedance.

Duty-ratio protection has greatly eased the problem of heat sinking created with a constant-current solution since the area of the heat sink, or its thermal resistance, need only remove the average power as reduced by the duty ratio. Heat sinks for the internal power devices must now only have adequate thermal mass to absorb the high peak power of the initial ON period.

REMAINING CONTROL CIRCUITRY

Other blocks within the UC1833 include a 2.0 Volt band-gap reference internally trimmed to 1% and a low input-offset Operational Transconductance Amplifier (OTA) to serve as the error sensing and amplifying circuitry. The OTA Error Amplifier has a gm of about 4 millimho and an output current capability of +/- 300 uA. This form of amplifier can usually be compensated with a simple network - often a single capacitor - from its output to ground; but more commonly, an R-C pole-zero pair is also added to compensate for an external PNP pass transistor's gain characteristics.

The Error Amplifier is followed by a unity-gain Buffer Amplifier which controls the Driver Stage consisting of a Darlington transistor pair with local current limiting. This Driver can either source or sink current, allowing its use as a driver for either NPN or PNP pass transistors. The Pullup and Pulldown current-sources shown at the Sink and Source terminals of Figure 6 are to provide turn-off bias to the pass transistor during duty-ratio switching so that it is not turned off into a BV_{CEO} condition.

Not shown on the schematic are two additional forms of protection built into the UC1833: Thermal Shutdown (TSD), and Under Voltage Lockout (UVLO). While it could be argued that thermal protection on the control chip does nothing to protect the pass transistor, the fact that the Driver can conduct up to at least 100 mA with a large portion of the input supply voltage across it, can result in more than acceptable internal heating of the UC1833. A good practice, when voltage levels permit, is the addition of an external resistor in series with either the Source or Sink outputs of the Driver to remove some of the voltage - and therefore some of the dissipation - from the controller.

Under Voltage Lockout keeps the Error Amplifier output low until the supply voltage reaches approximately 4 Volts insuring that all internal circuits - particularly current limiting functions - are intelligent before allowing the pass transistor to turn on. The UVLO function also disables the Pullup current feeding into the Sink terminal, for low input voltages, so that the pass transistor cannot be driven in the reverse direction should the input supply fall with a charged capacitor or other energy source on the output. The Source Pulldown current source is also disabled with UVLO but this terminal also has a two-diode path from the Source to the Compensation terminals. This is to allow any shutdown function which pulls the Comp pin low to discharge capacitance at the regulator's output without reverse-biasing the Driver's emitter-base junction.

THE UCI832 I4-PIN CONTROLLER

An important objective in the design of the UC1833 was that in addition to providing significant operating benefits over the omnipresent uA723, the resulting product should be cost-competitive with that device. Committing the UC1833 to an 8-pin

Minidip package allows the potential for meeting the cost objective (plus the benefit of less PC board area), but in several important ways, also restricts the device's versatility. Recognizing this fact led to the introduction of the same chip in a 14-pin package with a UC1832 designation. The block diagram of this device, in a uA723-type application, is shown in Figure 8.

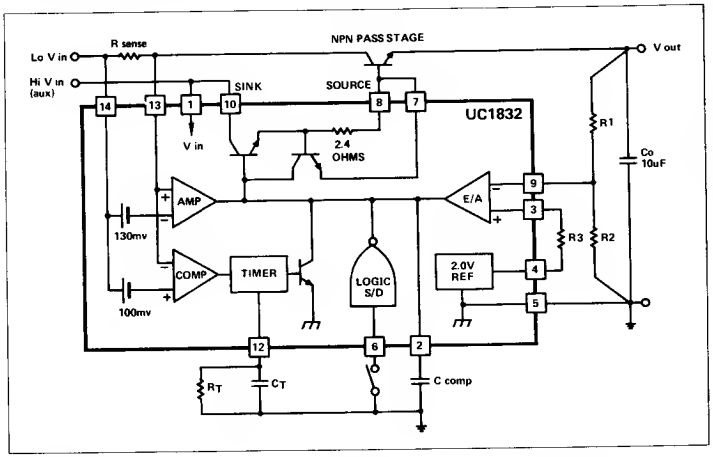

Figure 8: A 14-pin version, designated UC1832 / UC3832, offers enhanced versatility.

The characteristics of the UC1832 include all the performance features of the UC1833 plus the following:

1. Separating thc +Vin line from the CS+ terminal so that the controller could be supplied from a higher potential, low-current, auxiliary voltage while sensing current from the main supply.

2. Separating the Reference from the Error Amplifier (+) input and making both accessible to the user. Among other things, this allows phase reversal, an external or divided-down reference, and a convenient access point for soft-start.

3. Providing a separate input to the Driver's local current limiter allows considerable flexibility in setting that limit either higher or lower than the 300 mA (typical) defined by the internal 2.4 ohm resistor.

4. A separate logic-level digital shutdown function has been added to give more programming options such as accepting a shutdown command from an over-voltage sensor or implementing a turn-on delay. This input is fail-safe as it must be pulled low to allow the regulator to turn on.

TYPICAL CIRCUIT APPLICATIONS

Unitrode's Power General Division has already utilized the UC3833 (the commercial version of the UC1833) in several successful power supply designs. A brief description of some of these products will illustrate both the range of applications and the simplicity which this new device brings to power supply design.

The circuit of Figure 9 shows one of the simplest applications of the UC3833 repeated twice to implement a dual-polarity 12 volt, 200 mA supply. The timing components for duty-ratio protection are determined from the following equations:

$$Ton = .69 \times 10k \times CT$$

$$Toff = .69 \times RT \times CT$$

$$\text{Duty-ratio} = Ton/(Ton+Toff)$$
$$= 10k/(10k + RT)$$

The values shown provide approximately 7 mS ON time and 140 mS OFF. These fairly rapid time constants minimize the need for any significant thermal mass in the heat sinks and also allow fast recovery after an overload is removed. With the knowledge that the initial conducting time can be twice the ON time, the maximum output capacitance can be calculated from:

$$C = Imax\ (dt/dV)$$

$$C = 130mV/.5ohm\ (\ 14mS/12V\ ) = 300\ uF.$$

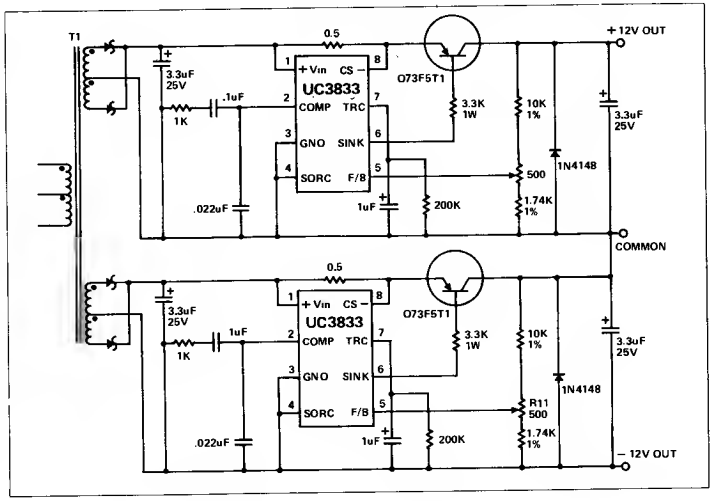

Figure 9: A +/-12V, 200mA regulator is easily implemented with two UC3833 devices.

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A higher power application is shown in the schematic of Figure 10 which was designed to supply 5 Volts at 5 Amps. The UC3833, configured as shown, will meet this requirement with an input voltage as low as 6 Volts due to the low saturation voltage of the paralleled 2N6489 transistors and the fact that the maximum non-fault voltage on the sense resistor is less than 100 mV. Actually, a little more sense voltage was sacrificed in the interests of selecting a standard resistor value, with the excess divided down by the 56/100 ohm divider. The additional BD438 drive transistor was added to boost the UC3833 drive current and keep the internal power dissipation low.

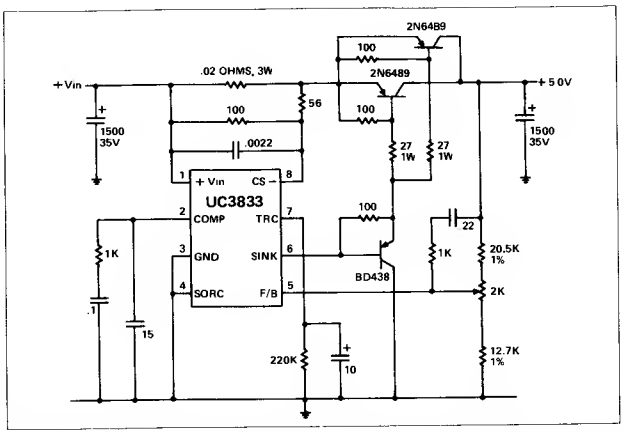


Figure 10: A high-efficiency configuration with added current boost will deliver 5V at 5A from a 6V source.

A third application of the UC3833 is one which took particular benefit from duty-cycle current limiting. This was for a disk drive power supply which required considerable current at turn-on to accelerate the disk. The circuit schematic is the same as that shown in Figure 10 with the voltage sense resistors selected for a 12 Volt output. The power requirements dictated a peak start current of 5 Amps decaying to 3 Amps in 30 seconds as the motor reached operating velocity. The current sense resistor was chosen to give a Timer initiation at 4.75 A and a constant current limit of 6.1 Amps. The timing capacitor value was set at 3300 uF yielding an ON-time of approximately 20 seconds, with 40 seconds for the initial turn on period - during which time the motor current will decrease to less than the lower threshold. With a duty-ratio of 20:1, when a fault does occur, the OFF-time will now be greater than 6 minutes, but, if this is excessive, recycling the input voltage to the regulator will reset the timing capacitor.

CONCLUSION

While no one can deny the long-term success of the uA723 as a general-purpose linear regulator controller, there has also long been a call for a device to improve its many limitations. While other products have been marketed offering some parametric improvements, the UC1833 - and its companion UC1832 - are the first to offer an innovative solution to a very basic problem. By combining switch-mode protection with linear regulation, these devices answer the question of which form of protection is best for whom, with a solution that is best for everyone.

A SIMPLIFIED APPROACH TO DC MOTOR MODELING FOR DYNAMIC STABILITY ANALYSIS.

By
Claudio de Sa e Silva
Applications Engineer
Unitrode Corporation

When we say that an electric motor is a device that transforms electric power into mechanical power, we say two things. First, that the motor is — and behaves as — a transformer. Second, that it stands at the dividing line between electrical and mechanical phenomena. In the case of permanent magnet (PM) motors we know that this power transformation works in both directions so that the electrical impedance depends on the mechanical load, while the mechanical behavior of the motor depends on the conditions at the electrical end.

This being the case, it should be possible to represent a motor's mechanical load, on the electrical side, by a set of familiar electrical components such as capacitors or resistors.

CHOOSING A UNIT SYSTEM

Before we get started, let us consider for a moment the system of measurement units that we have chosen.

The metric system of units has undergone a number of changes in its history, of which the latest is the SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is a coherent system, in which the product or quotient of two or more units is the unit of the resulting quantity. It will be seen here that certain simplifications result from using this form of the metric system.

In the SI system, force is measured in Newtons (N) and distance in meters (m). Consequently, the units of torque are Nm (see Conversion Table). If a motor shaft rotates at an angular velocity of ω_M radians per second, with torque T_M, the mechanical power output will be equal to the product T_M and ω_M and the units will be watts if T_M is in Nm.

Motor manufacturers usually specify a torque constant (K_T) and a voltage constant (K_V) for their motors. These constants have different values when the torque and speed are measured in English units, but they have the same numerical value when SI units are used. This becomes obvious when you consider that the electrical input power must be equal to the mechanical output power:

(1) $V_A I_A = T_M \omega_M$ (watts)

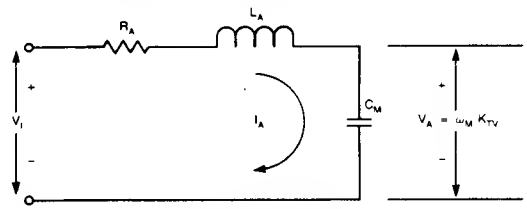
(2) $\frac{V_A}{\omega_M} = \frac{T_M}{I_A} = K_{TV}$

*where V_A is the internally generated armature voltage, or back emf, and I_A is the armature current. (See Fig. 1 for definition of motor terms.)

TABLE 1. UNITS CONVERSION

THESE UNITS	{ × → = / = ← ÷ }	SI UNITS	DIM.
oz	2.78×10^{-1}	N	MLT^{-2}
lb	4.448	N	MLT^{-2}
in	2.54×10^{-2}	m	L
ft	3.048×10^{-1}	m	L
gf	9.807×10^{-3}	N	MLT^{-2}
g cm^2	10^{-7}	Nm sec^2	ML^2
ft lb sec^2	1.356	Nm sec^2	ML^2
oz in sec^2	7.063×10^{-3}	Nm sec^2	ML^2
ft lb	1.356	Nm	ML^2T^{-2}
oz in	7.063×10^{-3}	Nm	ML^2T^{-2}

NOTE The dimensions are M (mass), L (length), and T (time). The gram (g) is a unit of mass, and the gram-force (gf) is a unit of force. The pound (lb) and the ounce (oz) are included as units of force only.



ω_M = motor speed in rad/sec
K_{TV} in Nm/A or Vsec/rad
$C_M = \frac{J}{K^2_{TV}}$ (farads)

FIGURE 1. THIS SERIES RLC CIRCUIT IS AN EXCELLENT MODEL OF A DC MOTOR LOADED WITH AN ESSENTIALLY INERTIAL LOAD. HERE, J IS THE TOTAL MOMENT OF INERTIA, INCLUDING THE ROTOR'S J_M.

If we do the same thing with the familiar electrical transformer, we get the turns ratio:

(3) $V_1 I_1 = V_2 I_2$ (watts)

(4) $\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{N_1}{N_2}$

Thus, the non-dimensional turns ratio N_1/N_2 is analogous to the dimensional torque (or voltage) constant K_{TV}. Furthermore, equations (2) and (4) give us a clear hint that the angular velocity (ω_M) is analogous to voltage, while the torque (T_M) is analogous to current.

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The units of K_{TV} may be either Nm/A, or V sec/rad. Thus, specifying both K_T and K_V for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer, and can only make sense where redundancy is required.

THE MOTOR AS A TRANSFORMER

We have established an analogy between K_{TV} and a transformer's turns ratio; between angular velocity and voltage; and between torque and current. If the motor behaves as a transformer, then we would expect to find the square of K_{TV} involved in something analogous to impedance transformation.

Suppose we apply a constant current I_A to the armature of a motor whose load is its own moment of inertia J_M (Nm sec^2). We know that according to Newton's law for rotating objects,

(5) $T_M = J_M \alpha_M$

where α_M is the angular acceleration $d\omega_M/dt$.

Since $T_M = I_A K_{TV}$ (Eq. 2)

(6) $$I_A K_{TV} = J_M \frac{d\omega_M}{dt}$$

Furthermore, also from Eq. 2,

(7) $$\omega_M = \frac{V_A}{K_{TV}}$$

so that

(8) $$I_A = \frac{J_M}{K_{TV}^2} \cdot \frac{dV_A}{dt}$$

Equation 6 has a familiar form, and we recognize at once the quantity J_M/K_{TV}^2 as a capacitor. It follows that the motor "reflects" a moment of inertia J_M back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

A neat way to check this result is to equate the energy stored kinetically in J_M with the electrical energy stored in a capacitor C_M:

(9) $\frac{1}{2} C_M V_A^2 = \frac{1}{2} J_M \omega_M^2$

(10) $$C_M = J_M \left(\frac{\omega_M}{V_A}\right)^2$$

Since $\frac{\omega_M}{V_A} = \frac{1}{K_{TV}}$,

(11) $$C_M = \frac{J_M}{K_{TV}^2} \text{ (farads)}$$

Similarly, a torsional spring with spring constant K_S (Nm/rad) is reflected as an inductance of K_{TV}^2/K_S henries. And a viscous damping component B (Nm sec/rad) appears as a resistor of K_{TV}^2/B ohms.

A MOTOR MODEL

Once we can represent the mechanical load by means of electric elements, we can draw an equivalent circuit of the motor and its mechanical load. The armature has a finite resistance R_A and an inductance L_A, through which the torque-generating current I_A must flow. These components are not negligible, and must be included. An inertially loaded motor can be represented as in Fig. 1, where the moment of inertia J is the sum of the load's J_L and the rotor's J_M.

It turns out that in practice, the moment of inertia that the motor must work against — or with, depending on how you look at it — is by far the most important component of the mechanical load. A frictional component also exists, to be sure, but because it is largely independent of speed, it would be represented electrically as a constant current source, which could not affect the dynamic behavior of the motor. And since a torsional spring — which would affect it — is rarely found in practice, we will concentrate on the inertial problem only.

MEASURING THE COMPONENTS

The measurement of R_A and L_A is not difficult. A good ohmmeter will get you R_A, and you can measure the electrical time constant τ_E to calculate L_A:

(12) $L_A = \tau_E R_A$

Just make sure that the rotor remains stationary during these measurements.

In order to determine the value of the capacitor, C_M, we will need to measure the shaft speed. If the motor being measured is a brushless DC motor, we can use the signal from one of the Hall effect devices as a tachometer. If the Hall frequency is f_H, and the number of rotor poles is P, the angular velocity ω_M is

(13) $$\omega_M = \frac{4\pi f_H}{P} \text{ (rad/sec)}$$

With other motors you will need a strobe-light or some other means to measure speed.

A good way to measure C_M is through a measurement of the mechanical time constant T_M. We do this by driving the motor with a constant voltage driver and measuring the time it takes to accelerate from zero speed to 63% of the highest speed achievable at the voltage used. To set a safe limit to the starting current we can reduce the supply voltage or add a series resistor with the motor, or both. The set-up is shown in Fig. 2. Note that the armature resistance R_A is already known, and we add resistors R_B, if needed, to limit the armature current I_A to a value that is safe for both driver and motor.

The first thing to do is let the motor run freely and measure ω_{MAX} and I_{MAX}, and use these values to calculate the armature voltage V_{MAX}:

(14) $V_{MAX} = V_{CC} - V_{SAT} - I_{MAX} (R_A + R_B)$

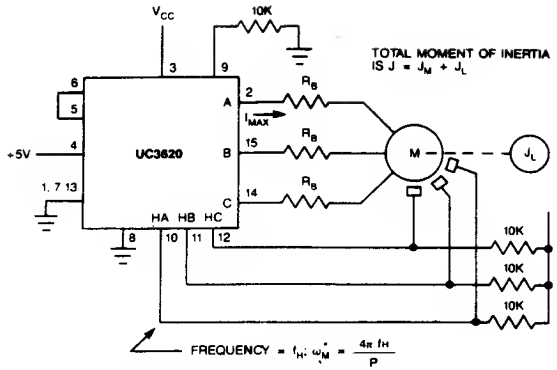

FIGURE 2. SET-UP FOR MEASUREMENT OF C_M = J/K_{TV} OF A 3-PHASE BRUSHLESS DC MOTOR WITH INERTIAL LOAD J1. THE MOTOR VOLTAGE $V_M = V_{CC} - V_{SAT}$, WHERE V_{SAT} IS THE OUTPUT SATURATION VOLTAGE.

Here V_{CC} is the supply voltage, V_{SAT} is the saturation voltage of the driving circuit, and I_{MAX} is the current drawn by the unloaded motor at maximum speed.

Thus we can calculate

$$(15)\quad K_{TV} = \frac{V_{MAX}}{\omega_{MAX}} \quad \text{(Vsec/rad)}$$

Next, set the oscilloscope time scale to that you can easily read a Hall frequency equal to 63% of ω_{MAX}, so that:

$$(16)\quad \omega_M = 0.63\ \omega_{MAX}$$

By holding and releasing the motor shaft, take several readings of the time T_M required to accelerate from zero to ω_M. Remember that these readings are taken "on the fly," since the motor continues to accelerate towards the maximum speed ω_{MAX}. Having obtained a good value of T_M you can now calculate

$$(17)\quad C_M = \frac{T_M}{(R_A + R_B)} \quad \text{(farads)}$$

This completes the RLC equivalent circuit, If the value of J_M is also required, it too can be calculated:

$$(18)\quad J_M = C_M K_{TV}^2$$

THE MOTOR'S TRANSFER-FUNCTION

In the circuit of Fig. 1, V_1 is the voltage applied to the motor leads, and V_A is the actual armature voltage, or back EMF. This latter voltage is equal to $\omega_M K_{TV}$, as we have seen, so that if we want to derive an expression relating the speed to the applied voltage, we can write:

$$(19)\quad \frac{\omega_M}{V_1} = \frac{1}{K_{TV}} \cdot \frac{V_A}{V_1} \quad \text{(rad/Vsec)}$$

If V_1 is a constant voltage, the speed ω_M will also be constant. This is clear from the circuit of Fig. 1 as well as from our experience with motors. If, however, V_1 varies sinusoidaly at some frequency f, the speed ω_M will vary similarly, but the amplitude and phase will in general be different from those of the driving function. This fact is very important if we are to include the motor in a feedback loop, because the motor's contribution to the overall loop gain and phase shift is an important factor in determining stability. The motor's transfer function — i.e. Eq. 19 expressed as a function of frequency — gives us a precise description of how the amplitude and phase behave at different frequencies. To do this, we use the variable $j\omega$, where $j = \sqrt{-1}$, and $\omega = 2\pi f$.

$$(20)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{(j\omega C_m)^{-1}}{j\omega^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(21)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{(j\omega)^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(22)\quad L_A C_M = \frac{1}{\omega_n^2}$$

where ω_n is the natural frequency of the circuit.

$$(23)\quad R_A C_M = \frac{R_A C_M L_A}{L_A} = \frac{R_A}{\omega_n^2 L_A} = \frac{1}{Q\omega_n}$$

since the circuit Q is

$$Q = \frac{\omega_n L_A}{R_A}.$$

Therefore,

$$(24)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Furthermore, using Eq. 19,

$$(25)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} = \left(\frac{1}{K_{TV}}\right) \cdot \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Since we know the values of K_{TV}, ω_n and Q, we can calculate the magnitude and phase angle of Eq. 25 for various values of $j\omega$. For a given $\omega = \omega_1$, Eq. 25 can be evaluated into a complex number $A_1 + jB_1$, whose angle is,

$$(26)\quad \theta_1 = \tan^{-1}\frac{B_1}{A_1}$$

and whose magnitude can be expressed in decibels as follows:

$$(27)\quad M_1 = 20 \log_{10} \sqrt{A_1^2 + B_1^2}$$

A plot of these quantities, using a logarithmic frequency scale, is called a Bode plot, and can be a handy tool in understanding how the device will affect the final loop performance.

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A DISC - DRIVE EXAMPLE

A small three phase brushless DC motor, measured as above, has the following characteristics:

K_{TV} = 0.015 Nm/A, or Vsec/rad.
R_A = 2.5 ohm
L_A = 0.002 Hy
J = 0.001 Nm sec_2

The J value was measured with three magnetic discs mounted, and represents the actual value required for the application. Using Eq. 11.

$$(28)\quad C_M = \frac{J}{K_{TV}^2} = \frac{001}{(0.015)^2} = 4.44 \text{ fd}$$

This may seem like an unusually large value for a capacitor, but it simply reflects the large amounts of kinetic energy that can be stored in the included inertia.

From Eq. 22

$$(29)\quad \omega_n = \frac{1}{\sqrt{L_A C_M}} = \frac{1}{\sqrt{0.002 \times 4.44}}$$

$$= 10.61 \text{ rad/sec}$$

From Eq. 23

$$(30)\quad Q = \frac{\omega_n L_A}{R_A} = \frac{10.61 \times 0.002}{2.5} = 0.0085$$

(The quality factor Q has no units). The motor transfer function, given in Eq. 25, is

$$(31)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} =$$

$$= \frac{66.67}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1} \text{ (rad/Vsec)}$$

A calculator that is pre-programed to operate with complex numbers (HP 28C, for example, or 15C) makes the evaluation, of this equation an easy task. With the 28C you can set up a USER routine called BODE, as follows:

<<DEG DUP ABS LOG 20 X SWAP ARG>>

This will convert a complex number x + jy into 20 log $\sqrt{x^2+y^2}$ at level 2, and arc tan (y/x) at level 1. Table 2 shows a list of several such computations of Eq. 31:

At ω = 0, the gain is simply 66.67 rad/Vsec. As ω increases from zero up, the gain decreases as shown in the GAIN column of Table 2. For our Bode plot, we want to show the gain relative to the initial, or DC, gain. Therefore, we subtract 66.67db from each gain value in Table 2 and plot the result. This is the same as plotting only the function

$$(32)\quad G(j\omega) = \frac{1}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1}$$

which should be compared with Eq. 31. The results are shown in Fig. 3.

TABLE 2. CALCULATED VALUES OF EQUATION 31.

ω (rad/sec)	$\frac{\omega_M(j\omega)}{V_1(j\omega)}$	GAIN (db)	PHASE (deg)
0.01	65.9 − j 7.32	36.4	−6.3
0.03	60 − j 20	36.0	−18.4
0.1	29.8 − j 33.2	33.0	−48.0
0.3	5.5 − j 18.4	25.7	−73.3
1.0	0.53 − j 5.95	15.5	−84.9
3.0	0.06 − j 2.00	6.0	−88.4
10.0	0 − j 0.60	−4.4	−89.9
30.0	-4.2×10^{-3} − j 0.20	−14.0	−91.2
100	-4.7×10^{-3} − j 0.06	−24.5	−94.5
300	-4.5×10^{-3} − j 0.02	−34.2	−103.5
1000	$-2.9 \times 10^{-3} - j\, 3.7 \times 10^{-3}$	−46.6	−128.6
3000	$-7.1 \times 10^{-3} - j\, 3 \times 10^{-4}$	−62.3	−157.4

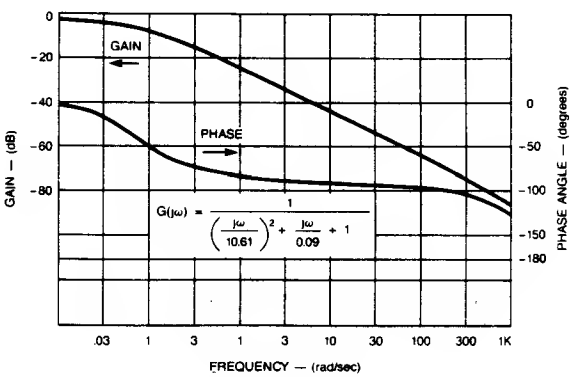

FIGURE 3. BODE PLOT OF MOTOR DATA IN EXAMPLE.

Note that up to about 100 rad/sec (15.9 Hz) the phase lag barely exceeds 90 degrees. The first pole occurs at ω = 0.09 rad/sec, at which point the phase lag is 45 degrees. The second pole, widely separated from the first in this case, occurs at a frequency in excess of 1000 rad/sec, as we can see from the further bend in the phase curve. The gain, which was drooping at a rate of −20db per decade below 100 rad/sec, now begins to bend towards a steeper droop of 40db/dec after the second pole is reached. At very high frequencies, the phase lag will reach 180 degrees.

Used in a speed control feedback loop, this motor will perform well provided that the user takes this gain and phase behavior into account. This is done by incorporating the motor transfer function into the overall loop equation, which will include other components. One's understanding of the motor's behavior improves with this type of analysis, which makes comparisons between different motors more clear and articulate.

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1 MHz 150W RESONANT CONVERTER DESIGN REVIEW

Bill Andreycak

Abstract:

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms and transferred charge and energy will be analyzed as functions of time and input/output conditions. Specific and generalized design equations are given, which are also applicable to other topologies by those skilled in modern power supply design.

Introduction:

The pioneers of resonant mode power conversion have generated a tremendous amount of interest in this new and emerging technology and approach to power conversion. Expectations of lossless switching and multi-megahertz operation are rapidly approaching realization. Given this recent stimulus, a new control IC, the UC3860, has been introduced for controlling many of the various resonant and quasi-resonant design approaches.

Despite the differences among the numerous and quasi-resonant switching topologies, all have one common denominator--the need for a high speed, complete and versatile resonant mode control IC. The ideal candidate would incorporate modulator functions or building blocks that could be easily configured by the user to control various circuit topologies and implementations.

This paper will show one application of this resonant control IC in a typical power supply design example. Described in the text is a 150 watt off-line converter switching at a maximum frequency of 1 megaHertz. This results in an effective 500 kiloHertz utilization of the main transformer. Delivering 15 volts at 10 amperes, of load current, it operates from a 110/220 AC input or from a 220 to 370 V dc bus at high efficiency.

Design Specifications:

An off-line 150 watt, single output design has been selected as a typical application for the purposes of this paper. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations. However, this discussion will concentrate on relevant calculations and new material regarding tthe quasi-resonant converter.

Input Voltage:

($110\ V_{AC}$) : 85 — 132 V_{AC}

($220\ V_{AC}$) : 170 — 265 V_{AC}

(DC Input) : 220 — 375 V_{DC}

AC Line Frequency : 50 Hz min

Output Voltage: 15 V_{DC}

Output Current: 2.5 — 10 Amps

Line Regulation: 16 mV

Load Regulation: 15 mV

Output Ripple: 100 mV p-p, dc-20 MHz
Efficiency: 85 % at full load

Quasi-resonant Circuit Operation

The quasi-resonant Buck regulator circuit shown in Fig. 1 is applicable to high frequency power conversion systems and will be dsescribed in detail. Initial conditions are given with the switch Q open, and no current flowing from the input source *V*. The resonant current I_r is zero and no voltage is acrosss either of the resonant components L_r or C_r. There is an output current I_{out} and voltage V_{out} delivered entirely by the output filter components L_o, C_o and D_o. For the purposes of this model, assume that each component is ideal.

Switch Q is closed at time t_o applying voltage V_{IN} across the circuit input. The input current I_{in} begins at zero and rises linearly at the rate of V_{IN}/L_r until it reaches output current I_{out}.

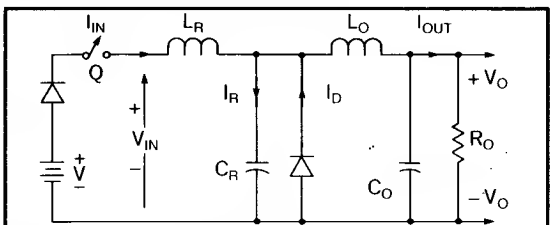

Figure 1 - Quasi-Resonant Buck Regulator

Simultaneously, the output diode current I_d which began at I_{out} linearly decreases to zero. At this point, the input power source is supplying the full output current I_{out}. This occurs at tiime t_1 which will vary linearly with I_{out} and V_{IN}. During the interval between t_o and t_1, no resonant current I_r flows in capacitor C_r.

Beginning at t_1 the resonant circuit current component I_r sinusoidally flows through C_r. This adds to the output current, making the input current the summation of both. Peak input current occurs at $t_1+\pi/(2\omega)$. It later intersects the I_{out} level at t_2, corresponding to $t_1+\pi/\omega$

The sinusoidal input current continues until t_3 where it reaches zero. Here, the switch is opened and turn-off is initiated at *zero current* which facilitates lossless switching. Since t_1 varies with I_{out} and V_{IN}, the zero current switch point t_3 varies also with these changing parameters.

A zero current detection circuit can be used to facilitate turn-off at precisely zero current. Another technique utilizes a fixed *on* time at the primary switches. This time constant is set above the maximum required *on* time of the resonant network over all line and load combinations. While this technique is easier to implement, it may compromise overall design at the maximum conversion frequency. The inability to switch consecutively at maximum rate hurts transformer turns ratio optimization. Higher currents will result due to the lower turns ratio, degrading overall efficiency at all frequencies.

During the interval between t_3 and t_4, C_r discharges, providing a constant current I_{out} to the load. The capacitor voltage decreases linearly, reaching zero at t_4.

The output filter section releases its stored energy between t_4 and t_5. The conversion period ends at t_5, which corresponds to the beginning of the next cycle, t_o. A detailed analysis of the voltages and currents during each interval is provided in the Appendix.

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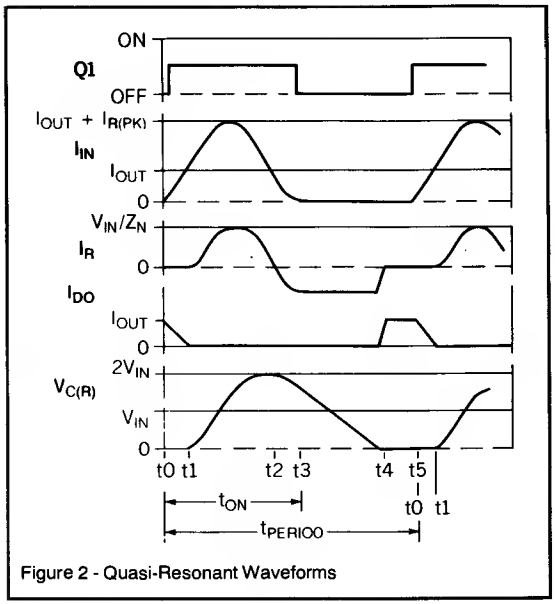

Figure 2 - Quasi-Resonant Waveforms

Quasi-Resonant Half-Bridge— Topology Fundamentals and Overview

The general circuit diagram for a quasi-resonant half bridge converter using secondary side resonance is shown in Fig. 3. The resonant half bridge portion and its associated waveforms are shown in Figs. 4 and 5.

Transistors Q_1 and Q_2 are alternately driven from the control circuitry at a repetition rate, or frequency determined by the error voltage.

Q_1 turns on, connecting the transformer primary across capacitor C_1 with voltage $V_{IN}/2$. This rectangular voltage waveform is divided by the turns ratio N (N_{pri}/N_{sec}) and coupled to the secondary side(s) of the transformer. Diode D_1 is forward biased and secondary current I_{sec} flows through L_{r1} and D_1. This can be expressed as two individual components, the "constant" output current I_{out} and the sinusoidal current I_r through C_r. During this interval, D_2 is reversed biased and is essentially out of the picture.

The secondary current starts at zero at time t_o and ramps up linearly, reaching I_{out} at t_1. I_{sec} then becomes sinusoidal, peaks at $I_{sec(peak)}$, and intersects the output current again at t_2. At t_3, zero current is reached sinusoidally and Q_1 is turned off.

Peak voltage across C_r occurs at t_2 and diminishes during the remainder of the interval ending at t_5. When the voltage across C_r reaches zero, all of its stored charge has been transferred to the output load, thus completing the conversion cycle. This process is repeated for transistor Q_2, resulting in similar operation.

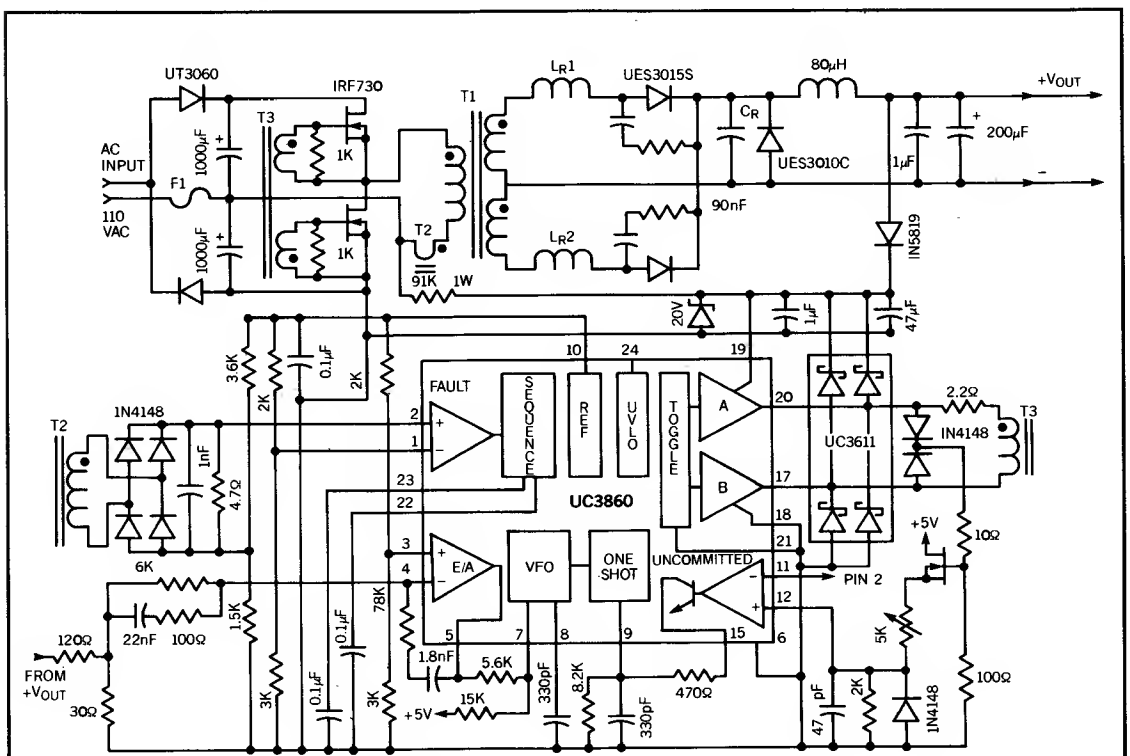

Figure 3 - 150 Watt Off-Line Quasi-Resonant Half Bridge

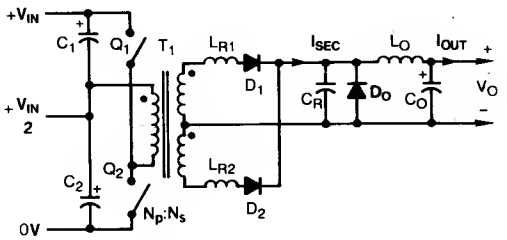

Figure 4 - Quasi-Resonant Half Bridge

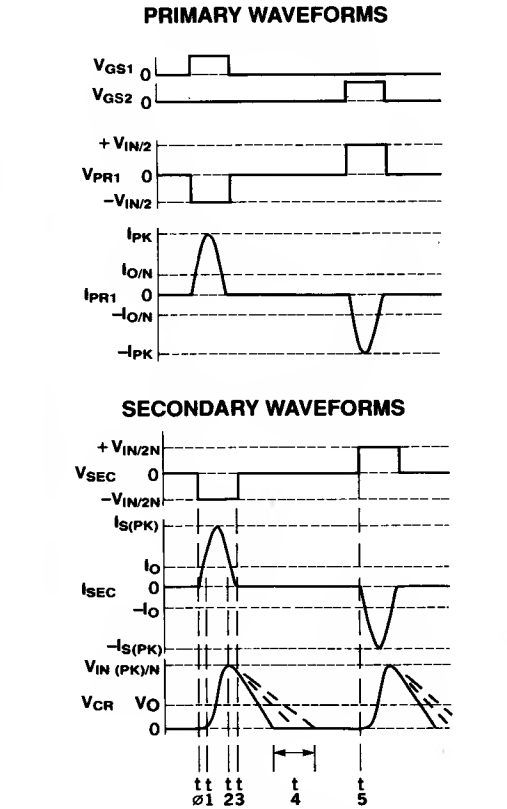

Figure 5 - Primary and Secondary Waveforms

Half Bridge Advantages and Alternatives

The thrust towards resonant mode power supply designs has been fueled by the demands for higher power densities and high overall efficiency. Although several basic topologies deserve consideration in this off-line application, the Half Bridge configuration offers many key advantages.

Unlike the single-ended forward converters, the half bridge provides bidirectional utilization of the tranformer. This eliminates the need to incorporate dissipative or complex flux reset mechanisms for the main transformer. Also, the primary switched voltage is one-half that of its single ended or full-bridge counterpart, halving the transistor voltage rating requirements.

In addition, the reduced voltage significantly reduces turn-on losses. Bear in mind that zero current switches minimizes *only* the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge has the lowest turn-off losses of all configurations.

Transformer size is smaller for the half bridge because the forward converter "wastes" half the period with no power transfer while the core is being reset. Also, all windings have half the number of turns compared to a forward converter approach. This could significantly lower the leakage inductance in certain designs where the low voltage, high current designs stand to benefit the most.

Half Wave Resonance: The half-wave resonant mode of operation facilitates a unidirectional current flow from the primary to the secondary. The major advantages of this can be seen near the primary switches. When a reverse current flows through the Mosfet, its parasitic drain-body diode conducts, exhibiting slow reverse recovery characteristics. To prevent this, the reverse current is generally directed to an external fast recovery diode that shunts the Mosfet. A Schottky diode must be added in series with the Mosfet to guarante that the external diode will conduct. This "elaborate" network is not lossless, and can signifcantly impact the power supply overall efficiency.

Seconday side half wave resonance eliminates the need for these components. Reverse current flow is restricted on the secondary side of the tansformer by the series rectifiers. Serving a dual purpose, these diodes isolate the resonant tank from the primary in addition to rectifying the secondary waveform.

Full wave designs return excess thank energy back to the primary, and require bidirectional switches on the primary. One merit, however, is that the switching frequency range is fairly narrow over various line and load combinations. On the other hand, the half wave resonant approach must span a fairly wide range of switching frequencies to maintain regulation for the the same input and output variations, since all resonant tank energy must be delivered to the output.

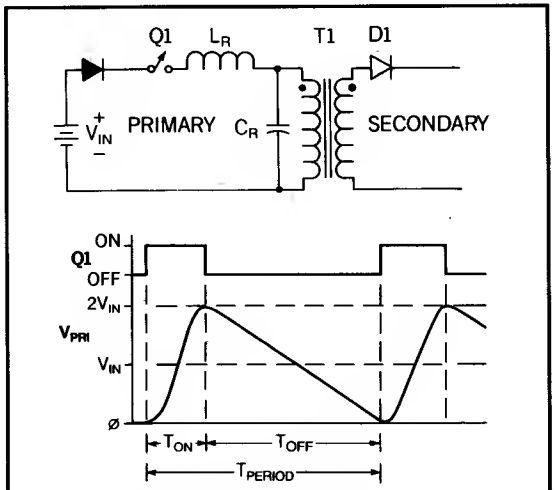

Figure 6 - Primary Side Half Wave Resonance

9

Secondary Side Resonance: Secondary side resonance helps minimize transformer size. With the resonant capacitor located on the transformer secondary side, the volt-second product depends only on the input voltage and transistor *on*time. During the remainder of the period, or *off* time, the transformer is not supporting the resonant capacitor discharge. Lower core losses are attained with this configuration, and are easier to analyze. The waveform is rectangular and is a function of input voltage, *on* time and switching frequency.

Resonant Control Circuit

Refer to the simplified block diagram and waveforms of Fig.8.

Error amplifier: The error amplifier is used to generate an output voltage proportional to the error between the amplifier inuts. A precision reference voltage is at the noninverting input, while the power supply output voltage is applied to the inverting input. The difference between the two is amplified and will respond to millivolt changes in power supply.output voltage, providing tight regulation. The error amplifier output is high when the supply output voltage falls below its setpoint, and a low amplifier output indicates the output voltage is higher than ideal. This variable error amplifier output voltage indicates the need for correction to maintain regulation.

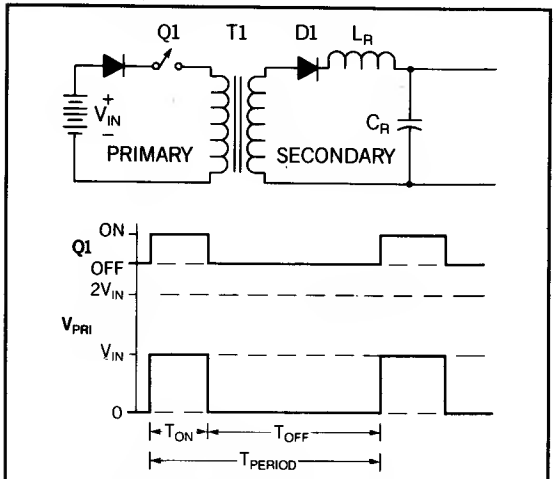

Figure 7 - Secondary Side Half Wave Resonance

Variable frequency oscillator: This device converts a variable input voltage to a variable frequency output pulse train. Increasing input voltage yields an increase in the frequency of the output pulses. Regulation of the output voltage is thus obtained over various line and load combinations by varying the switching (conversion) frequency. The VFO is driven by the error amplifier output voltage and is used to trigger the one-shot pulse generator.

One shot pulse generator: This module generates an accurate pulse width, or duration corresponding to the *on* time required for the resonant tank circuit switches. In fixed *on* time quasi-resonant applications this time constant is set slightly longer than one-half of the full resonant period. Another approach utilizes zero current switching (ZCS) which turns off the switches at zero current. In this application, the one shot is programmed for the maximum circuit on-time and modulated to facilitate ZCS.

Toggle flip flop and gating circuitry: Alternating outputs for "bridge" applications require a toggle flip-flop to divide the VFO frequency by two. This provides out-of-phase drive signals to each of the resonant switches with the proper on-time. In single ended applications like the Buck, Forward and Flyback topologies, toggle function is not used.

High power Mosfet drivers: High peak gate currents are required to deliver sharp Mosfet turn-on and turn-off transitions. The driver accepts low power (TTL) logic inputs and delivers high power (1 to 3 amp peak) Mosfet gate drive compatible outputs.

Zero current switching circuitry: Primary current is monitored and used to turn off the one shot-hence the outputs-when zero current is crossed. This minimizes the switching losses in the primary switches.

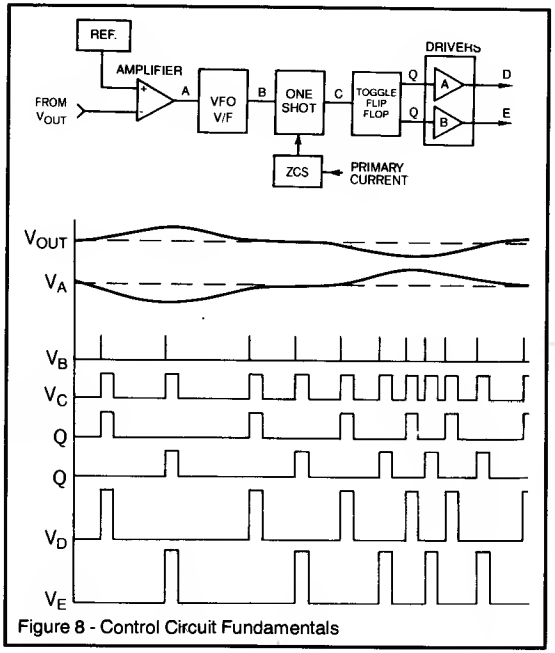

Figure 8 - Control Circuit Fundamentals

Quasi-Resonant Circuit Limitations

One obvious circuit constraint is that the peak resonant current component I_r *must* be greater than I_{out}. Otherwise, zero current will not be reached as shown in the figure below. This relationship specifies the limits of V_{IN} and I_{out} of the resonant tank as a function of the L_r-C_r resonant tank characteristic impedance, Z_r.

Increasing the resonant currrent component far above I_{out} max is one solution, but an inefficient one. The primary switch losses vary with primary current squared, and techniques to minimize this current are required.

The ideal ratio of the output current I_{out} to the minimum resonant peak current $I_{r(pk)}$ min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents and losses. The resonant component initial tolerances and temperature variations need to be analyzed and accommodated by adjusting the ratio of $I_{out\ max}$ to $I_{r(pk)}$. A twenty-five percent safety margin is used in this design corresponding to a ration of 0.75:1.

The resonant L-C elements are now defined *uniquely* by the power supply output voltage and load current for a specirfic resonant tank frequency and current ratio $I_{out\ max}$ to $I_{r(pk)}$.

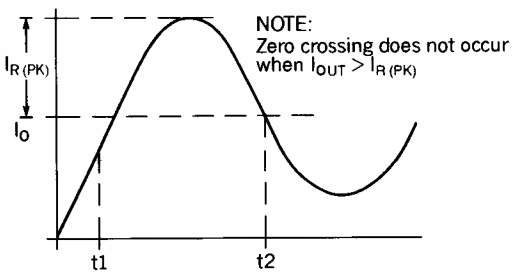

Figure 9 - Inut Current - No Zero Crossing

$$I_{r(min)} = \frac{V_{IN\ min}}{Z_r}, \text{ or } Z_r \le \frac{V_{IN\ min}}{I_{out\ max}}$$

Substituting $Z_r = \omega_r L_r$ and $V_{IN} = V_{sec}$ for secondary resonance, the resonant inductor L_r and C_r are defined by:

1. $L_r = \frac{0.75 V_{sec\ min}}{\omega I_{out\ max}} \Rightarrow \frac{0.12 V_{sec\ min}}{f_{res} I_{out\ max}}$

2. $C_r = 1 / (\omega^2 L_r) \Rightarrow .025 / (f_{res}{}^2 L_r)$

3. Verify that $Z_r < V_{out} / I_{out\ max}$. If not, the ratio of the resonant to output current may need to be altered.

Transformer Turn Ratio

The transformer turns ratio is derived by equating the circuit input and output volt-second products. A topology coefficient K_t is introduced which sepcifies the ratio of the maximum switching frequency to that of the resonant tank frequency. It is somewhat analagous to maximum duty cycle in a square wave converter. Allowing K_t to approach unity in a resonant converter maximizes the turns ratio, thus lowering the primary current.

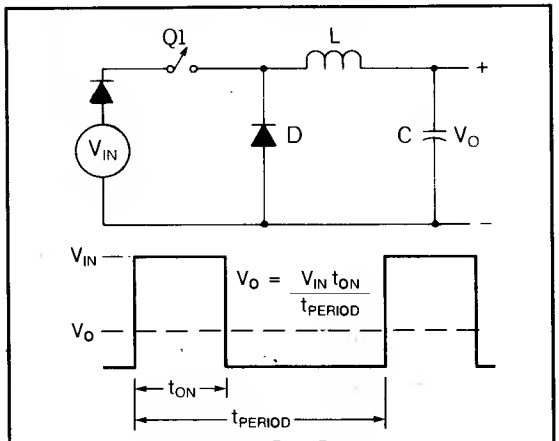

Figure 10 & 11 - Square Wave Buck Regulator

As switching frequencies approach 1 MHz, diode recovery times and Mosfet rise and fall times prevent the topology coefficient from reaching unity. In addition, the resonant capacitor requires time to discharge into the output load. A K_t value of 0.8 is suggested by several of the references listed in the Appendix. The turns ratio can now be calculated from the volt second relationship described previously.

The transformer turns ratio N =

$$V_o = \frac{V_{IN} K_t}{2N}, \quad N = \frac{K_t V_{IN\ min}}{2 V_o}$$

Accounting for the voltage drops, both the primary and secondary:

$$N = \frac{K_t}{2} \cdot \frac{V_{IN\ min} - V_{loss\ pri}}{V_{o\ min} + V_{diode} + V_{loss\ sec}}$$

The actual transformer secondary voltage has now been defined by V_{input} and the turns ratio N. The conversion period or frequency can be extracted from the energy transfer equations in the Appendix by substituting V_{sec} for V_{IN} in the given equations.

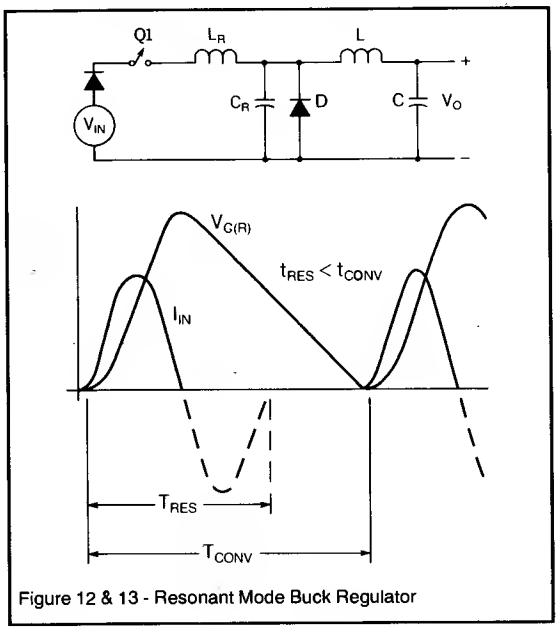

Figure 12 & 13 - Resonant Mode Buck Regulator

Conversion Frequency

As the output load current I_{out} and input voltage V_{IN} vary, the control circuit adjusts the conversion frequency to maintain a constant output voltage, V_{out}. The maximum conversion frequency will occur at low line and full load, where by design, the frequency equals the resonant tank frequency divided by K_t, the topology coefficient.

$$K_t = \frac{f_{conv\ max}}{f_{res}}; \quad f_{conv\ max} = K_t f_{res}$$

Minimum frequency will occur at high line $V_{IN\ max}$ and light load $I_{out\ min}$ which can be estimated by the following relationship:

$$1 / f_{conv\ min} = T_{conv\ max} = \frac{V_{IN\ min}\ Q}{2 N V_o I_{o\ min}}$$

where

$$Q = \left[\frac{2 N L_r I_o{}^2{}_{min}}{V_{IN\ min}} + \frac{V_{IN\ min}\ C_r}{N} + \frac{\pi I_{o\ min}}{2 f_{res}} \right]$$

9

Quasi-Resonant Circuit Relationships

SUMMARY OF APPENDIX1

Timing relationships:

t_o= time when the cycle is initiated
$t_1 = Lr * I_{out} / V_{sec}$
$dt_{21} = \pi/\omega_{res}$
$t_2 = t_1 + dt_{21}$
$dt_{32} = 1/\omega_{res} \times \sin^{-1}(I_{out} Z_r / V_{sec})$

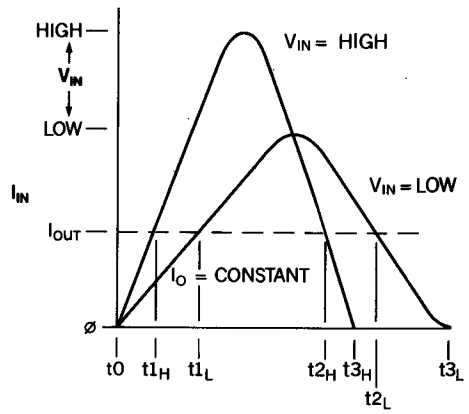

Figure 14 - Effects of Line Change on I_{in}

$t3 = t2 + dt_{32}$
$dt_{43} = V_{C(t3)} C_r / I_{out}$
$t_4 = t_3 + dt_{43}$
$t_5 = [V_{sec} Q_t / (V_{out} I_{out})]$ (approx)

The charge transferred per cycle, Qt, is approximated by:

$Q_t = L_r I_{out}^2 / V_{sec} + 2 V_{sec} Cr + \pi I_{out} / \omega$

Design Procedure and Calculations

The design specifications listed on page 1 will be used for this 150 watt application. A maximum switching frequency of 1 MHz has been selected as a good compromise between the attempts to obtain high power density (small size) and high overall efficiency.

1. Select the maximum switching fequency:

$f_{conv\ max}$ = 1.0 MHz

This also determines the resonant tank circuit frequency using the topology conversion coefficient, K_t.

$K_t = f_{conv\ max} / f_{res}$. Use $K_t = 0.8$

2. Calculate the resonant tank frequency, fres

$f_{res} = f_{conv\ max} / K_t = 1\ MHz/0.8 = 1.25\ MHz$

3. Determine the transformer turns ratio, N

$N = N_{pri} / N_{sec} = K_t V_{IN\ min} / (2 V_{out} + V_{diode})$

= 5.19 (use 5:1)

4. Calculate $V_{in\ min}$, the minimum input voltage referred to the secondary:

$V_{in\ min} = V_{s\ min} / 2N = 220V/(2 * 5) = 22V$

The resonant inductor and capacitor values are calculated using the minimum input voltage to the secondary.

5. Calculate the resonant inductor value, L_r

$L_r = 0.12V_{in\ min} / f_{res} I_{out\ max} = 176$ nH

6. Calculate the resonant capacitor value, C_r

$C_r = .025 / f_{res}^2 I_{out\ max} = 90.9$ nF

7. Calculate and check resonant impedance Z_n

$Z_n = (L_r / C_r)^{1/2} = 1.39\Omega$ (yes, < 1.5 ohms)

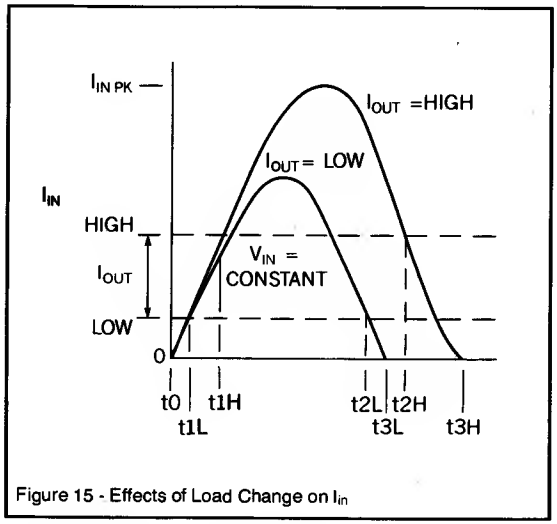

Figure 15 - Effects of Load Change on I_{in}

The basic sections of the circuit are now complete. Detailed analysis of the primary and secondary voltages and currents follow.

Peak Current calculations: The peak secondary current is approximated by :

$I_{sec\ pk} = I_o + V_{in} / Z_n = I_o + V_s / (2 * N * Z_n)$

$= .072\ V_s$

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

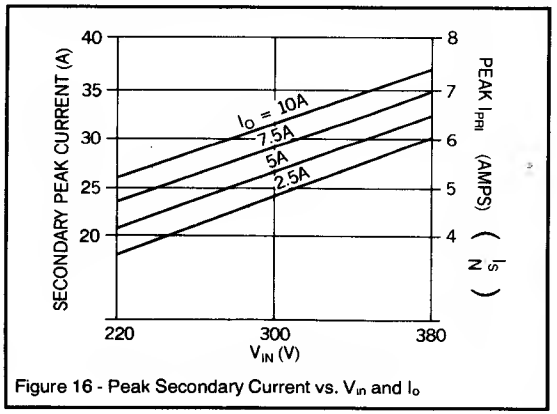

Figure 16 - Peak Secondary Current vs. V_{in} and I_o

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

The peak secondary voltage is:

$V_{s\,pk} = V_{s\,max}/2N = 370/2 * 5 = 37V$

Rectifiers in the secondary circuit need to block at least twice the peak voltage, and are typically selected with a much higher rating. Schottky diodes can be ruled out in this 15V output application due to their 45 to 90 volt breakdown voltages, so an ultra to hyperfast diode is required. A 150 volt, 30 amp (DC) device provides ample safety margin. A low capacitance power package is also desired to minimize parasitics and power losses.

rms current calculations: The primary and secondary RMS currents can be approximated to a high degree of accuracy by a pulsed sinusoidal waveform. The relationships derived in the previous section for peak currents, on times and conversion frequencies will be used to calculate the RMS currents incorporating the following equation.

$$I_{rms} = I_{peak}\left[\frac{T_{on}}{2\,T_{per}}\right]^2$$

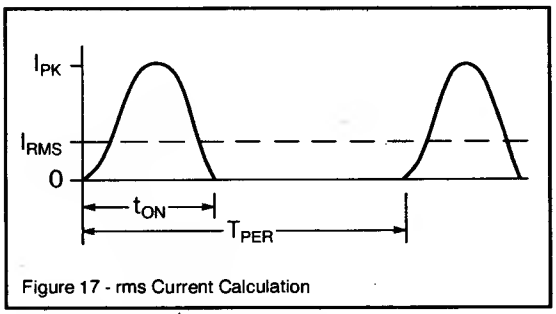

Figure 17 - rms Current Calculation

The primary current calculations will use the conversion period of 1/fconv due to the bidirectional switching of the primary. Secondary currents conduct only once per two conversion periods due to the bridge arrangement of the secondary windings. Both low and high input voltage conditions will be examined at full output load to determine worst case conditions.

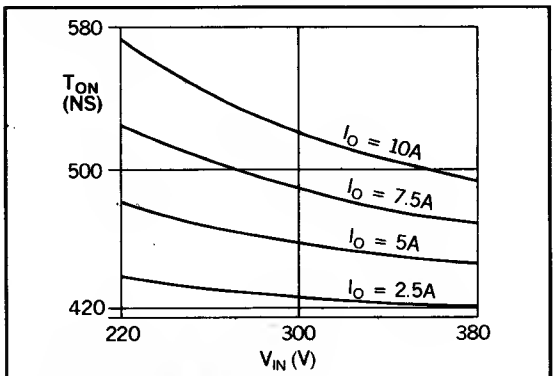

Figure 18 - On Time vs. V_{in} and I_{out}

The transformer primary wire size will be calculated using the rms current components, in addition to thermal considerations of the transistor switches and rectifiers.

Each of the Mosfet switches, secondary rectifiers and transformer secondary windings conduct current only once per two conversion cycles. This results in a lower rms current through each device.

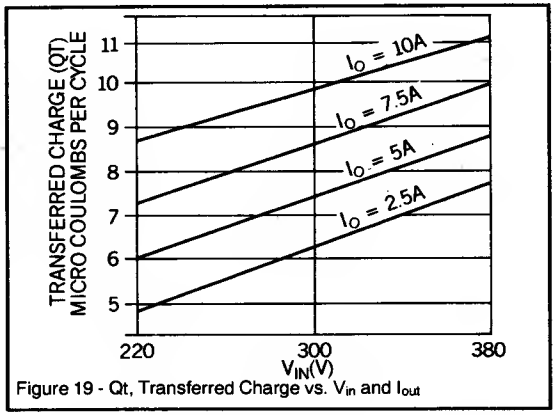

Figure 19 - Qt, Transferred Charge vs. V_{in} and I_{out}

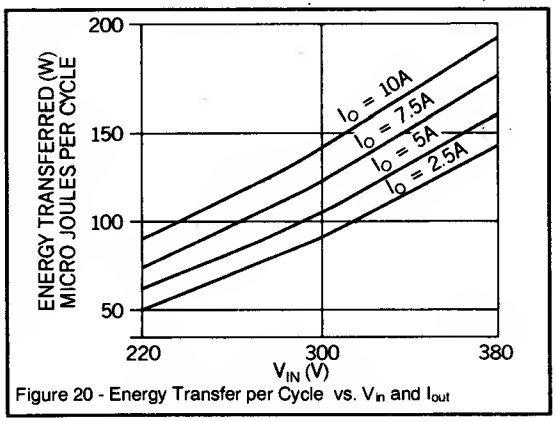

Figure 20 - Energy Transfer per Cycle vs. V_{in} and I_{out}

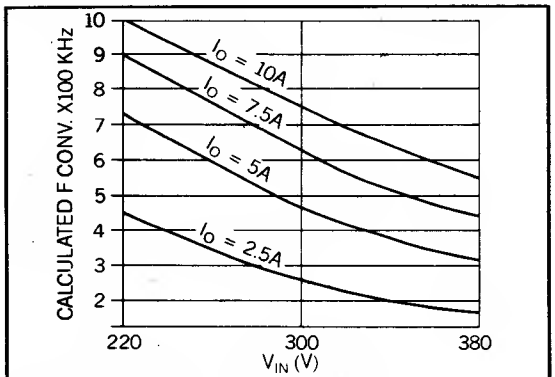

Figure 21 - Calc. Conversion Freq vs. V_{in} and I_{out}

9

Low Line	High Line
$I_{sec\ pk}$ = 26 A	$I_{sec\ pk}$ = 37A
$I_{pri\ pk}$ = 5.2A	$I_{pri\ pk}$ = 7.4 A
t_{on} = 575 ns	t_{on} = 495 ns
T_{per} =1.0 µs	T_{per} = 1.82 µs

rms Transformer Primary Currant:

$I_{pri\ rms}$ = 2.78 A $I_{pri\ rms}$ = 2.72 A

rma Current - Mosfet Switches and Secondary Ractifiers:

$I_{rect\ rms}$ = 9.86 A $I_{rect\ rms}$ = 9.65 A
$I_{MOS\ rms}$ = 1.97 A $I_{MOS\ rms}$ = 1.93 A

Timing Conaiderations: The operation of this quasi-resonant circuit has been described as requiring a variable frequency, *fixed on time* control pulse train. Actually, the on time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented earlier, the on time is calculated and plotted for the ranges of V_{in} and I_{out} in Fig. 18.

Transfarradcharge: The charge transferred from the primary to the secondary per cycle is a function of both V_{in} and I_{out}. Using the equations presented in the Appendix, the results are graphically represented in Fig. 19.

For the selected values of voltage and current shown, the average change required in voltage or output current per microCoulomb transferred havd been calculated.

Avg dV/µC = 5.935, and Avg dI/µC = 2.086

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by $V_{in}/2$ to convert from charge to energy, with the results shown in Fig. 20.

The conversion period is obtained by dividing the energy transferred per cycle by the output power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for varius input voltages and output currents in Fig. 21.

Power Mosfet Switch Considerations

The power Mosfet selection process must take into account the three types of losses incurred by the high voltage switch. First, and probably the most predominant loss contributor is the FET *on* resistance, or $R_{ds(on)}$. Conduction losses are minimized by using a FET with the lowest $R_{ds(on)}$ obtainable.

$P_{loss\ dc} = I_{pri\ rms}{}^2\ R_{ds\ (on)}$ (Watts)

Generally the low resistance is attained by paralleling numerous FET cells of higher on resistance. The result is a single high current, low resistance device with a large die size, or geometry. This technique is great for lower frequency applications where the transition (turn-on and turn-off) times are a small percentage of the entire duty cycle. At high frequencies and especially with high voltages, this paralleling scheme introduces many difficulties in minimizing the switching transition losses.

Each cell has a finite output capacitance which quickly "adds up" when many are placed in parallel. The FET output capacitance is charged and discharged to the FULL input bulk voltage each cycle, contributing losses. At high frequencies, changing to a larger size FET could increase the total FET losses, despite having a lower *on* resistance. The incremental gains of lower conduction losses are lost to the higher switching losses of the larer capacitance FET. For this reason, it is a worthwhile exercise to examine several different size FETs over the line and load ranges of this design.

$P_{loss\ ac} = 0.5 C_{oss}\ V_{in}{}^2 f_{conv}/2$ (watts)

The gate drive power losses are generally negligible with respect to the total losses, but can be calculated from:

$P_{loss\ gate} = 0.5 V_{aux}\ Qt\ f_{conv}/2$ (Watts)

where Q(t) is the FET total gate charge, accounting for the gate to source charge plus the Miller effect charge.

The greatest primary current occurs at full load, which will be used for the worst case evaluation of power losses. Both high and low input voltage were used to calculate the ac losses, then averaged. The following list is a summary of the total power loss for each Mosfet switch in this application. A 100°C junction temperature at the FET die was assumed, where the actual *on* resistance is double that of the published specification. Various size FETs have been analyzed to compare the ac and dc losses to select one which exhibits the lowest total losses.

Circuit specifica (at the FET awithces):

$I_{pri\ rms}$ = 1.97A at V_{in} = 220V, f_{conv} = 1 MHz

$I_{pri\ rms}$ = 1.93A at 375V, 550 KHz

Device	Rds	Coss	Qg	Pdc	Pac	Pg	Ptotal
aa)							
IRF720	3.6	64	20	13.7	1.05	0.08	14.87
IRF730	2.0	100	35	7.62	1.57	0.11	9.30
IRF740	1.1	210	63	4.19	3.30	0.19	7.68
IRF820	6.0	54	19	22.8	0.85	0.07	23.78
IRF830	3.0	91	32	11.4	1.43	0.10	12.96
IRF840	1.7	180	63	6.47	2.83	0.19	9.49
IRFP440	1.7	180	63	6.47	2.83	0.19	9.49
IRFP450	0.8	350	130	3.04	5.51	0.39	8.95
IRFP460	0.54	480	190	2.05	7.56	0.57	10.19

The lowest overall losses are obtained with the 740 type devices which will be utilized in this application. This procedure will yield different results for each application, and is a recommended step towards minimizing power losses.

Rectifier Selection

Evident from Figures 16 and 17 is the need for high performance rectifiers to achieve an overall high efficiency power supply. Peak secondary currents approach 40 amps, with an rms component near 14 amps. Due to the high peak reverse voltages of nearly 100 volts, Schottky diodes cannot be used as the secondary rectifiers. Even the "freewheeling" diode must withstand 80 volt peaks at high line.

Reverse recovery times must be minimal to prevent reverse current from flowing in the primary switches in addition to enhancing efficiency. While the circuit currents are quasi-sinusoidal, the rectifier voltage is not. Parasitic inductances and capacitances of the device and its package must also be accounted for as part of the resonant L-C tank. This implies that the transformer will be designed for a lower leakage inductance than the resonant L and external inductance will be introduced to obtain the precise amount.

The To-247 package will be utilized for two reasons. First, it has lower parasitics and is better suited to high frequency applications than its To-3 metal case counterpart. Second, it is simple to heatsink this flat package, which can be mounted in various configurations.

Unitrode UES3015S ultrafast 30 amp, 150 volt rectifiers were selected for the secondary input diodes. Typical performance characteristics are 35 ns reverse recovery times and less than 1 V forward drop at 30 A and 125°C junction temperature. The "freewheeling" diode used is a Unitrode UES1615S ultrafast type, with 16 amp dc capability and a forward drop of less than 0.85 V. It too exhibits a 25 ns reverse recovery time.

Power dissipation and heatsinking requirements for each device can be calculated using the secondary currents obtained previously in this power supply design. Snubbing of each diode will be left to the prototype stage when any parasitic circuit influences can be evaluated.

Main Transformer Design

The transformer design begins with a basic idea of the core geometry most applicable to the particular design. Off-line supplies lend themselves to low, wide winding windows, typical of the ETD geometry. This window shape provides adequate room to accomodate the creepage and clearance distances required for international safety specifications.

Switching of the transformer primary will occur at a maximum of 500 KHz, and standard ferrite materials will be utilized in this example. With numerous choices to consider, the 3C6A material was selected.

To begin this 150 watt design, a fair estimate is to keep the transformer losses around 1% of the total input power, or approximately 2 watts. In addition, the transformer temperature rise is desired to be less than 40°C for combined copper and core losses. A core size can be approximated knowing that its thermal resistance, R_t, needs to be in the neighborhood of 40°C/2W, or less than 20°C/W. This is useful as a first iteration to determine the approximate operating flux density required. The precise size will be calculated using the area product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} \cdot 10^4}{120 K 2f}\right]^{1.58} \cdot (K_h f + K_e f^2)^{0.66} \quad cm^4$$

where:

Pin - Input Power = 180 Watts
K - Winding Factor = 0.163 for half bridge
f - Transformer Frequency = 500 KHz
K_h - Hysteresis Coeff. (3C6A) = 1.10^{-5}
K_e - Eddy Current Coeff. (3C6A) = 4.10^{-10}

For this design, the area-product calculates to 0.543 cm^4, which is slightly less than the smallest standard core size, the ETD-34. Because the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19°C/W, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between the core and copper can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accomodate fewer turns, or less copper. The actual core power density, P_d, is calculated from the following equation, allowing a 20°C temperature rise, T_r, due solely to core losses.

$$Power\ Density = \frac{T_r}{R_t \cdot Vol} = \frac{20°C}{19 \cdot 7.64}$$

Referencing the manufacturers data sheet for the 3C6A material at a power loss density of approximately 140 mW/cm^3 and a 500 KHz operating frequency, it is determined that an operating flux density of 300 gauss (0.030 T) be used. The total flux density swing, ΔB, is twice that, or about 0.060 Tesla. The minimum number of primary turns is calculated assuming 5 V primary drops, low line conditions, and a cross-sectional core area, A_e, of 0.971 cm^2.

$$Power\ Density = \frac{V_{pri}\, t_{on} \cdot 10^4}{\Delta B \cdot A_e}$$

$$= \frac{105 \cdot 575 \cdot 10^{-9} \cdot 10^4}{.060 \cdot 0.971} = 10.3 turns \quad (use 10)$$

A turns ratio N of 5:1 was previously established for this design. Minimized leakage inductance is obtained by "sandwiching" the secondaries between the two primary halves. In this example, one-half of the primary turns will be wound first, closest to the core center leg. Then, the entire secondary is wound directly above the primary half. The final winding is remaining primary half, as shown in Fig. 22.

Copper strip or foil will be used for each winding to minimize "build-up" which increases the distance between windings, hence increases leakage inductance. If the transformer leakage inductance is greater than the required resonant inductance, then the transformer must be redesigned for lower leakage.

The required primary and secondary copper cross-section areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

Primary current rms current, $I_{pri\ rms}$ = 2.78 A rms
Secondary rms current, $I_{sec\ rms}$ = 9.86 A rms
Primary copper area, Axp = $I_{pri\ rms}$/450
= .0062 cm^2

Secondary copper area, $A_{xs} = I_{sec\ rms}/450$
= .022 cm^2

Pri. inductance, $L_{pri} = A_L N_p^2$ = 190μH
Sec (half) inductance, $L_{sec} = A_l N_s^2$ = 7.6μH

The primary conductor area is approximately equal to the area of an AWG # 19 wire, while the secondary area is closest to AWG # 14. Eddy current calculations show that the depth of penetration at 500 KHz is .0106 cm, or about the thickness of anumber 37 AWG wire. The most practical technique to minimize the AC loss in a transformer windingt is to use copper strip or foil, as in this design. Its width is determined by the bobbin width and safety creepage requirements requirements of 8 millimeters as shown.

The required 8 mm primary to secondary spacing between winding ends will be subtracted from the bobbin width of 2.10 cm, leaving 1.30 cm (0.51 inch) for the copper strip width. Allowing for tolerances, standard 0.5 inch width foil will be used in this design. The strip thickness is calculated by dividing the required copper area by the 1.27 cm (0.5 inch) width.

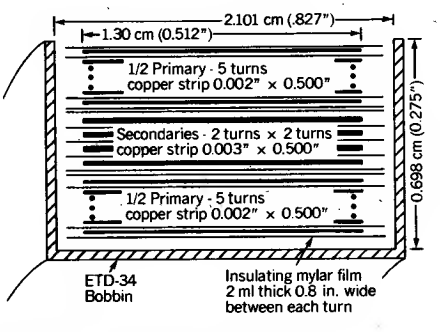

FIGURE 22 - Transformer Winding Layout

Pri thickness = A_{xp}/Width = $6.18 \cdot 10^{-3}/1.27$
= .00475 cm, or .00187 in

Sec Thickness = A_{xs}Width = $2.19 \cdot 10^{-3}/1.27$
= .01685 cm, or .00663 in

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Standard 2 mil (0.0051 cm) foil will be used for the primary. This is slightly larger than the required thickness of .00475 cm, and is less than 1/2 the .0106 cm penetration depth. Secondary penetration is from both sides because of the interleaved primary, so the calculated secondary thickness should be and is less than twice the penetration depth. Two paralleled 3 mil foils are used as secondary conductors.

The resistance and power loss of each winding is calculated from the following relationships, based on the resistivity of copper at 100°C, $p_{cu} = 2.29 \cdot 10^{-6}$ Ω-cm. Total copper and core losses are also highlighted, in addition to the toal temperature rise at the maximum conversion frequency.

$$Winding\ resistance = \frac{p_{cu} \cdot avg\ length\ turn \cdot N}{A_x}$$

$R_{pri} = 2.29 * 10^{-6} * 5.99 * 10/6.18 * 10^{-3} = 22.2\ m\Omega$
$R_{sec} = 2.29 * 10^{-6} * 5.99 * 2/2.19 * 10^{-3} = 1.25 m\Omega$
$P_{loss\ winding} = I_{rms}^2 * R$
$P_{loss\ pri} = 2.78^2 * .0222 = 171\ mW$
$P_{loss\ sec} = 9.86^2 * .00125 = 121.5\ mW$
$P_{loss\ copper} = 2 * 0.171 + 0.1215 = 0,4635\ W$
Total power loss = copper losses + core loss
$P_{total} = 0.464 + 1$ (approx) ≤ 1.5 W
Temp. rise = Rt x P_{total} = 19°C/W x 1.5W
= 28.5°C

Output Inductor Design

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHz. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. This mode of operation helps lower the overall losses at full load because with lower ripple the peak current that must be switched is less. In addition, it reduces the size of the output choke since the peak (DC + AC) and full load (DC) current are withinone percent of each other.

$L_o = [(V_{out} + V_{diode}) * t_{off\ max}] / \Delta I_{out}$

= 15.8V x 5 us / 1 A = 80 μH (approx)

At the maximum conversion frequency and $t_{off\ min}$, the output ripple current reduces to:

$\Delta I_{out} = [(V_{out} + V_{diode}) \times t_{off\ min}] / 80\ \mu H = .08A$

Referring to Section M5 of the Unitrode Seminar Manual, core selection starts by calculating the area product:

$$AP = A_w A_e = \left[\frac{L_o I_{pk} I_{fl} \cdot 10^4}{420 \cdot K \cdot B_{max}}\right]^{1.31}$$

A PQ type geometry has been selected for the output choke application. The core set closest in size to the required area product is the PQ 32, which is available in either a 20 or 30 mm height. Of the two, the PQ32/20 size will be used because its height is similar to the ETD34 core set used for the main transformer. Its magnetic area is 1.70 cm^2.

$$N_{min} = \frac{L \cdot I_{pk} I_{fl} \cdot 10^4}{B_{max} A_e}$$

$$= \frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10^4}{0.30 \cdot 1.7}$$

The cores will require gapping to store the required energy without saturation. Gap length is calculated from the inductance formula:

$l_g = (\mu_o \mu_r N^2 A_e \cdot 10^{-2}) / L = 0.68 cm$

using $\mu_o = 4\pi \cdot 10^{-7}$ and $\mu_r = 1 (air)$

Correcting the gap length for the fringing field, a gap of .082 cm (.032") should be used.

Again, copper strip is used to minimize losses. Winding resistance and power loss calculations are similar to those of the main transformer design, and total less than 1.5W.

OUTPUT CAPACITOR

There are two components of ripple voltage which need to be considered in meeting the design goal of 100 mV. They are both caused by inductor ripple current. The first is simply:

$\Delta V_{out} = DQ / C_{out}$

For a given ripple current, this component is minimized by increasing the capacitor value. If this were the only contributor, the minimum capacitance required is:

$$C_{outmin} = \frac{1}{2} \frac{\Delta I_{out}}{2 f \Delta V_{out}}$$

This component varies with frequency. At $f_{conv\ min}$, 6.25μF are needed, but at $f_{conv\ max}$ (1MHz) only 0.1 μF is required to maintain the ripple voltage specification.

The second (and usually predominant) ripple voltage component is the voltage drop across the capacitor Equivalent Series Resistance (ESR) caused by the ripple current of ΔI_{out}. The maximum ESR allowable for 100 mV ripple is:

$ESR_{max} = 100\ mV / 1.0\ A = 100 m\Omega$

The two ripple voltage components do not add directly as they are in quadrature. With electrolytic capacitors, the ESR component dominates the capacitor selection. The resulting capacitance value is so much greater than the minimum value required that the $\Delta Q/C_{out}$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

In this design, two 100 μF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 milliohms - a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers.

A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electryolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolithic capacitors are used for this application. Different capacitor types and values can be paralleled to obtain a low impendance over a broad frequency range, useful in this variable frequency application.

Gate Drive Circuitry

The ideal gate drive circuit must deliver sharp turn-on and turn-off pulses to the high voltage power Mosfets. This is made possible by the UC3860 controller's high speed totem pole drivers. Delivering 3 amp peak currents, the drivers have typical rise and fall times of 25 ns into a 1 nF load.

Half bridge circuits require the use of a gate drive transformer to electrically isolate the "high-side" switching transistor from the control circuit. Driving both transistors from the same transformer 180° out of phase offers nearly identical drive signals to each transistor. This tends to balance the switching losses and maintain a narrower band of the associated transition EMI.

The drive transformer must have low leakage inductance to provide crisp edges during the transitions with little overshoot. This makes zener clamps and snubbing circuits unnecessary at the transformer outputs. A 0.50" O.D. toroid is used, fitted with three identical windings of ten turns each. This helps minimize the transformer magnetizing current and maximizes the peak current delivered to the FET gates.

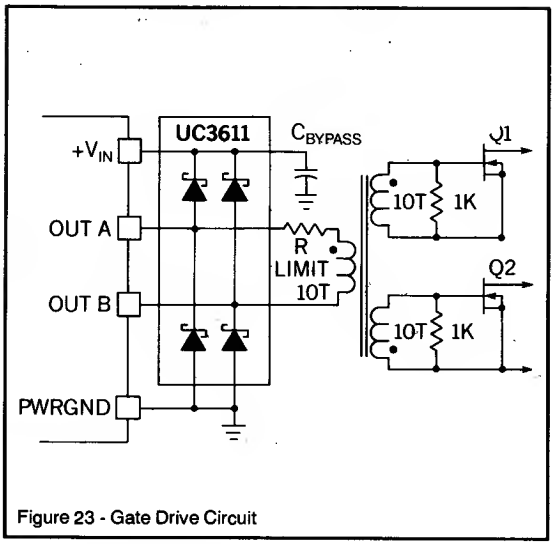

Figure 23 - Gate Drive Circuit

Resistors from gate to source at each FET provide a fairly low impedance to prevent turn-on during start-up while the IC may still be in undervoltage lockout. During regular operation, these resistors have negligible impedance.

On the controller side, the UC3611 quad Schottky diode prevents the ICoutputs from going below ground, avoiding substrate biasing problems. A series resistor limits the peak current to the 3 A rating, and the transformer is reset while both outputs are low, between cycles.

Zero Current Detection and Switching

The primary currrent is used for two important functions in this design, fault protection ans zero current detection. A typical configuration is shown in Fig. 26. The generalized circuit starts with the use of a current transformer in series with the primary of the main transformer to detect primary current. A turns ratio of 1:25 reduces the switch current to a manageable level. It is full wave rectified by 1N4148 diodes (D_6-D_9) and converted to an appropriate unipolar voltage at the current sense resistor, R_{11}. In addition, zero current or zero voltage can be detected by using the UC3860 uncommitted comparator. Its open collector output can interface with the RC on timing pin of the one shot, pulling it below the turn off threshold at zero detection. As shown in Fig. 24, this reduces the on time of the one shot timer, allowing the Mosfets to switch at zero current for high efficiency.

Implementation reqires shifting the noninverting input between two thresholds so that only the falling edge of primary current is an acceptable input for switching to occur. (See Fig. 25). This is done to prevent a false output from the comparator during the beginning of the cycle, where zero current also occurs. Primary current sensing will be offset by the resistor divider network R_{21} and R_{16} from V_{ref} to ground. This is fed into the invering input of the uncommitted comparator.

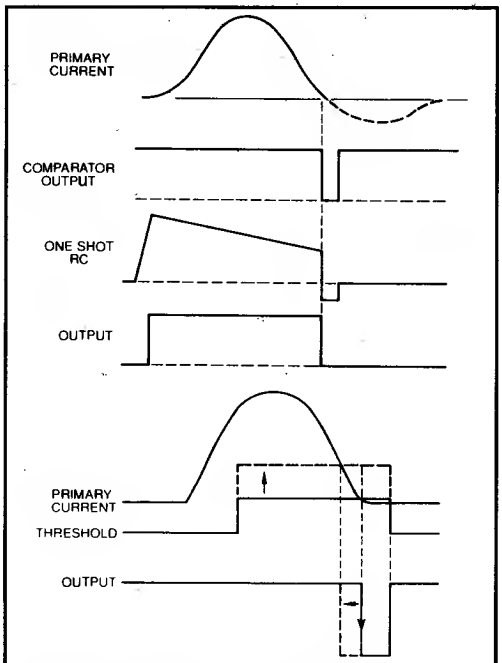

Figure 24 & 25 - Zero Current Switching

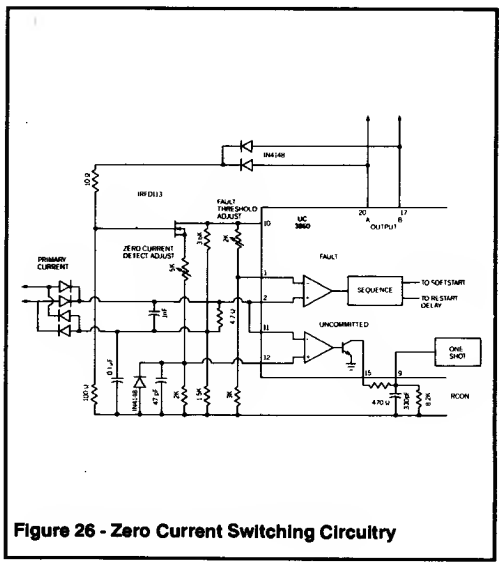

Figure 26 - Zero Current Switching Circuitry

In Fig. 26, adjustments can be made to provide a comparator output *just* prior to zero current by resistor R20. Propagation delays through the IC and drive circuitry, although minimal, can effectively be "nulled-out" along with Mosfet delays by this technique.

The UC3860 Resonant Mode Control IC

The block diagram of the UC3860 in Fig. 27 displays several key building blocks which together provide the functions necessary for precise resonant mode control. To begin, the undervoltage lockout turn-on and turn-off thresholds are pre-programmed for 17 and 10 volts respectively and are used in their standard configuration. This allows ample time for start-up and bootstrapping to occur in an off-line supply while providing adequate Mosfet gate drive voltages. The UVLO can also be reprogrammed for other turn-on and off thresholds. Also, it functions as an alternate shutdown mechanism. While UVLO is invalid, the UC3860 reference voltage output is held low, deactivating the internal circuitry. The 1% accuracy 5.0 V bandgap reference is capable of driving ten milliamps maximum external loads.

The power supply output voltage will be divided down to deliver 3.0 volts at the inverting error amplifier input for the desired V_{out}. With its high gain-bandwidth of 5 MHz, this voltage type op amp also features controlled output voltage excursions. The error amp output swings from 0.0 to 2.0 V above the voltage at the VFO I_{osc} input and tracks this node over temperature. This mechanism facilitates the maximum conversion frequency clamp in addition to the voltage (or current) to frequency conversion gain.

Variable frequency operation commences with the error amplifier providing a variable output voltage. This is transformed to a variable current at the VFO variable current input, I_{vfo}. Internal circuitry mirrors this current to the VFO timing capacitor, C_{vfo}. Maximum frequency occurrs at $2.0V/R_{vfo} * C_{vfo}$, which coincides with the error amplifier upper clamp. Minimum frequency is also programmable via resistor R_m from V_{ref} to the I_{vfo} input. The frequency to voltage gain of the IC in MHz/V (or GHz/V) is also established by these timing components. Additionally, the VFO can be externally triggered and/or disabled at the respective input pin accomodations.

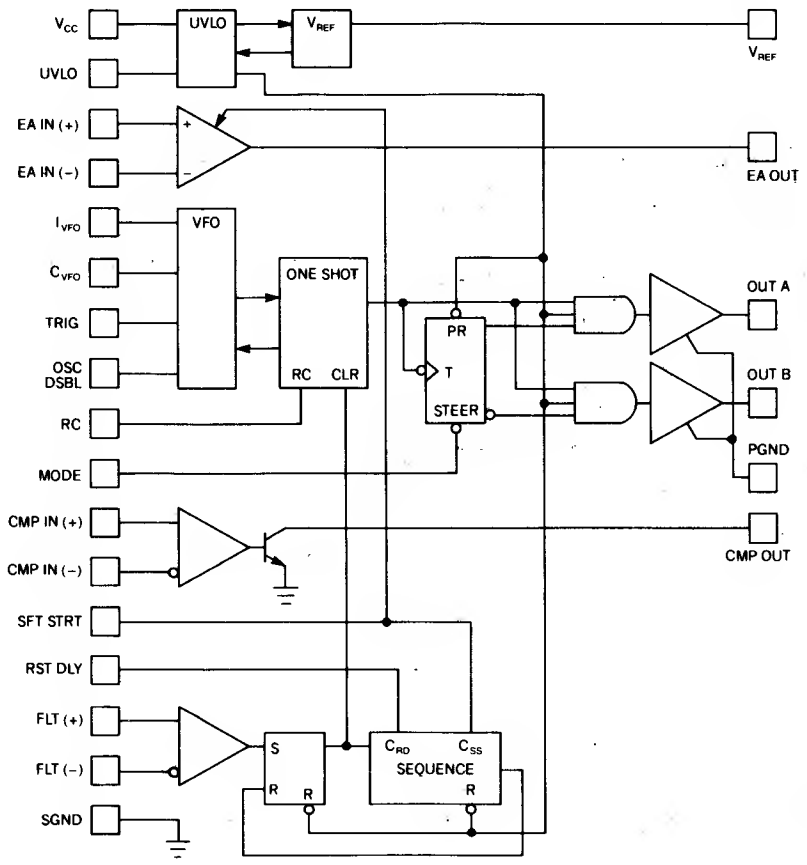

Figure 27 - UC3860 Block Diagram

Fixed on-time pulse widths are generated by the programmable one-shot timing circuit. An RC network is charged by an internal source at the onset of a cycle, then self discharges during the on-time. This occurs between the precise thrsholds of the one-shot's comparators. On-time can easily be shortened by an external influence used to discharge the RC components below the comparator's turn-off threshold. This architecture simplifies interfacing with various forms of zero voltage or zero current type switching. The output of the UC3860 uncommitted comparator is an open collector which can interface directly to the one shot (RC) timing pin.

Programming the VFO and One-shot:

Let C_{vfo} = 330 pF, $C_{oneshot}$ = 330 pF
f_{max} = 1.05 MHz, f_{min} = 200 KHz

1. $f_{max} = 2V/R_{vfo}\ C_{vfo}$;
$R_{vfo} = 2/(1.05MHz * 330\ pF) = 5.77\Omega$

2. $f_{min} = 1V/R_m\ C_{vfo}$;
$R_m = 1/(0.2MHz * 330\ pF) = 15.5\ k\Omega$

3. $t_{on} = 0.22 * R_{on} * C_{on}$;
$R_{on} = 600ns/(0.22 * 330\ pF) = 8.26\ k\Omega$

The output from the one-shot feeds another programmable module, the toggle flip-flop. Logic selection at the Output Mode pin either alternates the outputs for the dual-ended configurations, or unifies outputs A with B for single ended applications. As V_{ref} becomes valid, the toggle flip-flop is always steered towards the A output. While this may be of little concern in some designs, a predictable sequence of events upon power-up is always facilitated.

Each totem-pole output is specified for 3 Amp peak drive pulses, sufficient to insure abrupt transitions at the Mosfet switches. When operating in unison, a 6 A peak current is obtained. Rise and fall times into a 1 nF load are typically 20 nanoseconds. As seen in previous high power IC's, the totem pole power ground is terminated through a separate pin which isolates its power ground noise from that of the IC's signal ground.

Soft start is accomplished by limiting the amplifiers output voltage to that of the soft start pin, typical in most IC controllers. An internal 5 microamp current source from V_{ref} pulls up on the external soft start capacitor, which gradually increases the conversion frequency upon start-up, as opposed to widening the pulse width in conventional PWMs.

Fault protection and management circuits included in the UC3860 are fully user programmable. A fault comparator which has both inverting and non inverting inputs is used to drive a programmable sequence latch. The operation of this latch is controlled at the programmable Restart Delay (RST DLY) pin, and has three unique modes. First, it can be oriented to latch the outputs off until UVLO or V_{cc} are toggled, similar to firing a shutdown SCR. Secondly, it can be used to cease operation until the fault input is removed from the comparator, then recommence operation. The third and most popular mode is often referred to as "hic-cup" mode. After receiving a fault, the outputs are turned off for a programmed time interval called the restart delay. Operation is then resumed, provided of course that the fault was removed. Implementation only requires a capacitor from RST DLY to ground.

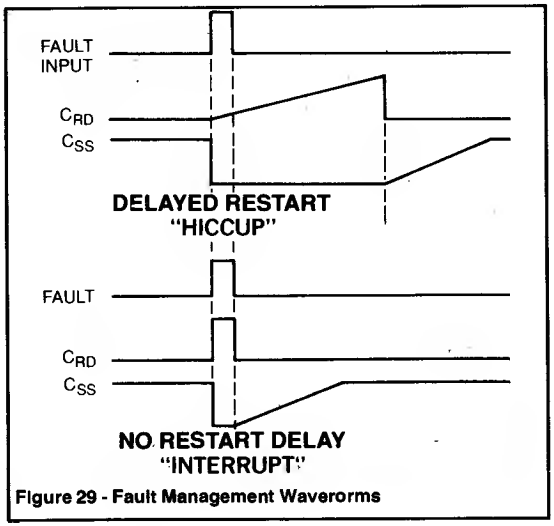

Figure 29 - Fault Management Waverorms

Closing the Loop

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

Error Amplifier: A reference voltage is applied to the noninverting input of the error amplifier, and the power supply output voltage, through a voltage divider, is applied to inverting input. The error amplifier (E/A) output is commonly referred to as the error voltage V_e, which is an amplifier signal corresponding to the deviation of the power supply output voltage from the desired level. The compensation network is designed last, after analyzing the other loop gain contributors. It will provide adequate phase margin at the desired zero dB crossover point to ensure circuit stability.

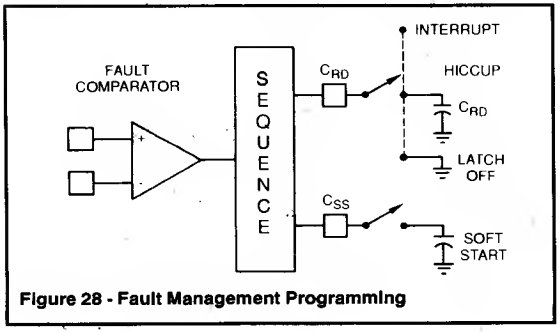

Figure 28 - Fault Management Programming

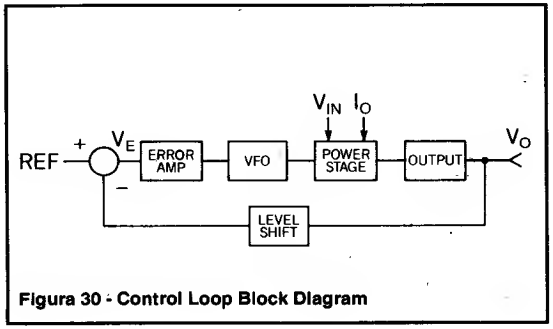

Figura 30 - Control Loop Block Diagram

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The varying E/A output voltage V_e is used to gnerate a variable current to the VFO current input pin, I_{vfo}. As this current is varied, so is the power stage conversion frequency. A higher V_e corresponds to a higher conversion frequency. These values are designed to track each other over temperature, and a linear voltage to current transformation can be assumed. The voltage to current gain into the VFO equals the 2 volt maximum output swing of the error amplifier divided by the VFO input resistor.

Variable frequency oscillator: The variable frequency converter stage accepts an input current at the I_{vfo} input and generates a proportional output frequency. The gain of this stage is programmed by the E/A output voltage with the I_{vfo} input resistor and the VFO timing capacitor, C_{vfo}. The VFO output frequency is approximated by:

$f_{osc} = I_{vfo} / C_{vfo}$, and $f_{max} = 2V/(R_{vfo} * C_{vfo})$

The minimum frequency is programmed by a resistor from V_{ref} to the I_{vfo} input, and the transformation of the error amplifier output voltage to frequency is quite linear.

Error amplifier voltage swing = 2 Volts

f_{conv} = 200KHz min = 1 MHz max

VFO gain:

$G_{vfo} = \Delta 800$ kHz / $\Delta 2$ V = 0.4 MHz/V

Power stage: The small signal gain of the power stage is approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch *on* time is constant, and any changes in frequency directly effect the *off* time, or resonant capacitor discharge time. In addition, both V_{IN} and I_{out} are assumed to be constant during the interval of interest.

Based on the relationship that the energy into the resonant circuit, W, equals the output power multiplied by the conversion period:

$W = (Q_{in} V_{sec} / 2)$ = Power * t_{conv}
$= V_{out} I_{out} / f_{conv}$

therefore:

$V_{out} = f_{conv} W / I_{out}$

This term is assumed constant for the interval of interest.

Tabulated below at several points of interest are the values for the values for the power stage gain, from the results of a previous section in this presentation. The gain (in volts per MHz) varies significantly over the input and output ranges and the highest value will be used to approximate the worst case conditon.

V_{IN} sec V	I_{out} A	W_{in} µJ/cyc	f_{conv} kHz	Gain V/MHz	Gain dB
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	21.4	26.6
22	7.5	78	900	19.3	25.7
38	7.5	185	450	22.6	27.0
22	10	91	1000	19.1	25.6
38	10	205	560	23.6	27.5

The worst case value of 23.6 V/MHz will be used for the power stage. Multiplying this by the VFO gain of 0.4 MHz/V results in a combined gain V_{out}/V_e of 9.44 (19.5 dB).

Output Filter Section: The output filter response is defined by:

L_{out} = 80 µH; C_{out} = 200 µF

R_{out} = 1.5 Ω min to 10 Ω max

ESR = 2 to 10 m Ω

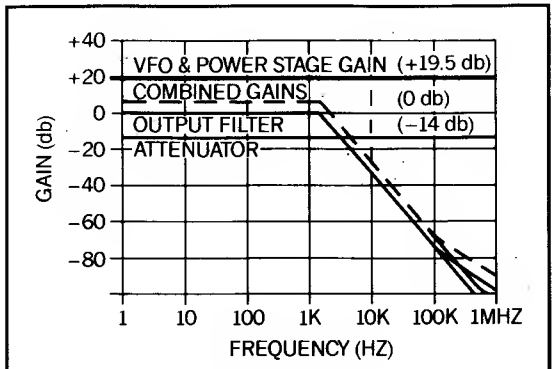

Figure 31 - Gains vs. Frequency

$$\text{Pole frequency} = \frac{1}{2\pi \left(L_{out}\, C_{out}^{0.5}\right)} = 1.25\ kHz$$

$$\text{ESR Zero} = \frac{1}{2\pi C_{out}\, ESR} = 79.6 - 398\ kHz$$

The output voltage divider shifts the level of the 15 V output to the required 3 V error amplifier input, resulting in a gain of -14 dB.

Compensating the quasi-resonant converter: The generalized approach to this compensation is to place the first pole at a low frequency, typically arond one hertz. Two zeros are then introduced at approximately the output filter break frequency to compensate for its two pole rolloff. A second pole is place at a fairly high frequency to roll off the loop gain in a predictable manner. Unlike their predecessors, the newer control Ics rarely run out of gain bandwidth and require this high frequency pole.

Most of the previously described elements can be lumped together into one gain vs. frequency Bode plot of everything except the error amplifier, as shown in Fig. 31. The VFO, power stage and level shifting voltage divider have gains that are independent of frequency, and are easily combined. The output filter section response is then multiplied by the combined gain of the previous calculation. One curve now depicts the entire loop response from the error amplifier output to its input.

The desired characteristic of overall loop including its zero dB crossover frequency can be shown in a Bode plot, as in Fig. 32. The E/A compensation network will include two zeros near the output filter break frequency to cancel these two poles. Assume for now that the high frequency pole of this circuitry will be around or above the overall zero dB crossover point. The required error amplifier response can now be approximated graphically from the curve and points plotted.

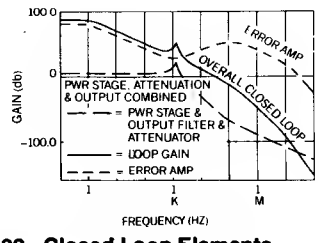

Figure 32 - Closed Loop Elements

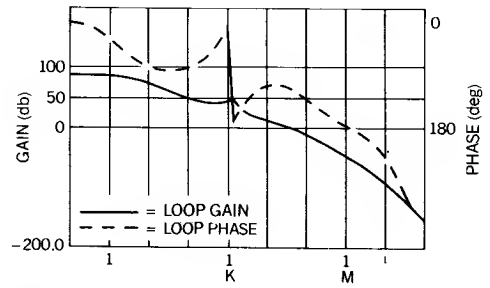

Figure 33 - Loop Gain and Phese

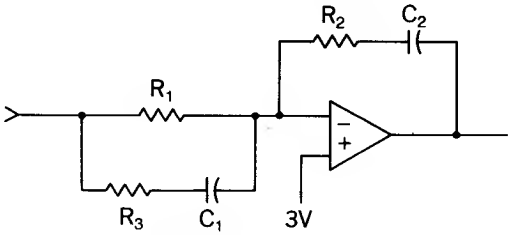

Figure 34 - E/A Compensation Newtork

In this example, two zeros will be introduced in the error amplifier response near the output filter break frequency of 1.25 kHz. A pole is located near the zero dB crossover point at 50 kilohertz. The actual gain and phase obtained in the overall loop is given in Fig. 33

The error amplifier with its compensation network is shown in Fig. 34. It provides high gain at low frequencies and good transient response.

Zero 1:1 ($2\pi R_1C_1$)
Zero 2: $1/(2\pi R_2C_2)$
Pole 1: $1/(2\pi R_3C_1)$
Max Gain: $R_2/(R_1$ & R_3 in parallel)

Input impedance is the parallel combination of R_1, R_2,and R_3

The compensation network is designed to produce:

Zero 1 and Zero 2 at 1.24 kHz

Pole 1 at 70 KHz

> 55 dB loop gain at 50 kHz

Using the previous equations and solving:

R_1 = 6.03K R_2 = 78.1K R3 = 100Ω

C_1 = 22 nF C_2 = 1.7 nF

From the Bode plot of the closed loop response, the supply is compensated to cross 0 dB at approximately 35 kHz, with ample phase margin.

Power Supply Performance

This 150 watt power supply was evaluated while being exercised over various line and load conditions, and exhibited excellent regulation. Response to dynamic loading was well within reasonable limits with little overshoot. Short circuit input current is extremely low, due to the programmed restart delay time constant of 50 milliseconds and soft start of 5 milliseconds.

High efficiency (above 80%) is achieved over the operating ranges. This is quite respectable for a high frequency, off-line power supply. The power stage was constructed on a double sided printed circuit board used for a precious high frequency example (1.5 MHZ current mode) in 1986.

The control circuit is constructed on the Unitrode UC3860 development PC board. The utilization of a ground plane precedes all circuit layout in megaHertz switch mode power designs, and is incorporated here. Coaxial cable interconnects the gate drive, current sense and output voltage signals between the control and power boards. Observation of the circuit waveforms requires the use of a UHF type scope probe socket, or chassis socket. Any length of ground or hook-up wire will distort the true waveforms.

Summary

Above several hundred kiloHertz, the square wave converter may not be optimal for off line designs. Losses associated with switching high voltages at high currents substantially reduce efficiency, power design and generate much EMI. The need for an alternative solution have resulted in various resonant and quasi-resonant approaches, each witih a unique set of merits, applications and control circuit requirements.

The UC3860 controller has integrated the numerous specific functions and "building blocks" required for resonant and quasi-resonant topologies. Configuration for fixed on-time, variable frequency operation is straightforward, and other adaptations are easily made possible. The uncommitted comparator interfaces well with zero current type switching arrangements. Thye UC3860's high speed logic, high power outputs and fault protection circuitry combine for an ideal mix of brains, brawn and speed.

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M2 Winding Data

C1 Closing The Feedback Loop and Appendices

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W. Andreycak, "3 Megahertz Resonant Mode Control IC Regulates 150 Watt Off-Line Supply", *High Frequency Power Conference*, 1988.

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Resonant Circuits-"Rust Remover" and Appendix

The abrupt transition from conventional square wave conversion to a resonant or quasi-resonant approach can be softened by a review of certain fundamentals. Fig. A1 shows the sine and cosine waveforms along with the timing

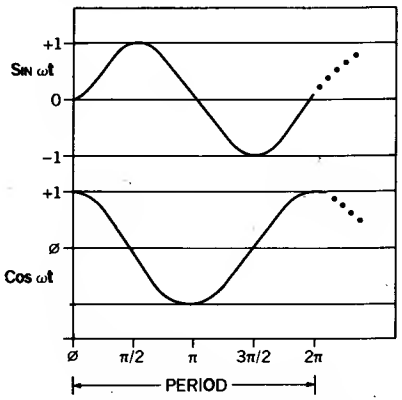
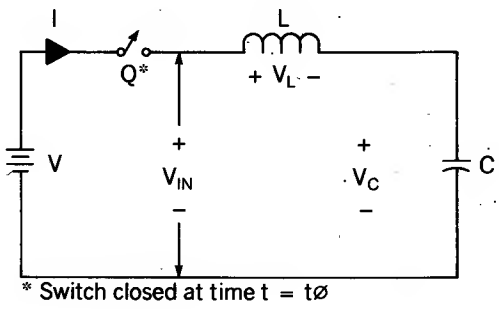


Figure A1 - Sine, Cosine Relationships relationships

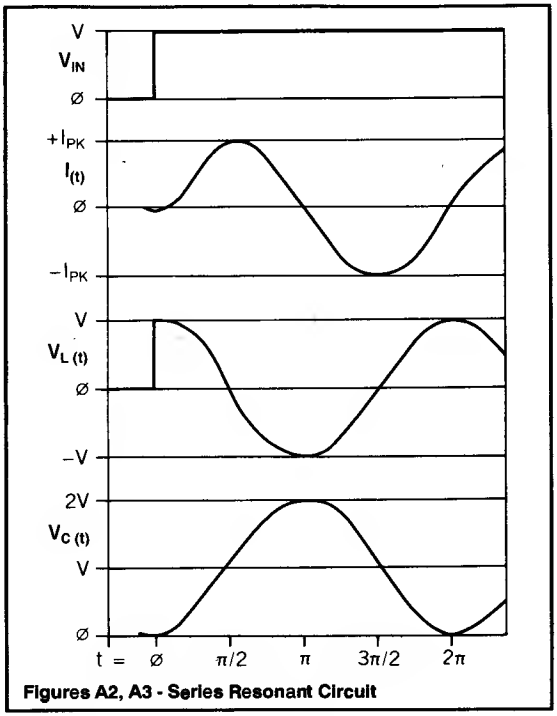


*** Switch closed at time t = t0**

Frequency = $\omega/2\pi$
$T_{period} = 1/f = 2\pi/\omega$

More specific to power conversion, a series resonant LC network driven by a DC voltage source is presented with its corresponding waveforms and equations in Figs. A2 and A3.

$\omega = 1/(LC)^{1/2}$, $Zr = (L/C)^{1/2}$
$i_{pk} = V_{IN} / Z_r$
$i = i_{pk} \sin(\omega t) = V_{IN} \sin(\omega t) / Zr$
$V_L = V_{IN} \cos(\omega t)$
$V_C = V_{IN}[1-\cos(\omega t)]$



Figures A2, A3 - Series Resonant Circuit

Resonant circuit timing relationships and waveforms: The waveforms of a series resonant, parallel loaded circuit will be analyzed in detail and used to generate the relationships between time, current, charge and energy transfer in a a resonant circuit application. Specifically, the buck topology will be used in this example, which can be applied to other topologies and configurations.

The cycle is initiated at time t_o Switch Q1 closes, delivering a rectangular voltage waveform to the resonant circuit. The input current rises linearly to I_{out} at a slope equal to V_{IN}/L_r. It reaches the constant output current level I_{out} at time t_1. The time for this to occur is $\Delta 10 = (t_1-t_0)$. During this interval, all resonant inductor current is directed to the output and none delivered to the resonant capacitor, C_r.

At t_o:

$i_{in} = 0$, $i_{cr} = 0$, $v_{cr} = 0$

From t_o to t_1,

$i_{in} = V_{IN} t / L_r$

At t_1, $i_{in} = I_{out}$

$\Delta t_{10} = L_r I_{out} / V_{IN}$

At time t_1, the input current equals the fixed current I_{out}. The resonant L_r & C_r tank components begin their resonant cycle at zero current, and the input current rises sinusoidally to its peak of $I_{out} + V_{IN}/Z_r$, It will later intersect the output current I_{out} again at time t_2 corresponding to 1/2 the resonant tank period, π radians.

At t_1:

$I_{in} = I_{out}$, $i_{cr} = 0$, $v_{cr} = 0$

From t_1 to t_2:

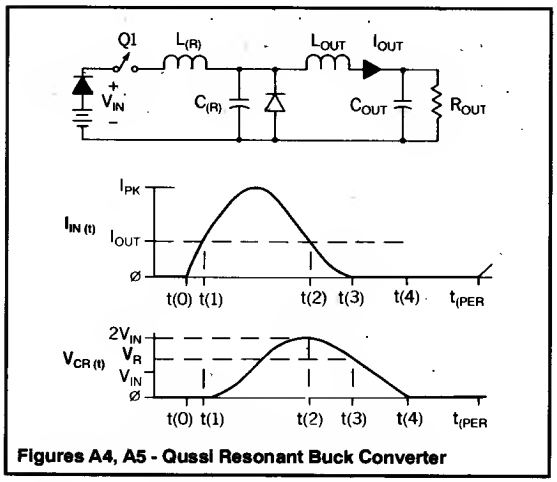
$i_{in} = I_{out} + (V_{IN}/Z_r)\sin\omega(t-t_1)$

$\Delta t_{21} = \omega/\pi = 1/(2f) = 1/\pi(L_rC_r)^{1/2}$

$$i_{cr} = \frac{V_{IN}}{Z_r} \sin \omega(t-t_1)$$

$V_{cr} = V_{IN}(1-\cos\omega(t-t_1))$

Once the input (inductor) current crosses I_{out} at time t_2 it continues sinusoidally until it reaches zero at time t_3. At th is point, switch Q_1 is turned off to facilitate zero current switching. The time required to reach zero current from I_{out} is Δ32, and depends upon the amplitude of I_{out} and V_{IN}.



Figures A4, A5 - Qussi Resonant Buck Converter

At t_2:

$i_{in} = I_{out}$, $i_r = 0$, $v_{cr} = 2V_{in}$

From t_2 to t_3:

$$\Delta t_{32} = \frac{1}{\omega} \sin^{-1}\left[\frac{I_{out}Z_r}{V_{in}}\right]$$

$$i_{in} = I_{out} + \frac{V_{IN}}{Z_r} \sin \omega(t-t_1)$$

$V_{cr} = V_{IN}(1-\cos\omega(t-t_1))$

The resonant capacitor voltage v_{Cr} discharges linearly during the interval of Δt43, beginning at time t_3. The capacitor voltage and Δt43 are determined from the following equations:

At t_3:

$i_{in} = 0$, $i_{cr} = 0$

From t_3 to t_4:

$v_{cr} = v_{cr(t3)} - I_{out}(t - t_3)/C_r$

$\Delta t_{43} = C_r v_{c(t3)} / I_{out}$

Evident from the previous equations is the need to vary the output on time to respond to the various line, load and resonant tank circuit influences.

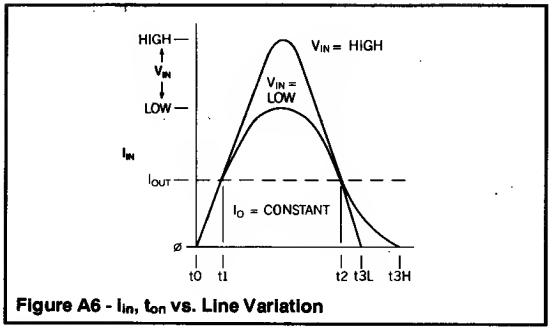


Figure A6 - I_{in}, t_{on} vs. Line Variation

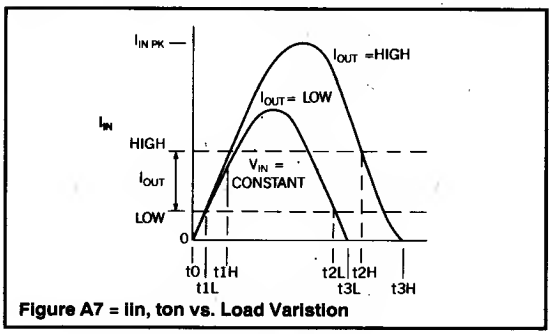


Figure A7 = Iin, ton vs. Load Variation

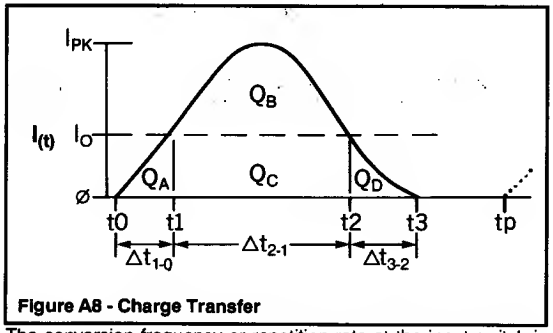


Figure A8 - Charge Transfer

The conversion frequency or repetition rate at the input switch is approximated following some intermediate calculations for total energy transfer from input to output, as follows:

Charge Transfer in the Resonant Circuit

During each resonant cycle a specific amount of charge (Q) is taken from the input supply and transferred to the output load. The corresponding energy (watt-sec) transferred is simply the charge (Q) multiplied by the input voltage V_{IN}. This relationship will be used to approximate the conversion frequencies required to regulate an output voltage for various ranges of input voltages and output currents.

The input current waveform will be divided into four specific intervals to simplify the calculations. The charge transferred in each interval will be calculated by integrating the current waveform throughout the interval.

Qa. The charge transferred during the time interval from to t_o t_1 is

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calculated from the equation for the area of the triangle formed:

$\Delta t_{1\text{-}0} = L I_o / V_{IN}$

Qa: $= \Delta t_{1\text{-}0} I_o / 2 = L I_{out}^2 / (2 V_{IN})$

Qb: During this resonant half-period, the sinusoidal portion of the input current waveform is integrated over the interval t_1 to t_2.

$I_{in} - I_{out} = (V_{IN} / Z_r) \sin \omega(t\text{-}t_1)$

$$Q_b = \frac{V_{IN}}{Z_r} \int_{t1}^{t2} \sin(\omega(t-t_1))dt$$

$$Q_b = \frac{V_{IN}}{Z_r} \omega \left[-\cos\theta \right]_0^{\pi}$$

$1/ Zr\omega = C_r$

$\therefore Qb = 2VIN\ Cr$

Qc: The rectangular area of charge delivered to the output during interval t_1 to t_2 is:

$Qc = I_{out} \Delta t2_1$, where $\Delta\tau 2_1 = \pi/\omega$

$Qc = \pi I_{out} / \omega$

Qd: The sinusoidal current decreases from I_{out} to zero during the t_2 and t_3 interval. The charge transferred is calculated by subtracting the sinusoidal component from the rectangular region formed by I_{out} and t_3.

$$Qd = I_{out} \Delta t_{32} + I_r \int_{t2}^{t3} \sin(\omega(t-t_1))dt$$

$$Qd = I_{out} \Delta t32 - \frac{V_{IN}}{Z_n \omega} \left[\cos\theta \right]_{\pi}^{\pi + \omega \Delta t32}$$

$$Qd = I_{out} \Delta t_{32} - V_{IN} C_r \left[\cos(\pi + \omega \Delta t_{32}) - \cos\pi \right]$$

$$\Delta t_{32} = (1/\omega) \sin^{-1}(I_{out} Z_n / V_{IN})$$

For practical purposes, this area can be repesented by a linear approximation without a significant compromise in accuracy. The area formed by $I_{out}\Delta t_{32}/2$ is a reasonable estimate of the area, resulting in approximately 1% error in the total charge transferred.

$Qd \approx I_{out} \Delta t_{32}/2 = (1/2\omega) I_{out} \sin^{-1}(I_{out} Z_n / V_{IN})$

Qt: The total charge transferred from the input to the output per cycle is the summation of charges Qa through Qd.

$Qt = Qa + Qb + Qc + Qd$

$$Qt = \frac{L I_{out}^2}{2 V_{In}} + 2 V_{IN} C_r + \frac{\pi I_{out}}{\omega} + \frac{I_{out}}{2\omega} \sin^{-1} \frac{I_o Z_n}{V_{IN}}$$

The approximation made to simplify the calculation of charge Qd also allows the substitution of charge Qa for Qd, thus reducing the total charge transfer to the following.

$Qt = 2Qa + Qb + Qc$

$$Q_t = \frac{L I_{out}^2}{V_{IN}} + 2 V_{IN} C_r + \frac{\pi I_{out}}{\omega}$$

Energy Transfer During the Resonant Cycle

The energy per oycle, W, can be calculated by multiplying the input voltage V_{IN} by the total charge Qt transferred from the input to the output. Dividing the energy per cycle W by the output power P_{out} unveils the conversion period - the inverse of the switching frequency.

$$T_{conv} = \frac{W/cycle}{P_{out}} = \frac{V_{IN} Q_t}{V_{out} I_{out}}$$

$$= \frac{V_{IN}}{V_{out} I_{out}} (Qa + Qb + Qc + Qd)$$

$$= \frac{V_{IN}}{V_{out} I_{out}} (2Qa + Qb + Qc)$$

$$T_{conv} = \frac{V_{IN}}{V_{out} I_{out}} \left[\frac{L_r I_{out}^2}{V_{IN}} + 2 V_{IN} C_r + \frac{\pi I_{out}}{\omega} \right]$$

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A NEW FAMILY OF INTEGRATED CIRCUITS CONTROLS RESONANT MODE POWER CONVERTERS

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ABSTRACT

A new family of integrated circuits is introduced. Devices from this family implement the necessary architecture to control a broad range of resonant mode converters. Key features in the areas of switch timing, fault management, and soft-start technique are unique to this family. Individual devices are customized to handle off-line or DC to DC, single-ended or dual-switch, zero-voltage-or-current-switched configurations. Specific application to three different resonant mode converters is mentioned.

SURVEY OF EXISTING CONTROL INTEGRATED CIRCUITS

Since 1986, interest in resonant mode power conversion has exploded in the technical conferences. IC makers have been quick to respond with offerings of control ICs. Table 1 is a list of chips available at the present time. To simplify thinking, the first three parts listed are essentially the same design as are the last two. There are significant differences in features and performance levels between the three groups. However, a common operational philosophy is shared by all: fixed-pulse-width variable-frequency. This approach has been applied to zero-current-switched (ZCS), quasi-resonant mode converters with reported success.

Table 1. List of Resonant Mode Control ICs

LD405
GP605
CS3805
- - - - - -
UC3860
- - - - - -
MC34066
CS360

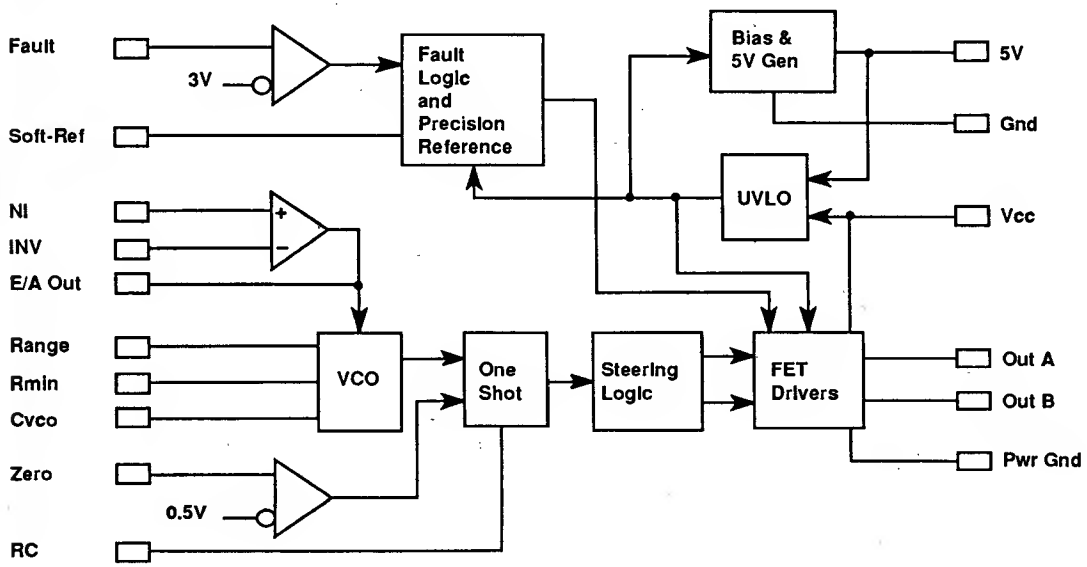

Figure 1. Controller Block Diagram

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NEW FAMILY OF RESONANT MODE CONTROL INTEGRATED CIRCUITS

As the discipline is maturing, the advantage of some feature changes has become apparent. Versatility to control both ZCS and zero-voltage-switched (ZVS) converters is needed. The ability to control proper switch times (on or off) with changing line, load, or component values is needed. To address these needs, a family of controllers based on a common silicon die has been developed. Three members of the family, the UC1861, UC1864, and UC1865 will be covered in detail.

The common block diagram of the family is illustrated in figure 1. These parts feature an error amplifier (E/A), voltage controlled oscillator (VCO), one shot timing generator with a zero wave-crossing detection comparator, steering logic to two output drivers, a 5V bias generator, and under voltage lockout (UVLO). A latched fault management scheme provides soft start, restart delay, and a precision reference.

Die options can be produced that give different UVLO levels, as well as different output properties. There are two UVLO options. The first, suited for off-line operation has thresholds of 16 and 10V. While UVLO is active, Icc is less than 0.3mA. The other option is 8 and 7V, to accommodate lower input voltage DC/DC converters.

The flavor of the outputs required by different resonant mode topologies requires the steering logic to be configured specially for each application. The basic options that can be built allow for single or dual switch drive, and controlled on or off times. Zero-current-switching applications require controlled switch on times while zero-voltage-switching applications require controlled switch off times. Figure 2 shows these options.

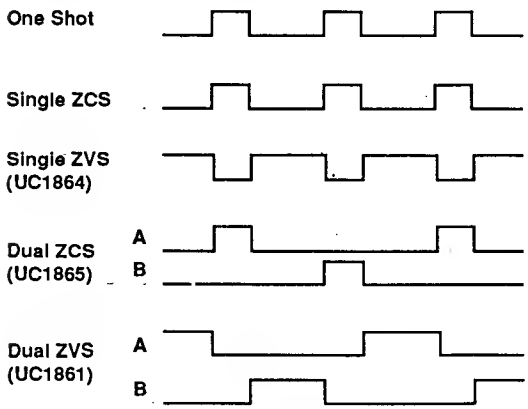

Figure 2. Output Drive For Different Converters

Table 2 details the options implemented in the 1861, '64, and '65. Other options can be built from the same die.

Table 2. Implemented Options in the 1861, '64, '65.

Device	UVLO Vth	Outputs	Zero-(?)-Switching
UC1861	16/10V	Dual	Voltage
UC1864	8/7V	Single	Voltage
UC1865	16/10V	Dual	Current

PRIMARY CONTROL BLOCKS

The fundamental control blocks essential for a majority of resonant mode converters are an error amplifier, VCO, one shot timing generator, and output stage to drive power mosfets.

ERROR AMP & VOLTAGE CONTROLLED OSCILLATOR

Figure 3 details the E/A and VCO. The E/A output directly controls the VCO via the Irange generator. The VCO has inputs for two resistors, R_{ange} and R_{min}, and one capacitor, C_{vco}. R_{min} and C_{vco} determine minimum frequency.

$$F_{min} = \frac{3.6}{(R_{min} * C_{vco})} \quad (1)$$

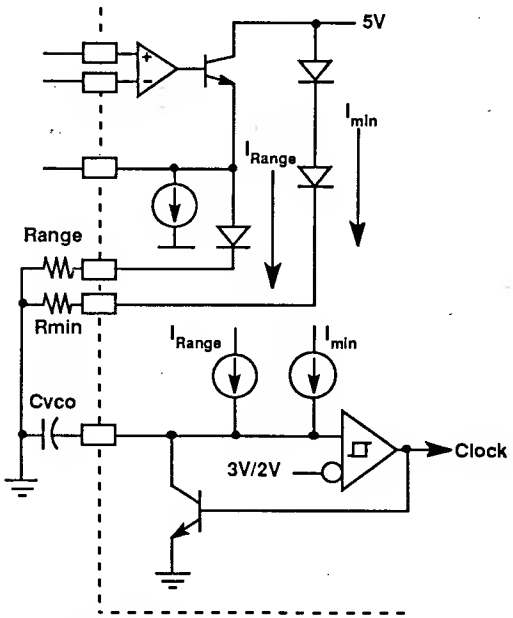

Figure 3. Error Amplifier and Voltage Controlled Oscillator

When the output of the E/A is less than or equal to one diode drop above ground, the VCO operates at minimum frequency. The E/A output can go as high as one diode drop below 5V. When at this potential, the VCO frequency is at its maximum.

$$F_{max} = \frac{3.6}{(R_{ange} \| R_{min}) * C_{vco}} \quad (2)$$

Usable maximum frequency tops out around 1.5MHz. The Frequency range is the difference in equations 2 and 1.

$$\Delta F = \frac{3.6}{R_{ange} * C_{vco}} \quad (3)$$

Since the nominal E/A output swing is approximately 3.6V for full variation in VCO frequency, the gain of the VCO block is

$$dF/dV = \frac{1}{R_{range} * C_{vco}} \quad (4)$$

In ZCS power supplies, an increase in frequency will correspond to an increase in the converter's output voltage. For these applications the E/A non-inverting input is connected to a reference voltage while the output voltage sense is fed back to the inverting input. For ZVS power supplies, a decrease in frequency corresponds to an increase in output voltage. For these systems, the inputs to the E/A are exchanged.

The common mode range of the E/A is from zero to 6V. This feature allows zero volts to be a valid reference voltage applied to the E/A. Soft start, covered later, takes advantage of this feature.

ONE SHOT TIMING REQUIREMENTS

The basic premise in resonant mode conversion is packets of energy delivered at varying repetition rates. Each energy packet dictates a basic switch on or off time, hence the one shot timer. In ZCS systems the switch is on. In ZVS systems the switch is off. The timer, then, should force the switch to conform to the resonant timing of the tank circuit. It is this conformance that achieves zero stress switching.

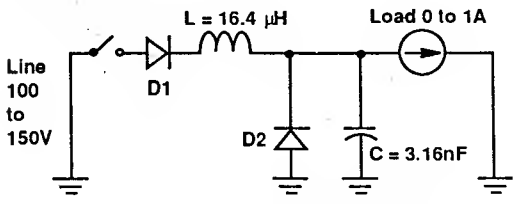

Figure 4. ZCS Resonant Tank Example

For purposes of convenience, a simplified ZCS resonant tank is presented to illustrate the timing requirements of resonant converters in general. This is an example, not a rigorous theoretical presentation. It does, however, demonstrate the problems to overcome in properly controlling a resonant mode converter. The circuit of figure 4 is designed to operate from line inputs of 100 to 150V and 0 to 1A load current. The tank frequency is arbitrarily selected to be 700kHz. A reasonable first guess for tank impedance is determined by

$$Z_o = \frac{V_{lowline}}{I_{max} * 1.386} \quad (5)$$

$$= 72 \text{ ohms.}$$

From the equations governing resonant tank natural frequency and impedance, L and C can be calculated.

$$F_o = \frac{1}{2\pi\sqrt{LC}} = 700\text{kHz} \quad (6)$$

$$Z_o = \sqrt{\frac{L}{C}} = 72 \text{ ohms} \quad (7)$$

$$L = \frac{Z_o}{2\pi F_o} = 16.4\ \mu\text{H} \quad (8)$$

$$C = \frac{1}{2\pi Z_o F_o} = 3.16\text{nF} \quad (9)$$

Figure 5 shows the pertinent current and voltage waveforms for the case of 125V input and 0.8A output. When the switch closes at zero time, the current starts to build linearly. Once the current reaches 0.8A, then load current is completely supplied through the inductor and D2 carries no current. At this point in time the L and C resonate together until inductor current returns to zero. At this time the switch is allowed to turn off, but it doesn't necessarily have to. D1 prevents reverse current in the switch. It isn't necessary to open the switch until the capacitor voltage decays to line voltage. It is acceptable to open the switch any time during this "switch window". If it is opened too soon, the circuit will suffer severe switching losses. If it is not opened, the tank will resume resonating, as shown by the dashed curves. If the switch is opened later than the switch window, not only will the circuit suffer switching losses, but the transfer function becomes overly complex.

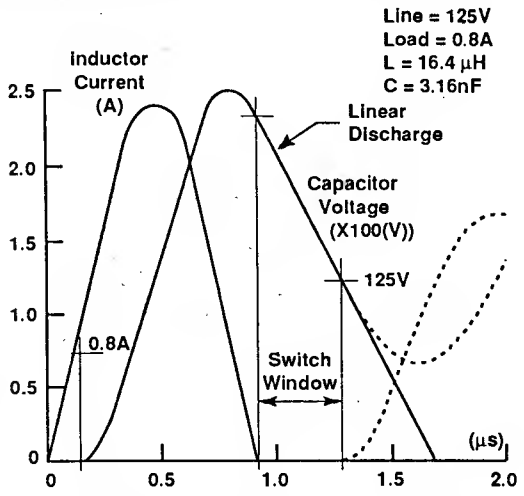

Figure 5. Typical Resonant Tank Waveforms

The graph in figure 6 plots the switch window as a function of load current for both high and low line voltage. For example, at a load current of 0.5A and high line, the switch must be closed for at least 0.80us and need not be opened until 1.61us. Examination reveals the most stringent switch window, 1.03 to 1.21us, occurs at low line and full load. Furthermore, this window is a subset of all other windows. This might lead to choosing a fixed on-time of 1.12us under the assumption that it is relatively easy to build a fixed time one-shot circuit with total variations less than +/-8%. However, further consideration will lead to a different conclusion.

In order to insure that the example in question can be produced; the variations of the resonant components and the possibility of output overload must also be examined. This example continues by assuming total variations for the capacitor are under 10% while under 20% for the inductor. A 20% overload is also allowed.

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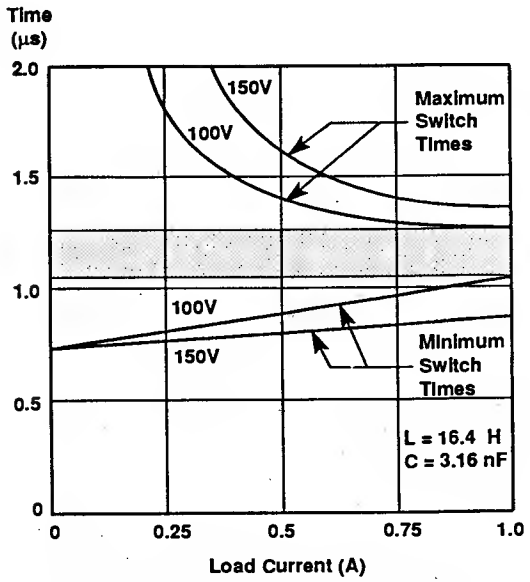

Figure 6. Minimum/Maximum Switch Time vs Load Current

Figure 7 shows the valid switch windows at 1.2A and 100V for nominal component values as well as the four tolerance corners. Several observations can be made. Firstly, the window for the case of +20% inductor and -10% capacitor variations has zero tolerance.

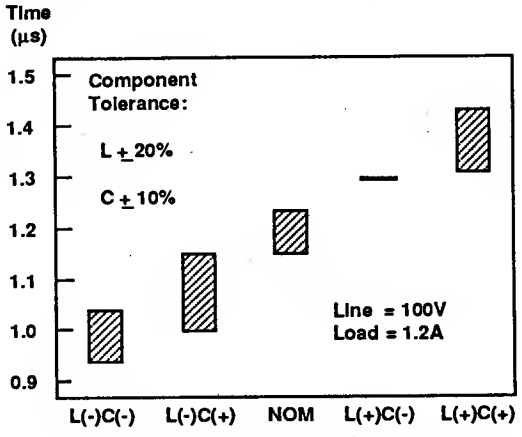

Figure 7. Switch Window vs Component Value

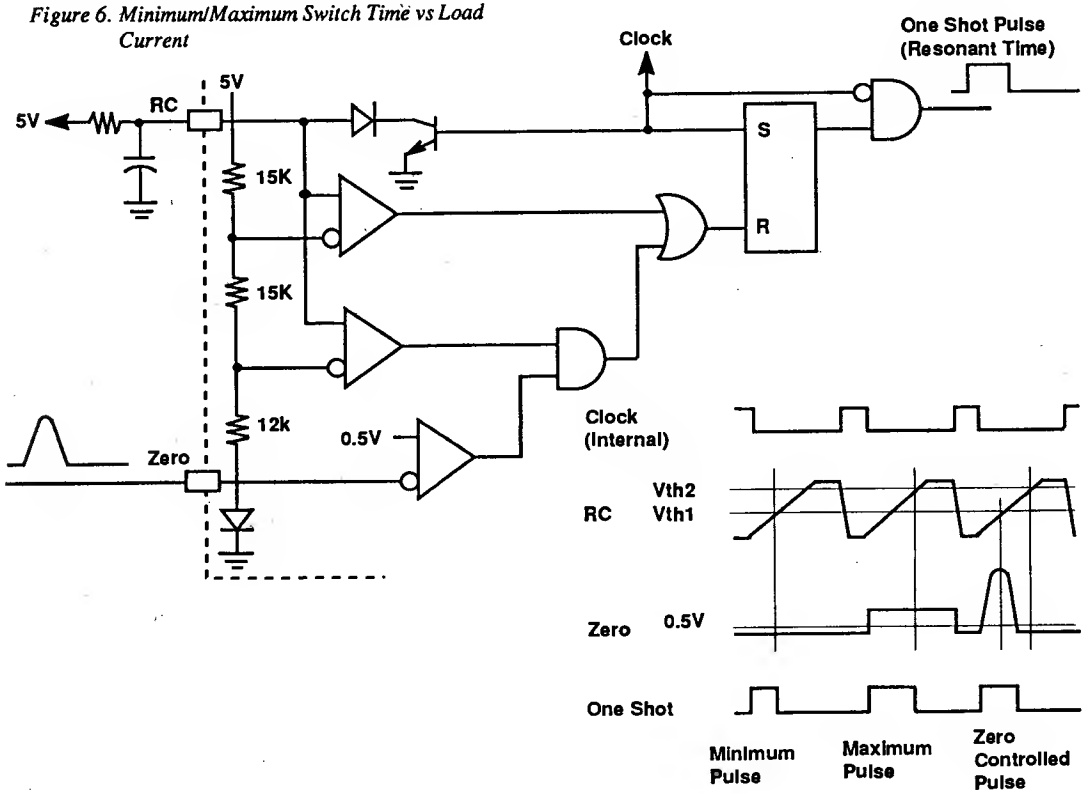

Figure 8. One Shot Timer.

The switch must turn off at 1.30us. This is because the tank impedance is exactly the ratio of low line voltage to overload current for these component values. This is the source of the 1.386 factor in equation 5. Secondly, and the point of the illustration, there is no possible value of fixed switch time that accommodates component variation.

ONE SHOT TIMING GENERATOR

In figure 8, details of the one shot timer are secn. The clock signal from the VCO sets the latch, blanks the output, and causes the RC timing pin to be discharged. The timing pin determines the minimum and maximum times the one shot output will be high.

$$T_{max} = R * C \quad (10)$$

$$T_{min} = 0.3 * T_{max} \quad (11)$$

Between these two limits, the zero detect comparator will terminate the one shot pulse whenever the Zero pin goes below 0.5V. By sensing the zero crossing of the resonant waveform, the one shot adapts to different resonant component values and varying line/load conditions. The switch time will properly track the resonant tank assuring zero stress switching.

STEERING LOGIC & OUTPUT STAGE

Figures 9, 10, and 11, are block diagrams of the steering logic and output stages. Each output stage is a totem pole driver optimized for driving power mosfet gates. Gate currents of 1A can be obtained from each driver. Note the 1864 single driver is actually both drivers on the chip paralleled. Sample waveforms for the three configurations were shown in figure 2.

Fault and UVLO response of the three configurations is identical. These indications always force both drivers to the low state. During UVLO, the outputs can easily sink 20mA irrespective of Vcc.

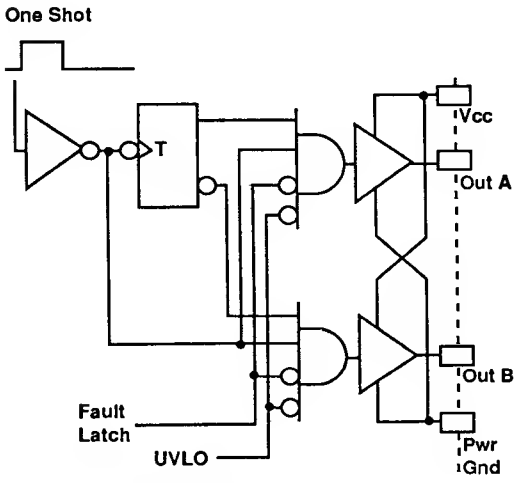

Figure 9. UC1861 Steering Logic

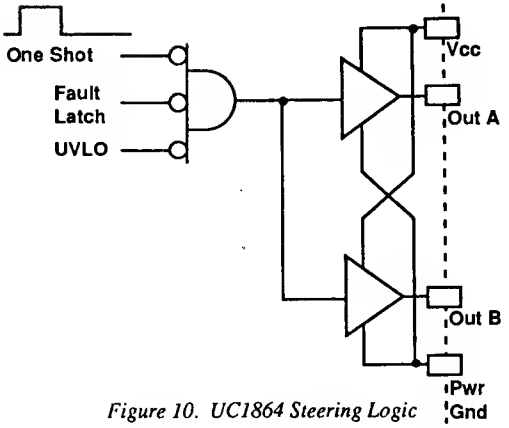

Figure 10. UC1864 Steering Logic

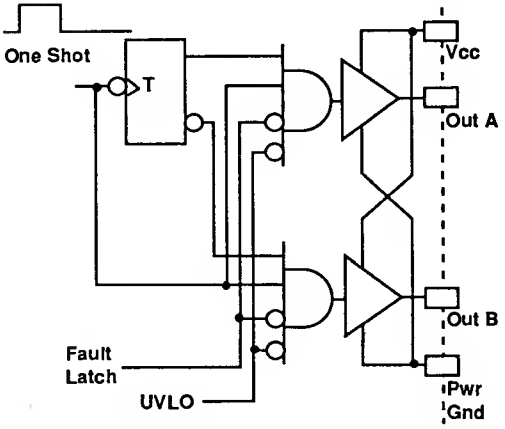

Figure 11. UC1865 Steering Logic

SECONDARY BLOCKS

The secondary blocks on board are UVLO, a 5V bias generator, and fault management with a precision reference. The purpose of the 5V generator is to provide a stable bias environment for internal circuits and up to 10mA of current for external loads. The one shot timing resistor connects to 5V.

UVLO senses both Vcc and 5V. It doesn't allow operation of the chip until both are above preset values. When Vcc is below the UVLO threshold, the 5V generator is off, the outputs are actively pulled low, the fault latch is set, and supply current is less than 300uA.

SOFT START, RESTART DELAY, PRECISION REFERENCE

A novel combination fault management and precision reference is shown in figure 12. One pin is dedicated to a fault sense comparator with a 3V threshold. A second pin does triple duty providing soft start, restart delay, and precision system reference. UVLO initializes the latches, forcing the chip output(s) to be low and the Soft-Ref pin to be discharged. After UVLO, Soft-Ref is charged by an internal 0.5mA current source until is it clamped at

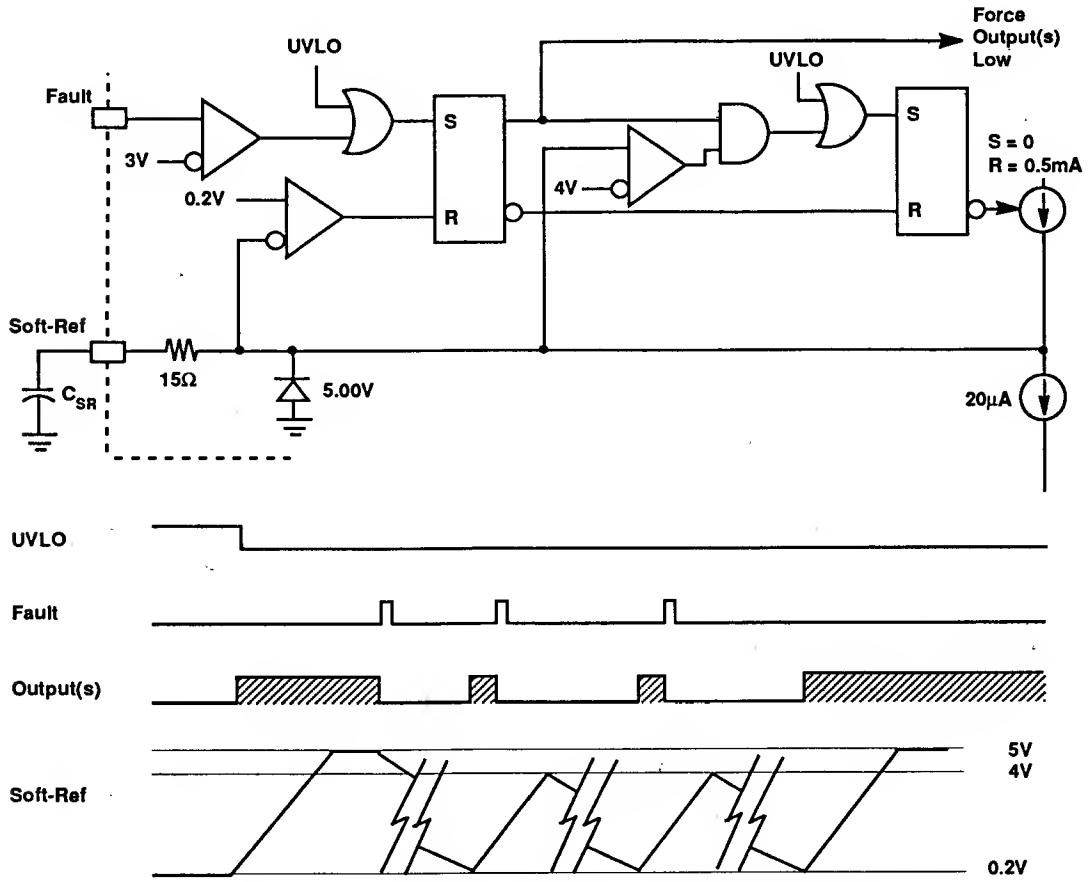

Figure 12. Fault Comparator, Soft Start, Restart Delay And Precision Reference

5V. The soft start time is approximately given by:

$$T_{softstart} = C_{sr} * 10kohms. \quad (12)$$

The recognition of a fault causes the outputs to be driven low and the Soft-Ref pin to be discharged with a 20uA current source. This is the restart delay period. When Soft-Ref reaches 0.2V, the outputs are enabled and the pin is recharged by the 0.5mA current. If a fault should occur before completion of the charge cycle, the outputs are immediately driven low, but the Soft-Ref pin is charged to 4 Volts before the 20uA restart delay current discharges the pin. The restart delay time during continuous fault operation is:

$$T_{restart} = C_{sr} * 190kohms. \quad (13)$$

The ratio of restart delay to soft start is 19:1. If shorter restart delay times are desired, a resistor of 20k or larger can be added from Soft-Ref to ground. The timing equations then become:

$$T_{softstart} = R_{sr} * C_{sr} * \ln\left(\frac{(0.48mA * Rsr) - 0.2}{(0.48mA * Rsr) - 5}\right) \quad (14)$$

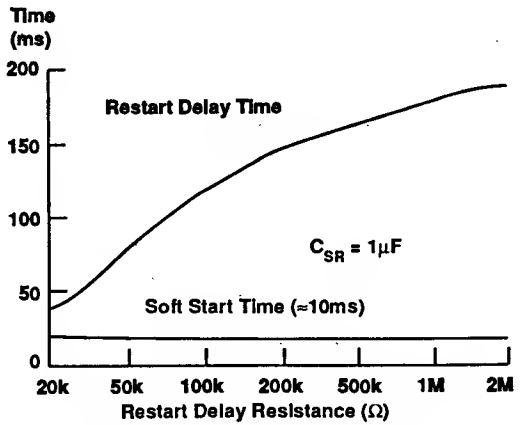

Figure 13. Soft Start And Restart Delay Times

$$T_{restart} = R_{sr} * C_{sr} * \ln\left(\frac{(20uA * Rsr) + 4}{(20uA * Rsr) + 0.2}\right) \quad (15)$$

Soft and restart times are plotted in figure 13 for C_{sr} = 1uF.

The restart feature can be defeated by the addition of a 100k resistor from Soft-Ref to 5V. In this configuration, a fault detection will permanently shut down the converter until either Vcc is recycled and UVLO resets the fault circuit, the 100k resistor is opened, or Soft-Ref is externally pulled to ground. The soft start time becomes:

$$T_{softstart} = C_{sr} * 9.2kohm. \quad (16)$$

The Soft-Ref pin is the system reference pin. By ramping the reference from zero during soft start, the converter output will follow the ramp up under closed loop control. This technique allows controlled starts for both ZCS and ZVS systems with no significant overshoot.

The reference characteristic of the Soft-Ref pin is due to a trimmed 5V zener-type clamp circuit. Fifteen ohms resistance separates the Soft-Ref pin from the clamp to eliminate zener oscillations for any external capacitance value. The clamp zener is designed to tolerate loading of +/- 200uA without degradation of reference accuracy. Loading, however, will alter the soft start and restart delay times, and could even preclude restart delay action unless care is taken in the design.

DC/DC ZVS SINGLE ENDED FORWARD CONVERTER APPLICATION

A ZVS multi-resonant forward converter based on previously reported (ref. 4) work is shown in figure 14. An 1864 is used to control the converter. A 22k resistor from the input line is used to start the circuit, which boot-straps power from the output to the chip after start-up. Before start-up, the chip draws less than 300uA and starts operating when Vcc reaches 8V. After start-up, the 22k resistor dissipates 70mW.

The switch voltage, V_s is sampled with a 100k/5.1k divider network. The chip anticipates zero crossing when V_s = 10V. In this power converter, switch voltages of 200 to 300V are to be expected. A pnp is used to clamp the zero voltage, Vz to prevent damage to the chip. The 100k resistor represents an insignificant load to the resonant circuit.

The paralleled outputs are connected, as good practice dictates, to the mosfet gate with a small-valued resistor. A schottky diode parallels the output pins to protect the chip from negative voltage spikes that might result from parasitic ringing in the gate circuit.

This power stage was demonstrated to have excellent short circuit tolerance when the minimum switching frequency is well controlled. For this reason, the fault input is not used.

Sensed output voltage is scaled & presented to the non-inverting pin of the E/A. The inverting input is DC referenced to the Soft-Ref

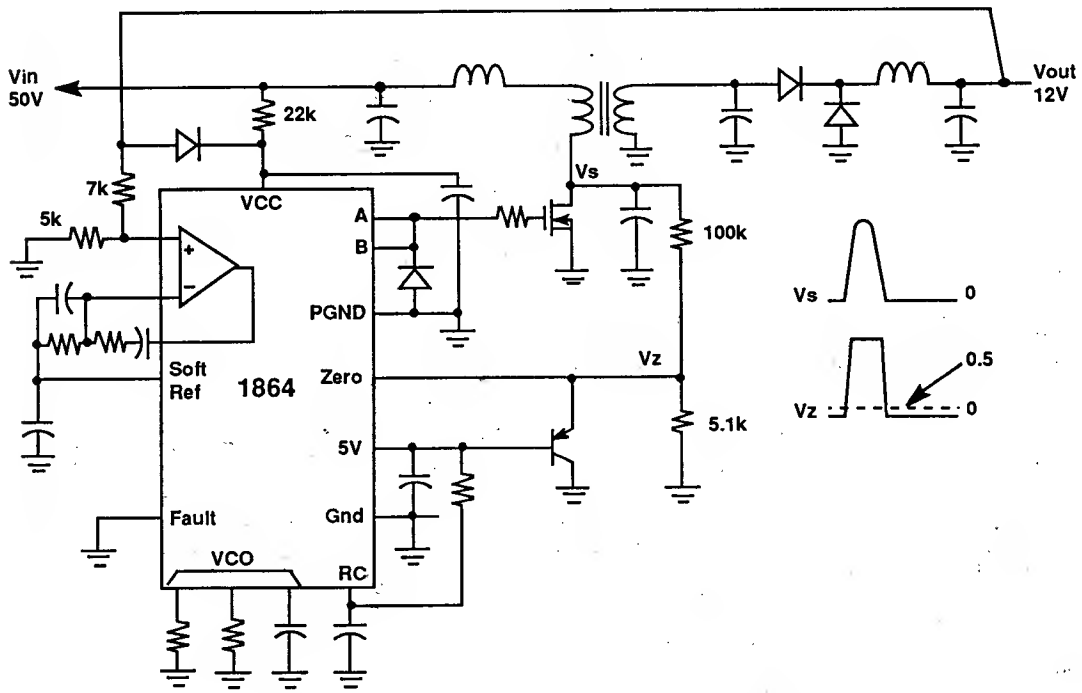

Figure 14. ZVS-MR Forward Converter Controlled By UC1864.

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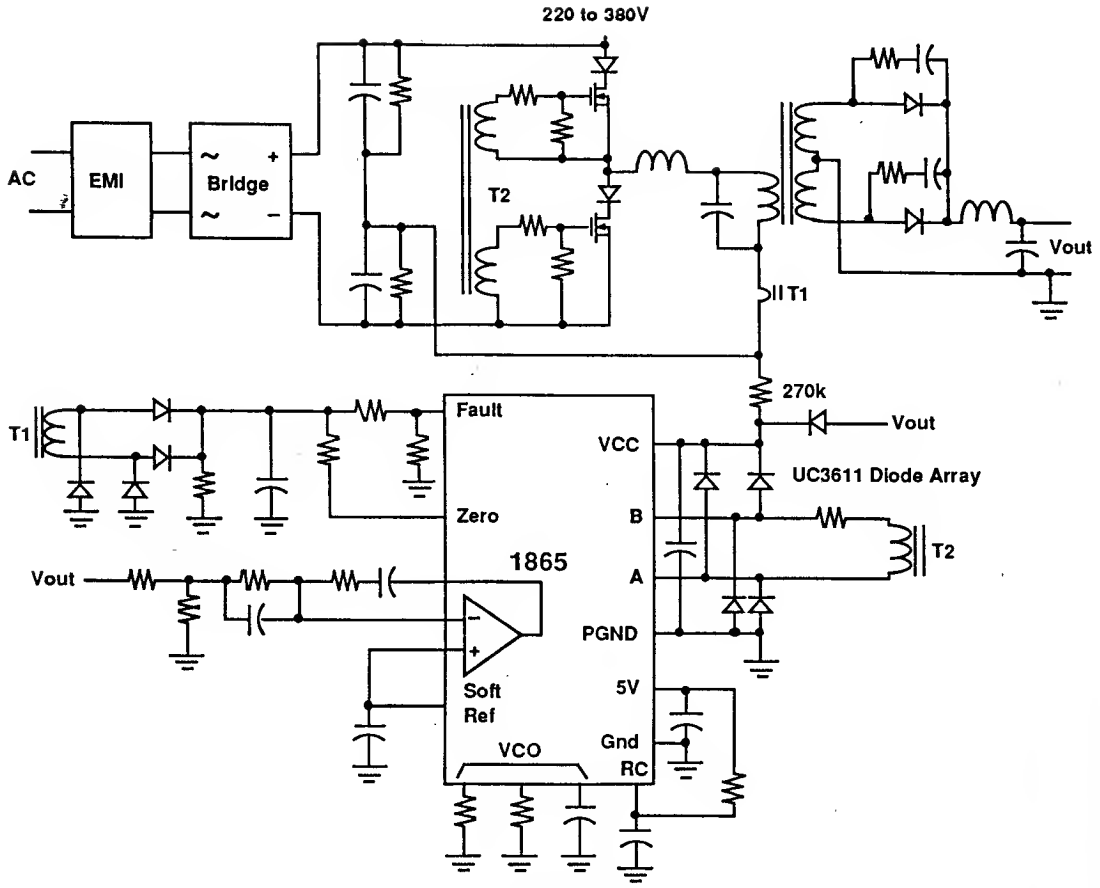

Figure 15. ZCS Off-Line Half-Bridge Converter With UC1865

pin, 5V. The compensation network shown represents zero DC load to the Soft-Ref pin. As long as C_{sr} is much larger than the feedback capacitor, then soft start behavior will be essentially as described in equation 12.

OFF-LINE ZCS HALF-BRIDGE CONVERTER APPLICATION

A ZCS off-line half-bridge converter (ref. 1) with an 1865 control IC is shown in figure 15. Irrelevant details in the converter have been simplified. The wide UVLO hysteresis and low start current of the chip have been used in start-up. A single resistor from the high voltage bus is used to start the circuit which then sustains itself from output voltage.

This circuit samples resonant current with transformer T1. Rectified secondary current, converted to an analog voltage, is applied to the fault and zero inputs of the 1865. Excessive current in the resonant tank will effect a shutdown and restart. The resistor between current sense transformer and the zero pin is to limit

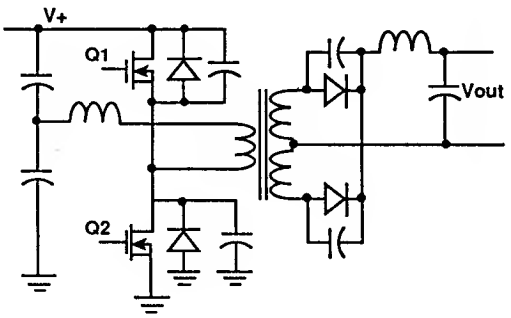

Figure 16. ZVS Half-Bridge Converter

current when the signal is at a high value. The allowable voltage range at the zero pin is zero to 9V, and resistive current limiting to less than 1mA is sufficient.

The half bridge power mosfets are transformer driven from the differentially connected output drivers of the 1865. A UC3611 schottky diode array has been used to prevent the outputs from being forced too far above Vcc or below ground.

The E/A non-inverting input is directly connected to the Soft-Ref pin to take advantage of all three features of the pin. This emphasizes the simplicity of application of the 1865 to this converter.

OFF-LINE ZVS HALF-BRIDGE CONVERTER APPLICATION

An off-line ZVS half-bridge converter (ref. 3) is shown in figure 16. An 1861 controls this converter in much the same manner as the two previous examples and is not shown here. The error amp configuration matches the ZVS example while the output stage is configured like the ZCS example.

This application does, however, present a difficulty in sensing zero voltage to control the one shot. In the first ZVS example, the voltage waveform was ground referenced and unipolar. The ZCS example had bipolar current, but a transformer and diode bridge conditioned the signal for the chip. In this example, zero switch voltage needs to be sensed for both Q1 and Q2. This poses no real problem for Q2. Q1 is another story. Some form of external circuitry must be employed to sense Q1 and translate the information to the ground referenced chip.

An easily implemented high voltage comparator circuit is shown in figure 17. The pnp and diode are the only high voltage components used. The circuit dissipates only 300mW. The output of this circuit is applied directly to the zero input of the 1861.

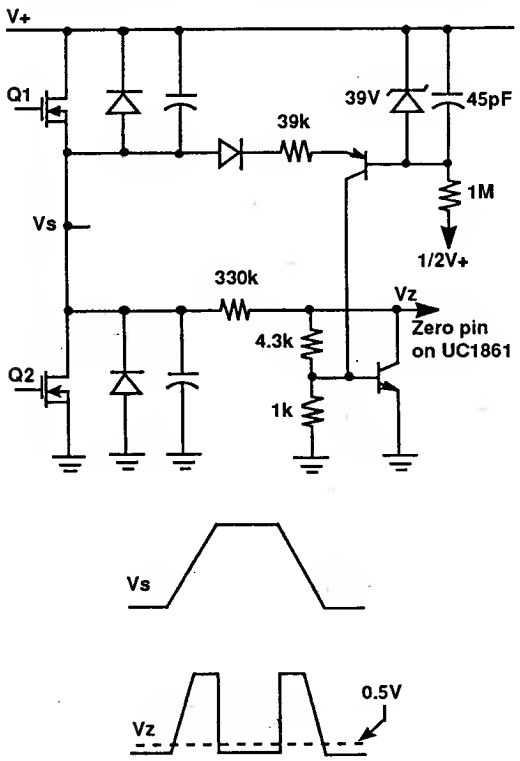

Figure 17. Zero Voltage Sensing Scheme For ZVS Half-Bridge Converter

CONCLUSION

A new family of integrated circuits to control resonant mode converters has been introduced that provides several improved features over those previously available. This family has parts that are suited not only to zero-current-switching, but also to zero-voltage-switching converters. The 1861, 1864, and 1865 are suited to off-line ZVS, DC/DC single ended ZVS, and off-line ZCS systems. Controllers for other specific converters can be built from this family. Adaptive control for resonant tank component variations as well as varying line and load conditions is inherent in the chip due to its zero crossing detect circuitry. A unique one pin approach to soft start, restart delay, and system reference provides adjustable restart delay to soft start time ratios as well as closed loop control during soft starts. Relative ease of application to three previously reported converters was discussed.

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CONTROLLING ZERO VOLTAGE SWITCHED POWER SUPPLIES

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ABSTRACT

Recent advancements in resonant and quasi–resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Today, the conventional approaches are by far, still in the production mainstream, however an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals awith a specific emphasis on the control IC requirements.

INTRODUCTION

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicised by others at various power conferences.[2,3] Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters.[4,5,6,7,8] In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its squarewave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the mosfet output capacitance (Coss) is discharged by the fet, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique. [9,10]

ZERO VOLTAGE SWITCHING OVERVIEW

Zero voltage switching can be considered as conventional square wave power conversion during the switch on-time with "resonant" switching transitions. Similar to constant off-time converters, the conversion frequency, or on-time is modulated in order to maintain regulation of the output voltage. For a given unit of time, this method is analagous to fixed frequency conversion which using an adjustable duty cycle. The foundation of this conversion is the volt-second product balancing of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the OFF-TIME of the ZVS converter's switch, the L-C tank circuit resonates. The voltage across the switch initially traverses linearly from "zero" to Vin, then resonantly to its peak, and back down again to zero. At this instant the switch can be reactivated, and lossless, zero voltage switching facilitated. Since the output capacitance of the mosfet switch (Coss) has been discharged by the resonant tank, it does not contribute as power lossin the switch. Therefore, the mosfet transition losses go to zero - regardless of operating frequency and

input voltage. This represents a significant savings in power, and results in a sustantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Furthermore, the technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback and boost converters, to name a few.

ZVS SWITCH WAVEFORMS

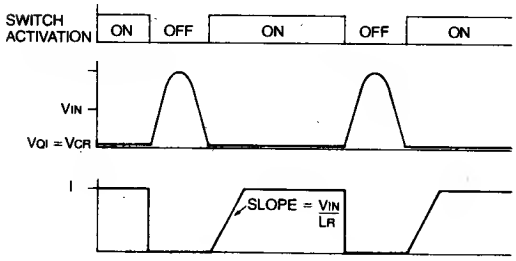

Figure 1.

ZVS BENEFITS

** Zero power "Lossless" switching transitions
** Reduced EMI / RFI at transitions
** No power loss due to discharging Coss
** No higher peak currents than square wave systems - unlike Zero Current Switching
** High efficiency with high voltage inputs - independant of conversion frequency
** Can incorporate parasitic circuit and component inductance and capacitance
** Reduced gate drive , no "Miller" effects
** Short circuit tolerant

ZVS DIFFERENCES

** Variable frequency operation (in general)
** Higher off-state voltages in single switch, unclamped topologies
** Relatively new technology (learning curve)
** Conversion frequency is inversely proportional to load current
** A more sophisticated control IC may be required

CONTROL CIRCUIT FUNDAMENTALS

Requirements for the Zero Voltage Switching generation of control ICs differ immensely from that of the more traditional pulse-width modulator. In fact, the two are direct opposites regarding the control circuit implementation in many respects, with similarities existing only amongst the housekeeping and gate drive attributes.

ERROR AMPLIFIER

The core of variable frequency operation focuses upon the error amplifier (E/A). The power supply output voltage (Vout) is sensed, compared to a reference input and the difference is amplified by the gain of the error amplifier. The resulting error voltage (Ve) signifys the need for the control circuit to respond to a change in the power supply's output voltage, typically caused by a line or load variation. This error voltage drives a voltage controlled oscillator (VCO) which decreases the conversion frequency with increasing error voltages, as required. An ideal amplifier should feature a high slew rate for fast transient response in addition to high gain-bandwidth for high frequency applications.

VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator needs to incorporate three programmable functions to satisfy the ZVS control circuit requirements; minimum conversion frequency, maximum conversion frequency and the voltage-to-frequency gain of the VCO. Programmability should request a minimal amount of external components for typical ranges in operating frequencies extenting into the megaHertz sector.

ONE-SHOT TIMER

The VCO output clocks the one-shot circuitry which generates the off-time for the ZVS switch. While a fixed off-time is generally associated with these ZVS converters, the "real" off-time can vary significantly. In most applications, a three-to-one variation in off-time is not uncommon, and necessary to accommodate the resonant components initial accuracies, temperature effects, line and load range combinations. A preferred approach is to program the maximum off-time at the one-shot and modulate it with a true zero voltage detection circuit. To state it quite simply, a fixed off-time control technique can NOT guarantee optimal zero voltage switching over all operating conditions.

ZERO VOLTAGE DETECTION

A zero crossing detection circuit is incorporated in the UC 1861/64 family of devices to implement "true" zero voltage switching. A precision threshold of 0.5 volts is compared to the ICs ZERO input, a representation of the switch drain-to-source voltage. When the falling edge of this waveform crosses the threshold, the ZERO detection comparator forces a change in the one-shot status, terminating its output. Numerous arrangements of external components provide the flexibility to adapt this feature to a wide range of ZVS switch topologies and applications. The drain-to-source voltage can be resistively scaled to the proper levels in high voltage applications, and offset above ground in low power usages.

PROTECTION CIRCUITRY

SOFT- START

Upon power-up the ZVS switch should start operation at the maximum conversion frequency, corresponding to the maximum switch off-time for an effective zero "duty" cycle. As the soft start circuitry lowers the conversion frequency the switch on-time starts at zero and gradually widens, increasing the effective duty cycle hence output power.

RESTART DELAY

Once a short circuit or overload on the power supply output has been detected, the IC controller needs to perform several functions. First, turn the output(s) off as quickly as possible (nanoseconds) to prevent a catastrophic failure of the supply. Second, the outputs should remain off for a programmed restart delay interval, one designed long enough to allow operation into a short circuit for extended periods of time (forever) without failing. Often called "Hiccup", this mode will subsequently restart the controller's output(s) in soft start under full fault protection once the restart delay period has concluded.

CLOSED LOOP START- UP

A preferred method to start or restart a power system is under full closed-loop control. The soft-rcf feature of the UC1861/64 controllers is intened to be used as the reference input to the error amplifier to facilitate closed loop start-up. Rather than simply clamping the output of the error amplifier as in a converntional PWM, this soft reference configuration controls the increasing power supply output voltage until regulation is attained. Additionally, only a single IC pin and one capacitor is used to provide both soft start and restart delay with user programmable fault management options.

UC 1861 / UC 1864 BLOCK DIAGRAM

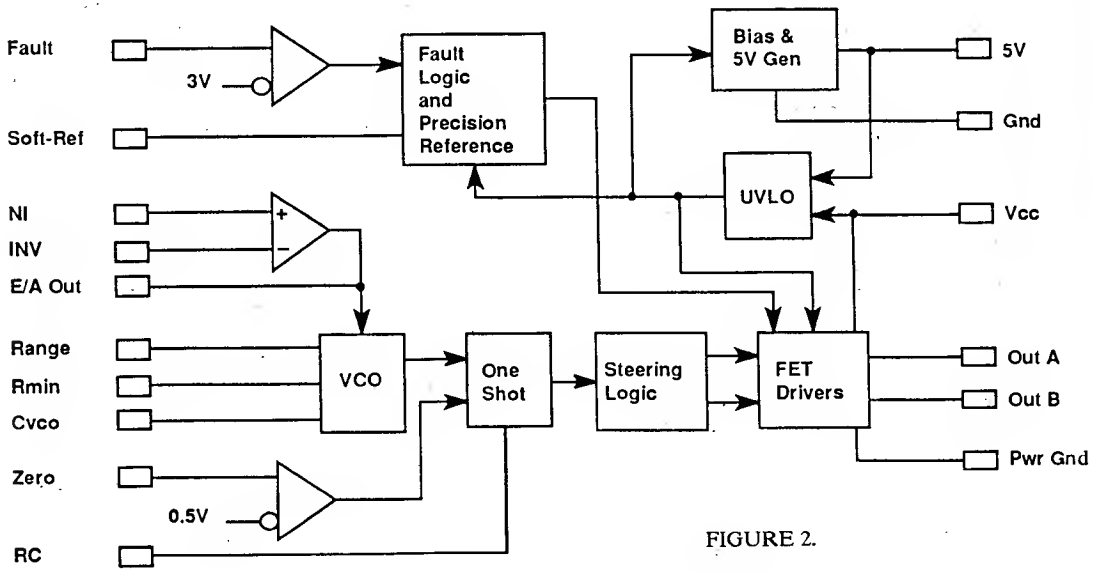

FIGURE 2.

ZVS - QRC FORWARD CONVERTER : DESIGN EXAMPLE AND PROCEDURE

TIMING INTERVALS AND DESIGN EQUATIONS

A zero voltage switched Forward converter will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevent polarities are shown in figure 3.

A valid assumption is that the output filter section consisting of output inductor (Lo) and capacitor (Co) has a time constant of several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value (Lr) and the magnetizing current (delta ILo) as well as the inductor's DC resistance is negligible. In addition, both the input voltage (Vin) and output voltage (Vo) are purely DC, and do not vary during a given conversion cycle. Additionally, the transformer is also ideal with a turns ratio of 1:1, thus allowing the simplification of this circuit to that of a Buck regulator. Last, the converter is operating in a stable, closed loop configuration which varies the conversion frequency in order to regulate the output voltage (Vo).

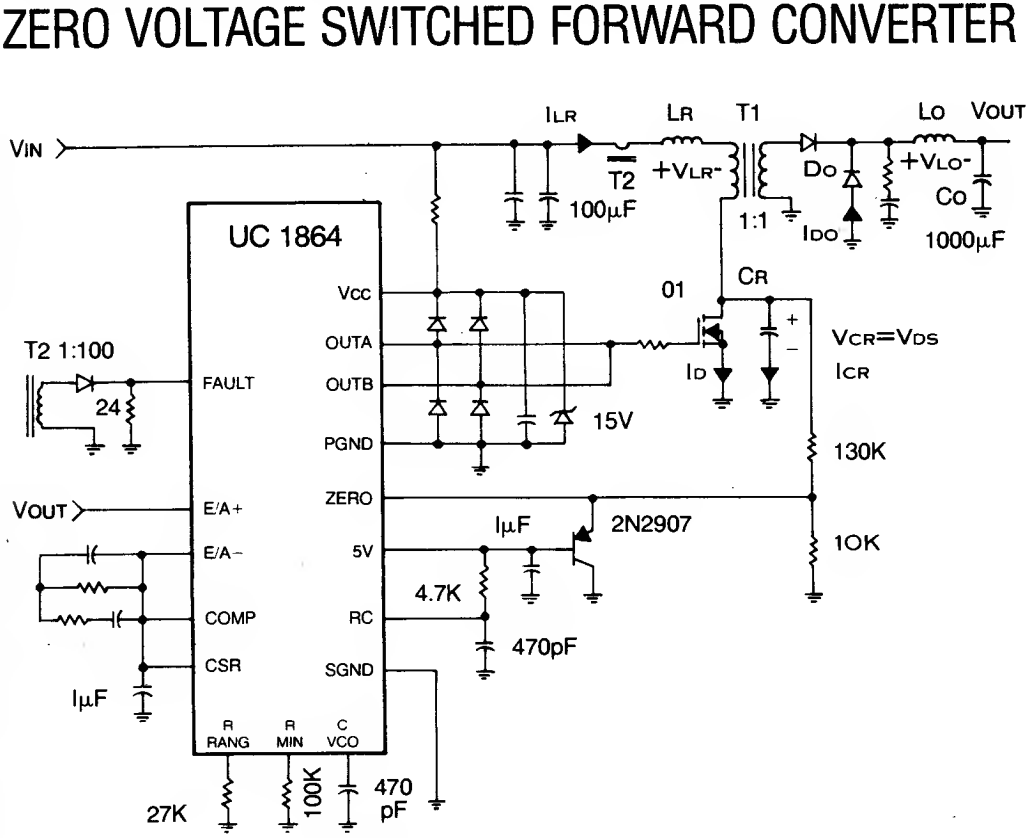

FIGURE 3. SCHEMATIC DIAGRAM

INITIAL CONDITIONS: t < t0

The analysis will begin with the switch (Q1) ON, conducting a drain current (Id) equal to the output current (Io), and Vds = VCr = 0 (ideal). In series with the switch (Q1) is the resonant inductor and the output inductor, also conducting the output current (Io). The voltage across the output inductor equals the input to output voltage differential; VLo = Vin - Vo. The output filter section catch diode is not conducting and sees a reverse voltage equal to the input voltage; VDo=Vi, observing the polarity shown in figure 3.

Q1 is ON , Vds = VCr = 0 ;
Id = ILr = ILo = Io
Do is OFF, VDo = Vin ; IDo = 0
ILr = Io ; VLr = 0
VLo = Vin - Vo; ILo = Io

CAPACITOR CHARGING STATE
Time interval: t0 < t < t1

The conversion period is initiated at time t0 when the switch is turned OFF. Since the current through the resonant inductor and output inductor cannot change instantaneously, and no drain current flows in Q1 while it is off, the current is diverted around the switch through the resonant capacitor. This constant output current of Io will linearly increase the voltage across the resonant capacitor until it reaches the input voltage (VCr = Vin). Since the current is not changing, neither is the voltage across the resonant inductor.

At time t0 the switch current "instantly" drops from Io to zero. Simultaneously, the resonant capacitor current snaps from zero to Io, while the resonant inductor current and output inductor current remains constant and equal also to Io over the duration of this span from t0 to t1. Voltage across the output inductor and output catch diode is linearly decreasing from time t0 to t1 due to the linearly increasing voltage across the resonant capacitor, Cr. This interval ends at time t1 when VCr equals Vin, and the output catch diode starts to conduct.

Q1 is OFF; Id=0; Vds(t)=VCr(t)
ICr(t)=Io; VCr(t)=[Io * t] / Cr
ILr(t)=Io; VLr=0
VDo(t) = Vin - [Io * t]/Cr
VLo(t0) = VDo - Vo

RESONANT STATE
Time interval: t1 < t < t2

The resonant portion of the conversion cycle begins at time t1 when the voltage across the resonant capacitor equals the input voltage, and the output catch diode begins conducting. Current through the resonant components at time t1 equals the output current.

The stimulus for this series resonant L-C circuit is output current flowing through the resonant inductor prior to time t1. The ensueing resonant tank current follows a cosine fuction beginning at time t1, and ending at time t2. At the natural resonant frequency (Wr), each of the L-C tank components exhibit an impedance equal to the tank impedance, Zr. Therefore, the peak capacitor voltage and peak OFF switch voltage is a function of the tank impedance and the load current.

Of great importance is the ability to solve the equations for the precise switch off-time which varies with line and load changes. While some allowance does exist for a fixed off time technique, the degree of latitude is insufficient to accommodate typical input and output variations.

The absolute maximum duration for this interval occurs when 270 degrees [(3/2) * Pi * Wr] of resonance is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line are approached.

Prior to time t1, the catch diode was not conducting. Its voltage was linearly decreasing from Vin at time t0 to zero at t1 while the input source was supplying full output current. At time t1, however, this situation changes as resonance is initiated, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage changes polarity as it conducts, supplementing the decreasing resonant inductor current with a diode current, extracted from stored energy in the output inductor. The diode current waveshape follows a cosine function during this interval, equalling Io minus ICr(t).

Vds(t)=VCr(t)=Vin+{Io*Zr*SIN[Wr(t-t1)]}
ILr(t)=ICr(t)=Io*COS[Wr(t-t1)]
VLr(t)=[Io*Zr*SIN[Wr(t-t1)]
IDo(t)=Io-ILr(t)

ZVS FORWARD WAVEFORMS

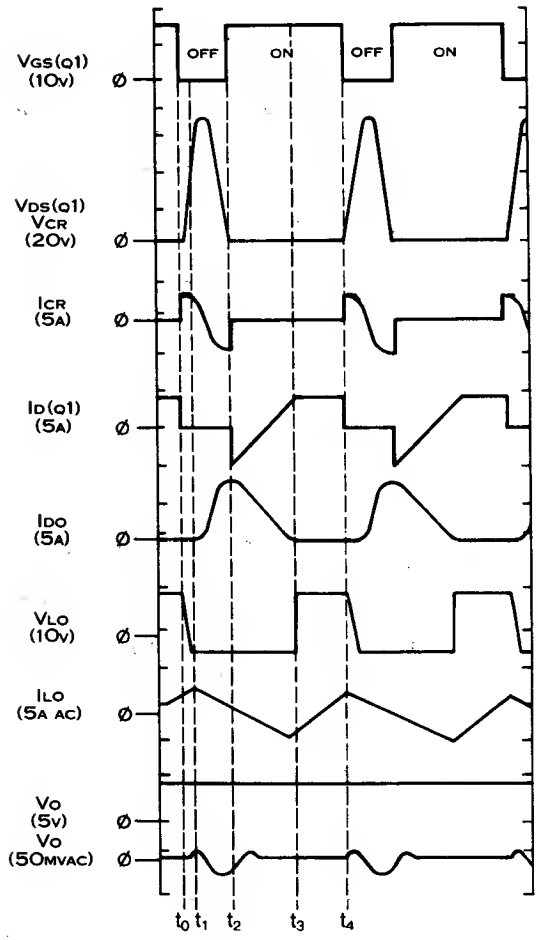

FIGURE 4 .

INDUCTOR CHARGING STATE
Time interval: t2 < t < t3

To facilitate zero voltage switching, the switch is activated once the voltage across the switching device and the resonant capacitor has reached zero, occurring at time t2. During the interval from t2 to t3, the resonant inductor current is linearly returned from its negative peak of minus Io to its positive level of plus Io.

The output filter section catch diode conducts during this interval, continuing to freewheel the full output current, and clamping one end of the resonant inductor to ground through the output diode. The voltage across the resonant inductor is equal to Vin - VDo resulting in a linearly rising resonant inductor current along with a linearly decreasing catch diode current. Energy stored in the output inductor is providing the output power to the load during this interval.

A noteworthy peculiarity during this timespan can be seen in the switch drain current waveform. At time t2, when the switch is turned on, current is actually returning from the resonant tank to the input source, Vin. An interesting diversion is that the switch can virtually be turned on at leisure during the first half of the t2 to t3 interval at any time without interfering with normal operation. A seperate time interval could be used to identify this region if necessary.

$ILr(t)=ID(t)= -Io+[(Vin+VDo)/Lr]*t \quad t2<t<t3$
$VLr=Vin+VDo$
$IDo(t)=Io-ILr(t) \quad t2<t<t3$
$ILo=Io \; ; \quad VLo= - Vo+VDo$

POWER TRANSFER STATE
Time interval : t3 < t <t4

Once the resonant inductor current has reached the output current at time t3, the zero voltage switched converter resembles that of a conventional square wave power processor. During the remainder of the conversion period, most of the pertinant waveforms approach DC conditions.

With switch Q1 closed, the input source is supplying the output current, and the output filter inductor voltage equals Vin minus Vout. Both the switch current and resonant inductor currents are equal to the output current.The output catch diode voltage equals Vin, and no current flows.

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In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the timing interval between t3 and t4. Variable frequency operation is the result of modulating the on-time as dictated by line and load conditions. Increasing the ON time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter.The conversion frequency is inversely proportional to output load.

Vds=Io*Rds(on) ; Id=Io
VLo=Vin-Vo ; ILo=Io
VDo = Vin

TIMING INTERVAL SUMMARY

dt10 = (Cr * Vin) /Io
dt21 = (Pi/Wr) + (1/Wr)ARCSIN[Vin/(Io*Zr)]
dt32 = (2*Io*Lr) / Vin
dt43 = (Vo*dt30) / (Vin-Vo)
where dt30=dt10+dt21+dt32

and the conversion period (tconv)=
dt40=dt10+dt21+dt32+dt43

CONTROL CIRCUIT PROGRAMMING

Determination of the range of required ON and OFF durations of the control circuit is necessary to program the UC3864s VCO and one-shot timer. Equally as important is the need to analyze these variations to accommodate changes in line voltages, load currents, component initial tolerances and temperature effects. Once obtained, the minimum and maximum operating frequencies define the VCO timing component values. Additionally, the one shot timer is programmed for the maximum on-time, and modulated by the ZERO detect circuitry to facilitate true zero voltage switching. [9]

OFF - TIME

The OFF-TIME of the switch and controller includes the linear charge and resonant intervals which begin at time t0 and end at time t2.

t off = t10 + t21

MAXIMUM OFF - TIME

The maximum off-time is used to program the one-shot timer which corresponds to :
t off max = dt10 max + dt21 max

t off max = [1 + (1.5 * Pi)] / Wr
= 0.909 / Fres

MAXIMUM CONVERSION FREQUENCY

The maximum conversion frequency occurs as both the switch ON-TIME and OFF-TIME go to their minimum value. For the circuit to remain resonant, the inductor charging interval limitations must be satisfied, therefore dt32 cannot go to zero. However, the power transfer interval, dt43, can, although the output will be out of regulation. [10]

MINIMUM ON - TIME

t on MIN = dT32 MIN + dT43 MIN
= 1/(Pi * Fres) = 0.318 / Fres

The conversion period (t40) is the sum of the four timing intervals and equal to the ON plus OFF times of the switch. The conversion frequency, Fconv, is the reciprocal of the conversion period.

f conv = 1/ tconv = 1 / t40

Both minimum and maximum conversion frequency need to be calculated to program the UC3864 VCO, a task best performed by a personal computer. The program should accommodate component initial tolerances, diode and switch voltage drops versus output currents, in addition to the temperature effects on all.

ZVS FORWARD CONVERTER DESIGN SPECIFICATIONS

A low voltage DC/DC converter design has been selected for the purposes of generalization and simplicity. Each of the previously listed equations will be utilized to determine the circuit specifics and can be altered by the user to accommodate circuit and device losses. A resonant tank frequency of 500 KiloHertz will be incorporated as a compromise between high frequency operation and minimal circuit and device parasitic interference. The maximum conversion frequency of this design will approach that of the resonant tank , but never exceed it in normal operation.

SPECIFICATIONS

Vin = 18 to 26 VDC
Vout = 5.0
Iout = 2.5 to 10 ADC
Fres = 500KHz

INTERVAL DURATIONS : t10 - t43

VARIATIONS WITH LINE & LOAD

	VIN=18		VIN=26	
	IO=2.5	IO=10	IO=2.5	IO=10
(uSec)				
dT10	0.217	0.055	0.314	0.078
dT21	1.29	1,06	1.49	1.08
dT32	0.93	3.72	0.64	2.58
dT43	1.39	6.68	0.78	1.78
Tconv	3.83	11.51	3.23	5.52
Fcon	261K	87K	310K	181K

SWITCH DURATIONS (uSec)

Toff	1.51	1.11	1.80	1.16
Ton	2.32	10.4	1.42	4.36

The ZVS Forward converter gain in kiloHertz per volt of Vin (KHz/V) and amp of Iout (KHz/A) can be evaluatated over the specified ranges. As summary of these follows.

AVERAGE d(Fconv) / d(Vin) vs Iout

Io =	2.5A	5A	7.5A	10A
dF/dV =	11.25	11.8	11.75	10.25

Average d(Fconv) / d(Vin) = 11.26 KHz/V

The highest gain of 11.87 KHz/V occurs near full load.

AVERAGE d(Fconv) / d(Io) vs Vin

Vin =	18	20	22	24	26
dF/dI =	23.3	22.1	20.5	18.8	17.3

AVERAGE dF/dI (KHz/A) = 20.4

The highest gain of 23.3 KHz/A occurs at Vin min.

It may be required to use the highest gain figures to compensate the control loop for stability over all operating conditions. While this may not optimize the loop transient response for all operating loadlines, it will guarantee stability over the the input and ouput variations.

PROGRAMMING THE CONTROL CIRCUIT

ONE - SHOT : ACCOMMODATING OFF - TIME VARIATIONS

The switch off-time varies with line and load by approximately +/- 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects will result in an much wider excursion. For all practical purposes, a true fixed off-time technique will NOT work as previously mentioned. Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

In this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting any temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a minimum of 5:1 (minimum to maximum) range of duration, and will programmed for 3.0 uS (max), controllable down to 0.60 uS. Programming of the one-shot requires a single R-C time constant and is straighforward using the design information and equations from the datasheet. Implementation of this feature is shown in figure 3.

PROGRAMMING THE VCO

The calculated range of conversion frequencies spans between 87 KHz and 310 KHz which will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences. First, a minimum conversion frequency of 75 KHz has been selected

9

and programmed according to the following equation:
Fvco min = 3.6 / (Rmin * Cvco)

The maximum conversion frequency of 350 KHZ is programmed by:
Fvco max = 3.6 / [(Rmin || Rrange) *Cvco]

Numerous values of Rmin and Cvco will satisfy the equations which can be simplified by letting Rmin equal 100K.

Cvco (uF) = 0.036 / Fmin(KHz)
Rrange(K)= 100 / [(Fconv max/Fconv min) - 1]
where Rmin= 100 K , Cvco= 480 pF (use470pF)
Rrange= 27.2 K

The VCO gain in frequency per volt in from the error amplifier output is approximated by :
dF/dV = 1 / (Rrange * Cvco) = 78.2 KHz / V
with an approximate 3.6 volt delta from the error amplifier.

ZERO DETECTION CIRCUIT

True zero voltage switching occurs every cycle as the ZERO detection circuitry modulates the width of the one-shot output. The falling edge of the resonant capacitor waveform is sensed, resistively scaled and fed to one input of the the ZERO comparator. Its other input is a precision 0.5 volt reference and the output is tied to the one-shot. Once the half-volt threshold is crossed, the one-shot output is clocked, thus terminating the output and initiating the next VCO timing pulse. Typical operation is show in figure 5.

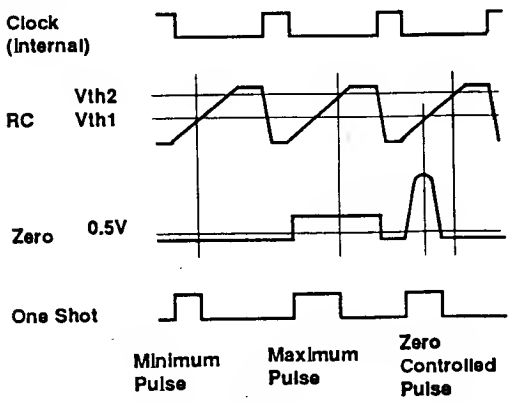


Figure 5.

FAULT PROTECTION- SOFTSTART & RESTART DELAY

One of the many unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latchoff following fault, etc) with a single resistor to ground or Vcc.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 milliseconds and a restart delay of approximately 200 milliseconds. The pre-programmed ratio of 19:1 (restart delay to softstart) will be utilized. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short cirucit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold. Core reset is accomplished by the bidirectional resonant current in this transformers primary.

TIMING EQUATIONS:

SOFT START (Tss)
Tss = Csr * 10K ohms

RESTART DELAY Trd
Trd = Csr * 190 K ohms

TIMING RATIO (Trd:Tss)
APPROX 19:1

GATE DRIVE

Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem poles shows 30 nanosecond rise and fall times into 1nF. One significant advantage of zero voltage switching is the reduced "miller" effects at the fet gates - the switch is only transitioned while Vds has reached zero, substantially reducing the gate drive requirements.

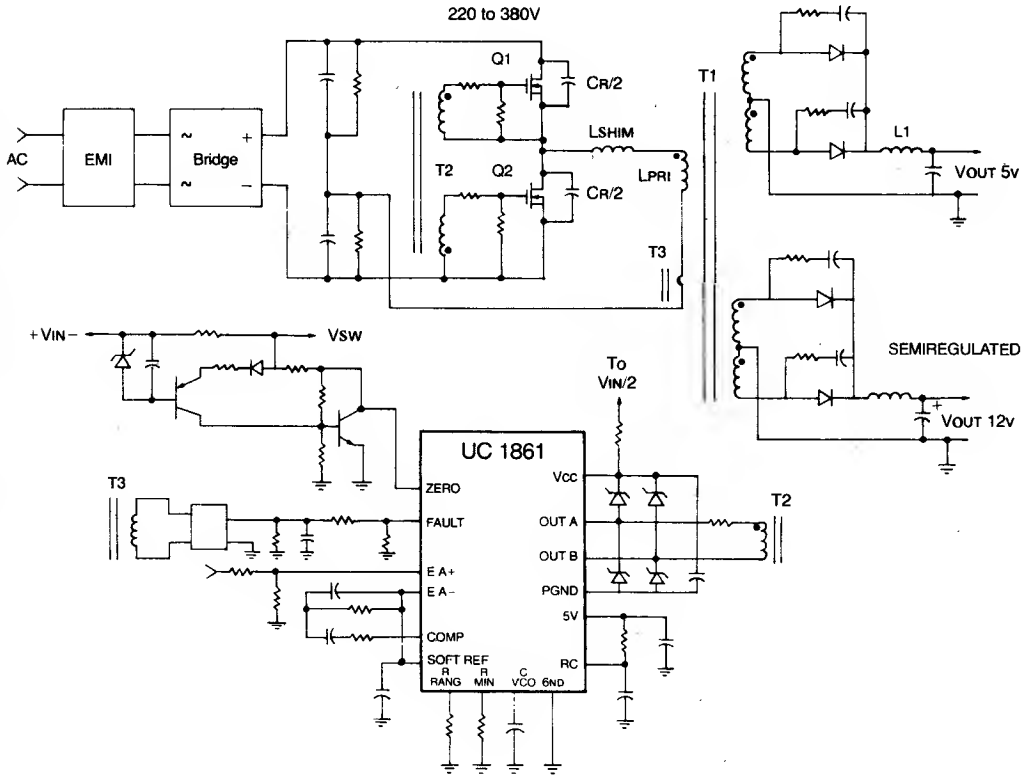
LOOP COMPENSATION GENERAL INFORMATION

The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unike the dual loop system of current mode control, the ZVS output filter section exhibits a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for high low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filters two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

ZVS HALF - BRIDGE

The foundation of zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains quite similar, ther is a difference in the resonant interval, t1-t2.

ZERO VOLTAGE SWITCHED HALF-BRIDGE CONVERTER



Unlike the single switch converter's high off-state voltage, the bridge circuits clamp the voltage excursions to the DC input rails, thereby reducing the switch voltage stress and requirements. This alters the duration of the off segment of the resonant interval since the opposite switch(es) must be activated long before the resonant cycle were to have been completed. In fact, the opposite switch(es) should turn on immediately ofter their voltage is clamped to the rails while their drain-to-source voltage equals zero. If not, the resonant tank will continue its resonance and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes. To guarantee true zero voltage switching, it is necessary to incorporate a zero voltage detection circuit, and modulate the controller's programmed off-time. The circuitry shown connected to the UC1861 ZERO input performs the attenuation and sensing to interface to the switch voltage in this half-bridge design.

THE UC1861 CONTROLLER

The UC1861 controller is similar to the UC1864, and incorporates a toggle flip-flop to generate the alternating A and B outputs for half and full bridge applications. All other programmable features and connections remain identical to the UC1864 IC. Each device is optimized for controlling zero voltage switched converters at frequencies into the megahertz with minimal parts count and interface logic.

SUMMARY

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the mosfet output capacitance can be significant at high switching frequencies, imparing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the uscful load range of the converter as well, an unacccptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [11,12] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detremental parasitics generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

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CHIP PAIR PROVIDES ISOLATED DRIVE FOR POWER MOSFETS IN PWM DRIVES REQUIRING 0% TO 100% DUTY CYCLE

UNITRODE'S UC3724 AND UC3725

Claudio de Sa e Silva
Senior Applications Engineer

INTRODUCTION

Designers of power drives for PWM motor controls and switching power supplies often have to face the problem of how to drive the high-side transistor in a totem-pole MOSFET output stage. In most cases there are several of these to implement, and the problems of cost, complexity, and low efficiency tend to be discouraging. For many reasons, it is usually desirable to use N-channel MOSFET devices exclusively, and the need to drive the high-side transistor's gate to a voltage ten to fifteen volts above the upper rail can lead to complicated and often unreliable schemes.

The new chip pair UC3724/UC3725 from Unitrode offers an elegant, compact, and comparatively inexpensive way out of this dilema. To put it briefly, the two chips—together with a small pulse transformer which supplies the required isolation—employ a modulated carrier to convey both the switching power and the ON/OFF information to the MOSFET gate. The circuit of Fig. 1 shows all that is needed for fast switching of a power transistor at any of the voltages commonly found in motor control or power supply applications.

The primary chip (UC3724) generates a carrier signal, usually at a frequency of several hundred kilohertz, and applies it to the transformer primary with one of two possible duty cycles, determined by a TTL-level logic input. The output signal is delivered to the transformer by a current-sensing circuit which ascertains that the primary current reaches zero before starting each new cycle, thus preventing direct current buildup in the winding. This is done continually, at both high and low duty cycles, and has the significant consequence that the average voltage of the output signal is always zero. A properly designed transformer (see below) cannot saturate under these conditions, and there are no severe transients that can affect the response at each duty cycle change.

Because of the high carrier frequency and constantly monitored primary current, the transformer can be constructed using a high permeability ferrite core of no more than 0.5in OD. Though very small, the transformer can easily provide more than 1000V of isolation, with minimal capacitance between windings, and very low leakage inductance.

On the power circuit side, the secondary chip (UC3725) rectifies the steady carrier with an efficient full-wave Schottky bridge and stores in a small capacitor the energy needed to run its internal circuits and to deliver the husky one ampere current pulses required to charge the power MOSFET gate in a fraction of a microsecond. The incoming duty cycle, which may be either low (about 33%) or high (about 67%), is sensed by the internal circuit to determine the high or low state of the output drive. Furthermore, the same secondary IC contains a local current-sensing feature that can be used to terminate an ON command if the load current exceeds a given value. This extremely fast current-limiting circuit works in a hickcup mode, with both the current level and the fixed off-time selected by the user.

DRIVING THE MOSFET GATE

It should be noted that although the instantaneous power needed to charge the MOSFET gate from zero to 15V is relatively large if the switching time is short, the long-term average power is quite low. This is because the switching time, during which gate current flows, is necessarily small compared to the period of the PWM signal. The isolation transformer needs to transfer power to the secondary side at the average rate only, and this is why it can be of very small size.

By way of illustration, consider a large MOSFET with an equivalent gate charge of about 200 nanocoulombs. For an ON voltage of 15V, we calculate an equivalent capacity of 13nF. With the 15 ohm resistor shown in Fig. 1 in series with the gate (to limit the peak current to the rated 1A maximum), we can approximate the gate voltage as a rising exponential function of time, of the usual RC variety with which we are familiar. Thus; the gate voltage starts from zero and approaches 15V with a time constant of 10 * 13 = 130 nanoseconds.

Now, it so happens that the efficiency of charging a capacitor through a resistor is 50%, so that the energy required to charge the gate fully is equal to twice the amount stored. Consequently,

1) Energy used to charge the gate = $C * V^2$.

Using Eq.1, the energy needed per cycle turns out to be 3 microjoules, a result which could also be obtained by simply multiplying the equivalent gate charge by the gate source voltage. At a switching frequency of 30KHz, this amounts to an average gate drive power of only 90mW, even though the instantaneous peak value is actually 15W. The small transformer must be rated to handle the average 90mW—plus the low power needed to run the chip, while the secondary storage capacitor C1 supplies the high instantaneous peaks. Not that no additional energy is required to discharge the gate capacitance at the end of each ON time; at these times, the stored energy is simply dissipated locally.

THE PRIMARY SIDE: UC3724

A block diagram of the UC3724 is shown in Fig. 2. The carrier signal is generated by a retriggerable monostable multivibrator working in conjunction with the current sensing circuits of the output stages. The timing components Rt and Ct can be chosen for any frequency from 3.3KHz to 600KHz by referring to the curves supplied in the data sheet. If the chip is energized without a transformer primary connected across the two output terminals, the oscillator will not run, and the voltage at pin 1 (Ct) will remain fixed at about 2.9V. This is a normal condition, caused by the absence of current at the output dirvers. In this state the differential output voltage VA - VB is positive if pin 7 is high, and negative if pin 7 is low.

With the transformer connected to pins 3 and 5, the primary magnetizing current is sensed by one of the two current-sensing comparators to generate the signal required to trigger the multivibrator. This causes the oscillator to run, and the waveform appearing at pin 1 will be as shown in the timing diagram of Fig. 3. If we observe the output signals at pins 4 and 6 differentially, we will see the waveform labelled Va-Vb in the diagram. It has two main characteristics:

1. The duty cycle is either 1/3 (33%) or 2/3 (67%) approx.:

2. The average voltage is always zero.

While the capacitor Ct is charging, the voltage Va-Vb is just 2V lower than Vcc. During this time, the magnetizing current increases linearly with slope

2) di/dt = (Va-Vb)/L amperes per second,

where L is the primary magnetizing inductance. When the timing capacitor voltage reaches the threshold value of 2.5V, the output voltage (Va-Vb) is reversed in polarity and, at the same time reduced by one-half. With this now opposing voltage, the magnetizing current begins to decrease with a slope equal to half the value given by Eq.2, towards zero. At zero current, one of the two current-sense comparators triggers the multivibrator to start another cycle. This resets the core once per cycle, preventing saturation and protecting the chip from uncontrolled output currents.

From the above description, it is clear that the generation of the output signal depends heavily on the shape of the magnetizing current waveform. But the output current contains another component, namely the current that carries the power needed at the secondary side. The bridge rectifier at the input of the UC3725 works in our favor here, because it is essentially OFF during the half-voltage part of the cycle. For this reason, the total primary current looks like the Iprim trace in Fig. 3. For best results, the primary inductance should be chosen so as to obtain a peak magnetizing current of between 20mA and 40mA. If the chosen PWM frequency is f,

3) L = 10(Vcc-2)/f henries. (for 33mA peak Imag)

With Vcc=22V and f=200KHz, this gives L=1mH. A Ferroxcube toroidal core 204T250-3E2A, with an OD of 0.5In has the following specifications:

A1 = 3uH/turn squared; equivalent length = Le = 3.12cm.

We calculate N^2 = L/A1; N = 18 turns, and

4) Imax = H*Le/1.25*N = 69mA.

Here the current Imax has been calculated for H = 0.5 oersteds, or B = 2800 gauss approximately (see Ferroxcube Linear Ferrite catalog). With these values, this core can be used at temperatures well above 70C.

THE SECONDARY SIDE: UC3725

It can be seen from the block diagram of Fig. 4 that the transformer secondary winding supplies power to the chip through the internal full-wave rectifier bridge of high efficiency Schottky diodes. A small storage capacitor must be connected from pin 3 to pin 1 to filter out the carrier frequency and to supply peak output currents; in most cases, a 1uF ceramic type with low ESR will be adequate. The signal from the transformer is also applied to a high hysteresis comparator where the two possible incoming duty cycles are recognized.

In this discussion we will refer to pin 1 as GROUND and give all voltages with pin 1 as the reference point, even though it is rarely used at ground potential. In most applications, this pin is connected to the source terminal of a high-side power MOSFET transistor, and the UC3725 with its external circuit components ride with the load between power ground and the positive rail.

With the transformer output applied to pins 7 and 8, the circuit is ready to drive the power MOSFET if:

A. The voltage Vcc (at pin 3) is 12.6V < V3 < 35V:

B. ENABLE (pin 6) is low:

C. The voltage Vcs (at pin 4) is OV < V4 < 0.5V;

D. The voltage Vt (at pin 5) is high (about 7.2V).

If these conditions are satisfied, the OUTPUT voltage Vo (pin 2) will be controlled by the duty cycle of the signal received from the transformer and sensed by the input comparator.

The transformer cannot pass DC, and therefore the voltage Va-Vb, measured between pins 7 and 8 must have an average value of zero volts. If the duty cycle is "low" (about 1/3), the positive excursion has a shorter duration and, consequently must have a higher amplitude. This means that current will flow into pin 7 and out of pin 8 during these short pulses, and not at all during the remaining 2/3 of the period. The comparator output stays high as long as the duty cycle does not change, and the output voltage (pin 2) is held low: the power MOSFET is held OFF. Conversely, if the differential voltage Va-Vb has a "high" duty cycle, the negative voltage excursion will be higher, and the power transistor will be ON.

CURRENT LIMIT: By applying to pin 4 a voltage proportional to the current flowing through the power transistor, as shown in Fig. 1, it is possible fo turn OFF the device with a minimum of delay, thus protecting it from damage in case of shorts or other mishaps. The chip itself is capable of reacting in less than 50ns, so that the time constant of the RC filter between the MOSFET source and pin 4 will be responsible for most of the turn-off delay. This filter is usually required to prevent false triggering of the current sense comparator.

The two components Rt and Ct at pin 5 set the time during which the power device is held in the OFF state after an overcurrent condition is detected. The OFF time is

4) t = 1.28*Rt*Ct seconds.

If the current limit feature is not required, pin 4 should be grounded, and pin 5 should be left open.

LAYOUT PRECAUTIONS

Because of the high performance requirements of the applications for which the UC3724 and UC3725 were designed, these ICs offer extremely fast circuits with low propagation times. For this reason, the circuit layout in breadboarding and in the final product design should be done with care, if unnecessary problems and delays are to be avoided. A good ground plane over the circuit area—which is relatively small anyway—is always helpful. Good quality ceramic filter capacitors for Vcc in both primary and secondary circuits are mandatory. Ground loops must be shunned like the plague: it is easier to avoid them from the start than to eliminate them later.

NOTE: The name "ground loop" is an unfortunate misnomer. It has led some to believe it is enough to avoid closed loop circuits in which ground currents could conceivably circulate and cause all kinds of trouble. But the problem is quite different, and requires a different solution.

Refer to the UC3725 circuit in Fig. 1. There are several components connected to "ground", such as the capacitors from pins 3, 4, and 5, for example, You will have a ground loop if you return any of these to a point in the ground bus that is remote from the chip's ground pin, or pin 1 in this case. Depending on the current level and switching speed, even a fraction of an inch can be too far. The reason is that the ground wires (or traces) always have some small but finite amount of resistance and inductance, and it is the voltage drops due to these can often cause malfunctions.

CONCLUSIONS

With the UC3724 and UC3725, the problem of driving an N-channel power MOSFET with high voltage isolation between the low level and the power circuits can be easily handled. The chips are suitable for use in PWM amplifiers at switching rates of over 50KHz, which makes them suitable for most motor applications, as well as many power supply designs. A number of novel configurations not specifically described here will surely come to mind to experienced designers. For example, using a transformer with multiple secondaries, it is possible to have one UC3724 commutating two or more UC3725, each controlling its own power transistor.

The devices are useful also in "off the line" power stages, where all of the power transistors must be driven with isolated drivers in order to meet UL or other specifications.

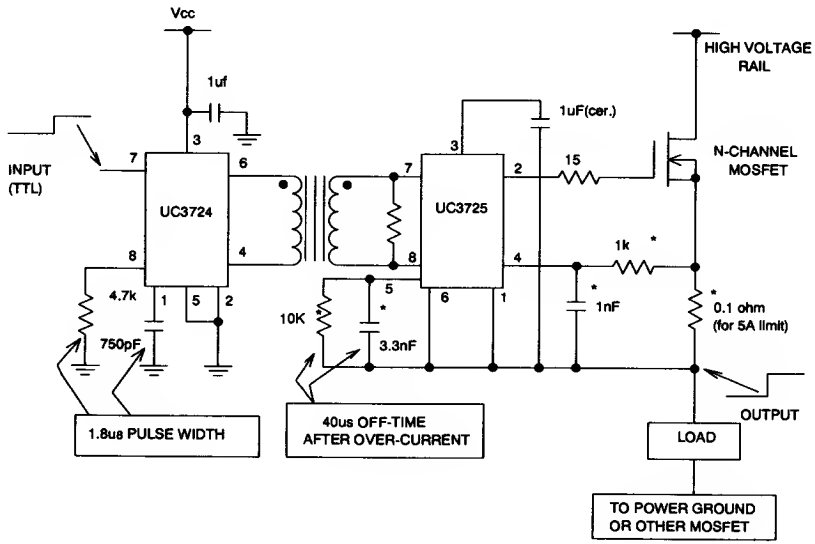

FIGURE 1: Isolated MOSFET driver. The five current-sensing components (*) can be omitted if this feature is not required.

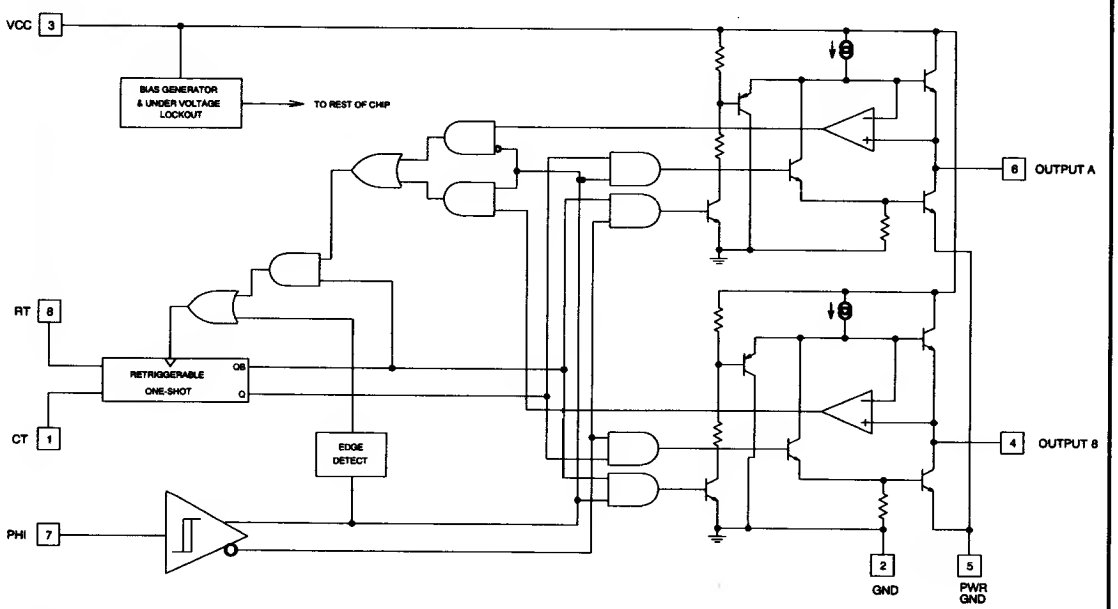

FIGURE 2: UC3724 Block Diagram

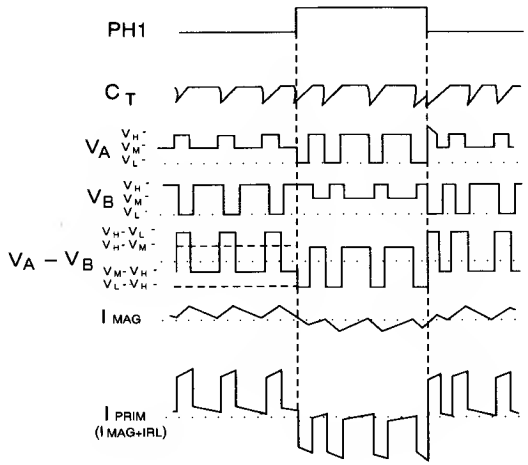

FIGURE 3: UC3724 Timing Diagram

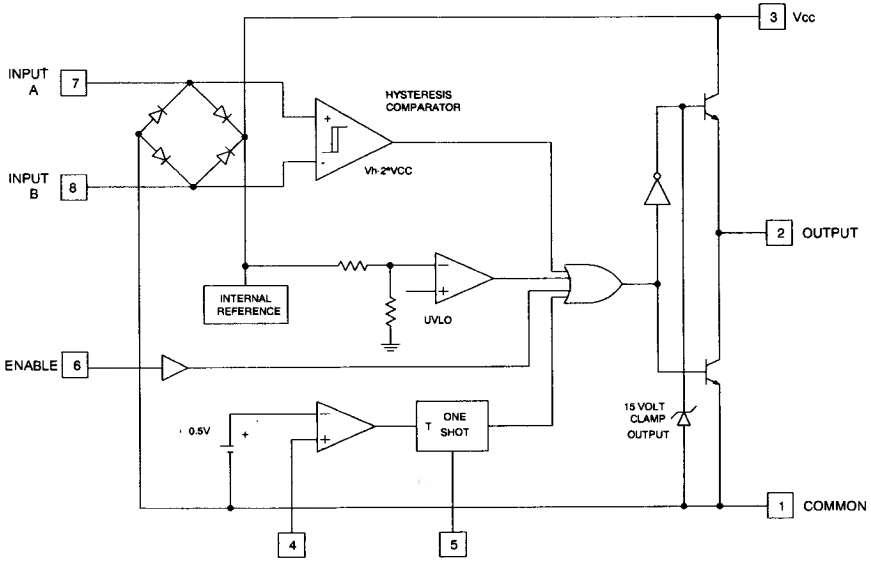

FIGURE 4: UC3725 Block Diagram

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POWER FACTOR CORRECTION WITH THE UC3854

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POWER FACTOR: WHAT CAN BE DONE TO IMPROVE IT

In an electric power distribution line, the power factor is the ratio of real power (watts) to apparent power (volt-amperes). The optimum value for this ratio is unity, a value that is obtained only when the line current is sinusoidal and in phase with the line voltage — assuming, of course, that the line voltage is itself sinusoidal. This means that any current component in quadrature with the fundamental, and any components at frequencies other than the fundamental (harmonics), cannot carry any power to the load. However, these components contribute to total line losses, and because they add to the current actually required by the user, they mandate the use of heavier wiring and circuit breakers, which means increased installation costs.

In the past, the main cause of low power factor was phase lag, caused by the inductive characteristic of the electric motors which accounted for a large portion of the overall load serviced by the electric power companies. In this case, the power factor is equal to the cosine of the phase angle — unity when the angle is zero. Phase lag can be corrected by simply adding the right amount of capacitance in shunt with the offending machinery, as has been done for many years.

With the advent of the electronics industry during the post-war decades and, more recently, the enormous increase in the number of computers and other equipment incorporating line rectifiers followed by capacitor-input filters, the nature of the problem has changed. The current drawn by these circuits is distinctly non-sinusoidal, as shown in Fig.1, The distorted current waveform in the figure is the sum of many components of different frequencies, the one at the fundamental line frequency being the only useful one. The resulting power factor may be as low as 50% under these conditions, and if the power involved is higher than several hundred watts, cost considerations alone make it imperative for equipment manufacturers to search for some means of improvement. In addition, there are environments — aboard submarines, for example — where the allowable percentage of harmonics in the line current is extremely low. In these systems, the use of an advanced form of power factor correction is a basic requirement.

With Unitrode's UC3854 High Power Factor Preregulator, the task of reducing the amount of distortion in the line current waveform becomes easy and cost-effective. This monolithic integrated circuit contains all the active control devices required to obtain power factors approaching unity, with only a handful of additional components needed to tailor the overall circuit to specific requirements. Furthermore, the device makes possible the design of a preregulator capable of operating over a wide range of power line voltages without any component or wiring changes. This means that the equipment can be plugged into any commercial power outlet in the world, regardless of the local voltage or frequency.

HOW THE UC3854 IMPROVES THE POWER FACTOR

In a simple power supply, such as the one shown in Fig. 1, the DC load draws current as needed from the "bulk" capacitor, while the full-wave rectifier replenishes the capacitor at each half-cycle with bursts of current that occur briefly at each voltage peak. The output voltage Vo is essentially constant, while the input AC current is badly distorted, as shown. We can eliminate this distortion with a high power factor PWM preregulator which, working between the rectifier and the bulk capacitor, forces the replenishing current to have the same waveshape as that of the line voltage. The same PWM circuit can be used to sense and to some extent regulate the output DC voltage.

Two independent feedback loops are involved. The inner current control loop must have a bandwidth wide enough to follow accurately the waveshape of the full-wave rectified line voltage. This waveshape is the sum of the following components:

	average DC value----------63.7% of Vpk
+	2nd harmonic----------42.4%
+	4th harmonic----------8.5%
+	6th harmonic----------3.6%
+	8th harmonic----------2.0%
+	10th harmonic----------1.3%
+	higher harmonics.

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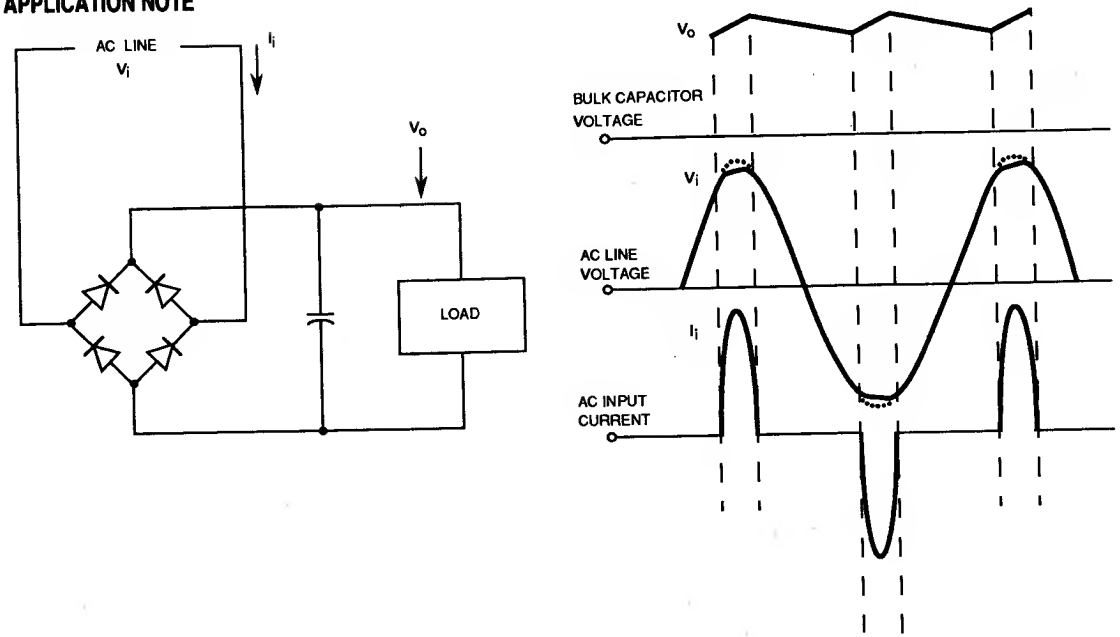

Figure 1. Voltage and current waveforms found in conventional capacitor filtered rectifiers.

Fig. 2 shows the first three of these components to scale. Because the amplitude of the 16th harmonic (960Hz for a 60Hz line) is only 0.5% of the input line voltage, with higher components becoming progressively smaller, a current loop bandwidth of a few kilohertz is adequate to accommodate all of the significant signal components. The PWM switching frequency must be well above the unity gain crossover frequency of the loop.

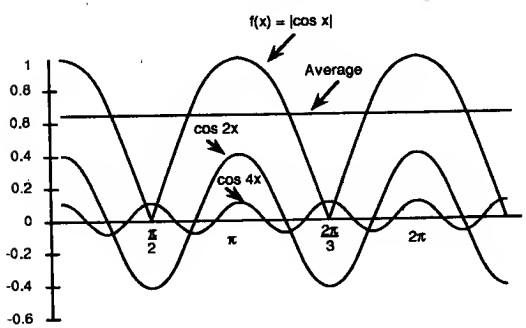

Figure 2. Rectified cosine wave f(x) = |cos x|, with average (DC value), second, and fourth harmonics shown. (Higher harmonics have been left out for clarity.

By sensing and controlling the average current value — rather than peak, as is done in some schemes — we maintain the same extremely low level of distortion in line current over the full range of current values, even though the required boost inductor value is quite low. This means that the mode boundary (between continuous and discontinuous modes), that is inevitable at some low current value, is of no concern to us, since the loop knows and controls the right thing: the average value of current.

Because load current varies, a voltage control loop is also required. (See Fig. 3). This outer loop senses the bulk capacitor voltage and keeps it constant by regulating the line current as required by the changing load. Unlike the current control loop, this feedback circuit must have a narrow bandwidth to prevent the voltage ripple (at twice the line frequency) from distorting the current waveform. Any interference of this type will defeat the main objective, which is to minimize the harmonic content of the line current.

Besides these two main functions, the UC3854 incorporates line voltage feedforward. This stabilizes the voltage control loop gain which would otherwise vary with the square of the line voltage. It provides fast constant power control when the line voltage varies, which also accounts for the wide range of

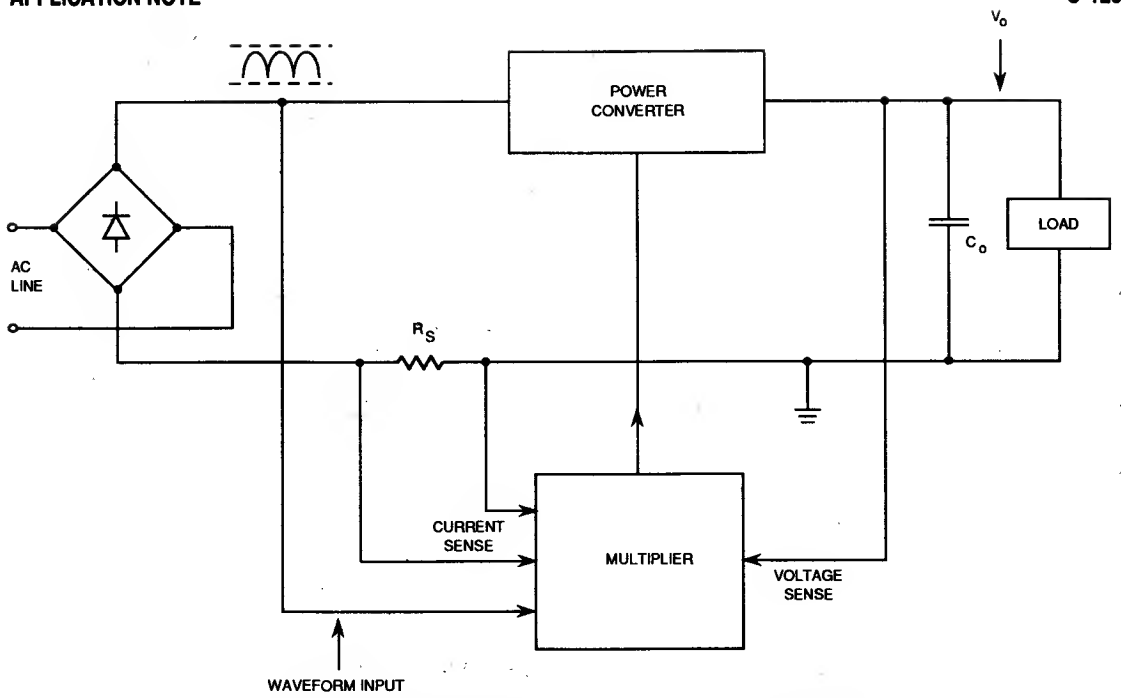

Figure 3. Basic configuration of high power factor control circuit, showing inner current loop and outer voltage loop.

input voltages that the preregulator can accomodate without any adjustments. (See Ref. 1 for an excellent treatment of this subject).

THE POWER OUTPUT CONVERTER

For the power stage, we have the choice of either a flyback, a buck, or a boost configuration (see Fig. 4). We will concentrate on the boost topology here, because it offers the most significant advantages. Its main characteristics are that the input current is not chopped, and that the output voltage must be higher than the highest input voltage peak. The benefits are:

1. Energy is more efficiently stored in the bulk capacitor at high voltage, allowing use of smaller capacitor.

2. Longer hold-up time due to high voltage.

3. Lower RFI/EMI in line.

4. The input inductor helps block fast line transients.

5. Control can be maintained over full swing of line voltage, including zero volts.

6. Inductor current IS input current, facilitating use of current-mode control.

7. The switch voltage is no greater than the output voltage.

8. Easy to drive PWM switch at ground level.

The switching diode of the boost stage (see Fig. 4) requires the output voltage Vo to have a value higher than the line peak value. To accomodate input line voltages up to 270Vrms, the value of Vo must be at least 380VDC.

By operating the boost converter in the continuous mode, we can minimize the noise injected into the line and reduce the peak current in the boost transistor and diode. In this mode, the inductor current flows during the entire PWM period, with a finite amount of ripple present. The required inductance L can be calculated using the simple design rule (see Ref. 1),

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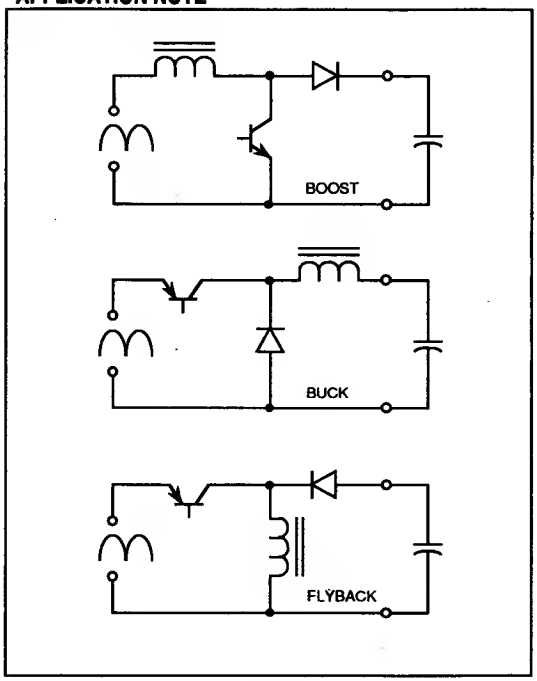

Figure 4. Basic converter topologies which can be used to implement the preregulator.

1) $$L = \frac{25{,}000}{f_S \cdot P_{in}} \quad \text{henries.}$$

where f is the PWM frequency, and Pin is the input power. For a 100Kz system, this simplifies to

2) $$L = \frac{0.25}{P_{in}} \quad \text{henries.}$$

This value of inductance will result in 20%p-p current ripple at the peak of the current waveform at full load and low line. Thus, if the peak value of current at low line is 5A, the maximum instantaneous current will be only 5.5A. At high line and low load, operation will become discontinuous, but with average current sensing, accuracy is preserved even if the percentage ripple is higher.

The bulk capacitor value C_o is often calculated in terms of the energy that must be supplied by the capacitor during a line dropout. If the output voltage is to drop from V_o to not less than V_{min} during the dropout period t_d, then

3) $$P_o \cdot t_d = 0.5 \cdot C_o \cdot (V_o^2 \cdot V_{min}^2) \quad \text{joules.}$$

If V_o = 380V, 1μF/watt will provide holdup to 335 volts for 20ms, and 2μF/watt will hold 363V for 20ms, or to 335V for 40ms. With the larger capacitor there will be less voltage ripple (second harmonic) present at the output, making it easier to achieve the desired low power factor with low distortion. Where low line current distortion is the overriding requirement, the capacitor size must be determined on that basis. The current that the boost stage delivers to the capacitor and load has an average value equal to the DC load current I_o, plus a single-frequency alternating component at 120Hz. The peak value of this AC component is equal to I_o, since the current swings from zero to $2I_o$. As this current flows through the capacitor only, we can calculate the ripple voltage V_{or} for a given capacitor C_o:

4) $$V_{or} = \frac{P_o}{2\pi \cdot 120 \cdot V_o \cdot C_o} \quad \text{volts peak}$$

where P_o is the output power and V_o is the output DC voltage. The effect of this ripple on the line current distortion is discussed in Section (K) below.

Gain of the Power Stage

The gain G_b of the boost stage is the incremental change in line current that results from an incremental change in duty cycle. Since the input current is equal to the 100KHz averaged inductor current in the continuous mode, and since the effect of duty cycle on the voltage appearing across the inductor is directly proportional to the output voltage V_o, it follows that

5) $$G_b = \frac{V_o}{sL} \quad \text{amperes}$$

where s is $(j \cdot 2\pi \cdot f_S)$, and f_S is the PWM frequency.

Inside and Around the UC3854

Refer to Fig. 8 for this section. Here we will discuss each of the various functions incorporated in the device, and explain its function and setup procedure. All values given are typical, unless otherwise indicated. Also, the component symbols used in this section correspond to those of Fig. 8.

(A) V_{CC} Supply, Pin 15: The recommended supply voltage to the chip is between 18V and 30V. Note that on power-up, the device does not become active until V_{CC} reaches 16V (provided that the enable input ENA is high). The current drawn before the turn-on threshold is reached will not exceed 2mA. At turn-on, this current increases to 10mA (20mA max) and

remains fairly constant thereafter. The V_{CC} turn-off threshold is set at 10V. These values permit the use of a simple and inexpensive V_{CC} supply.

(B) ENA, Pin 10: If the ENABLE input is low, the UC3854 will remain inactive even if V_{CC} is above 16V. This TTL compatible input provides an ideal on/off switch for the preregulator. Note that the REFERENCE voltage turns off when this input is low.

(C) R_{set}, Pin 12: The value of R_{set} determines the maximum value of PWM controlled line current by setting the peak current that the multiplier can deliver. If we denote the multiplier output current by I_m,

$$6) \qquad I_m\,(max) = \frac{-3.75}{R_{set}} \quad \text{amperes}$$

The negative sign indicates that this current flows out of Pin 5. If a resistor R_2 is placed between Pin 5 and the current sense resistor R_S, the peak line current will be limited to

$$7) \qquad I_i\,(max) = \frac{3.75 \cdot R_2}{R_{set} \cdot R_S} \quad \text{amperes}$$

(D) C_t, Pin 14: The capacitor C_t, together with resistor R_{set}, determines the PWM frequency:

$$8) \qquad f_S = \frac{1.25}{C_t \cdot R_{set}} \quad \text{hertz}$$

The saw-tooth waveform generated by the oscillator has a linear, positive slope, with an amplitude of 5.5Vp-p. The maximum usable frequency is in excess of 200KHz.

(E) REF, Pin 9: The enabled chip delivers a precise voltage V_{ref} of 7.5 volts at Pin 9, capable of -10mA with excellent regulation, and current-limited to -30mA.

(F) GT DRV, Pin 16: This output can drive a power MOSFET gate with an instantaneous peak current of 1A, allowing switching times of less than 100ns. Peak output voltage is internally limited to 16V. A peak current limiting resistor of about 20 ohms is recommended in series with the MOSFET gate. Note also that a maximum duty-cycle of 97% is specified.

The output duty cycle varies over its full range as the current amplifier output changes by 5.5V, which is the sawtooth peak-to-peak voltage. It follows that we can include the internal PWM control gain as part of the power stage gain G_b. To do this, we combine equation 5 above with the chip's PWM gain and get

$$9) \qquad G_{pwm} = \frac{V_o}{5.5 \cdot sL} \quad \text{siemens, or}$$

$$10) \qquad G_{pwm} = \frac{R_S\ V_o}{5.5 \cdot sL} \quad \text{volts per volt.}$$

Equation 10 gives the overall PWM/boost power stage gain in terms of the small signal voltage across the current sense resistor Rs divided by the small signal voltage at the current amplifier output, Pin 3.

(G) I SENSE, Pins 3, 4, and 5: The voltage across the current sense resistor R_S is applied to Pins 4 and 5, the input terminals of the current amplifier, with two equal resistors R_2 and R_3 (see Eq. 7). For average current sensing, the feedback components required between Pins 3 and 5 are as shown in Fig. 5. This amplifier's response is also shown in the figure, with the critical points labeled. Note that the phase response deviates from -90 degrees in the vicinity of the zero and pole, reaching a value of only -35 degrees if the two break points are separated by a factor of ten ($p = 10 \cdot z$). This fact will be important later, when we combine this amplifier with the power stage in a closed loop (see Eq. 10 above) because the boost converter introduces an additional phase lag of 90 degrees.

(H) MULTIPLIER and SQUARER, Pins 5, 6, 7, and 8: These blocks compute the quantity

$$11) \qquad I_m = \frac{K_m \cdot (V_a - 1) \cdot I_{ac}}{V_{rms}^2} \quad \text{amperes}$$

where I_m is the current IMULTOUT,
K_m is the multiplier constant,
V_a is the voltage amplifier output,
I_{ac} is the current into Pin 6,
V_{rms} is the voltage at Pin 8.

The voltage VAOUT directly controls power. The range of control is from IV (zero power) to 5.6V (peak power). If we pick the value 5V to correspond to the maximum power required in a given design, we will have a sufficient margin above that value before limiting occurs. Thus, we can select values for V_{ac} and V_{rms} such that at low line voltage and full load the voltage V_a will be 5V. For the line voltage range from 75V to 275V, the setup shown in Fig. 8 will give very good results.

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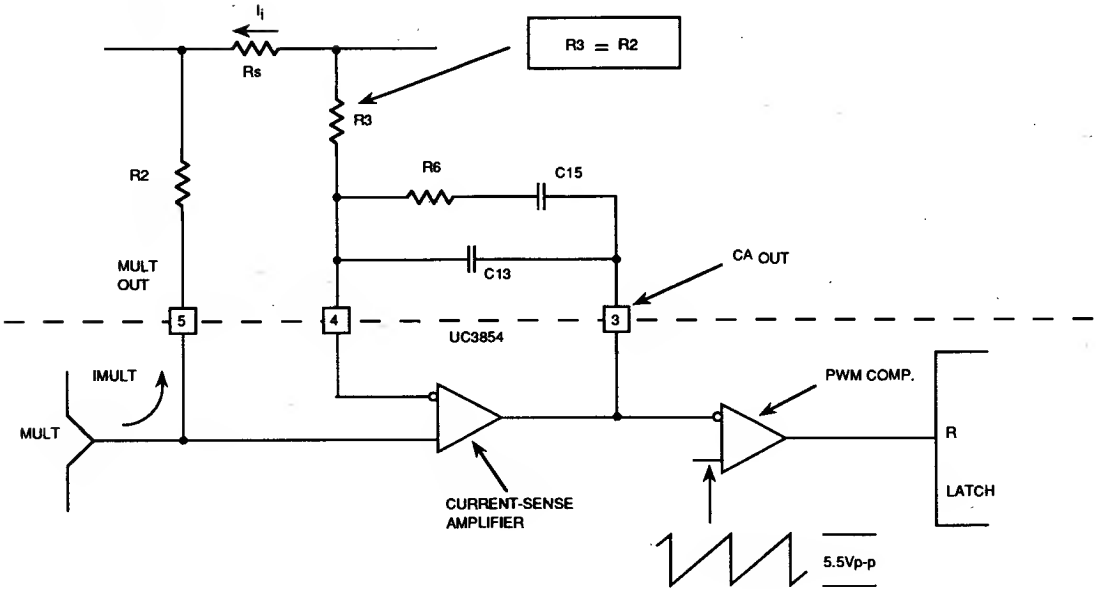

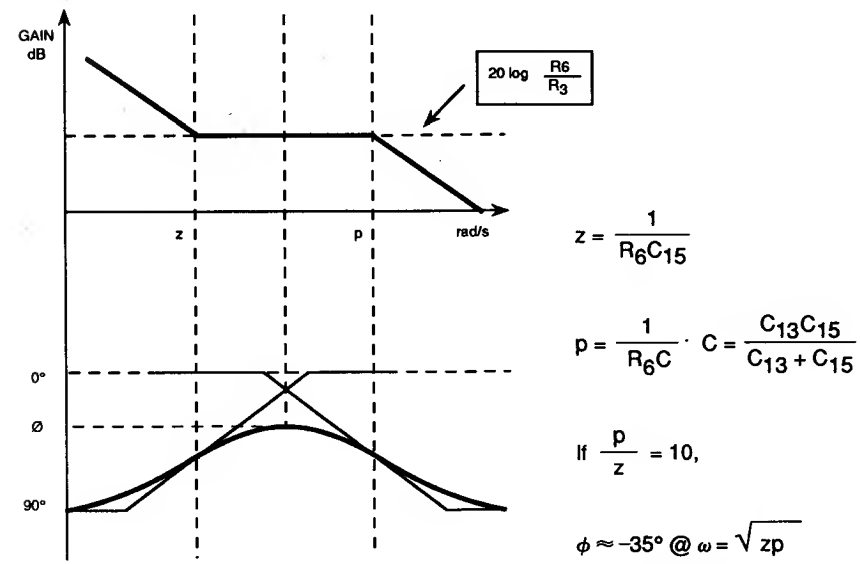

Figure 5A. Current-sense amplifier compensation. By setting the pole p at a frequency ten times higher than z, you can reduce the phase lag to -35° at the geometrical midpoint.

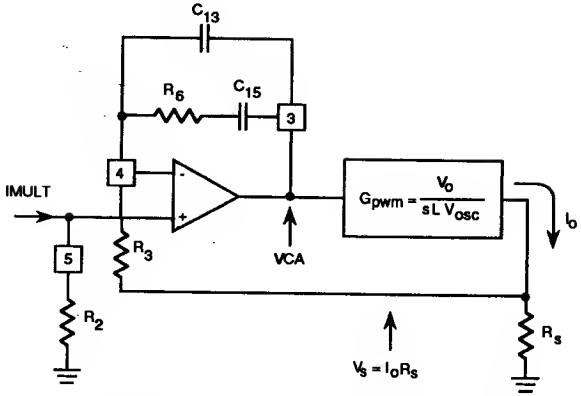

Figure 5B. Current control loop. The open-loop gain G_{CLO} is:

$$G_{CLO} = \frac{V_o R_s}{L V_{osc} R_6 C_{15}} \cdot \left[\frac{(s+z)}{s^2(s+p)}\right]$$

where $z = \frac{1}{R_6 C_{15}}$ (rad/s)

$$p = \frac{C_{13} + C_{15}}{R_6 C_{13} C_{15}} \text{ (rad/s)}$$

The constant K_m is the multiplier constant, approximately equal to -1, the negative sign indicating that the current I_m flows out of Pin 5. The voltage V_m that appears at Pin 5 depends on the value of R_2. (See above).

(I) I_{ac}, Pin 6: This current supplies to the UC3854 a sample of the rectified line waveform, which is needed to shape the line current. The output of the power rectifier supplies this small current through a large-value resistor, R_8. But because there is a potential of 6V present at Pin 6, and the full-wave rectified signal swings all the way to zero volts, a compensating resistor, R_{11}, is needed from Pin 6 to Pin 9, the REF output:

12) $R_{11} = 0.25 \cdot R_8$ ohms.

I_{ac} should be in the range from zero to 1mA. Therefore, for line voltages that can be as high as $275V_{rms}$, R_8 should be 500K or greater.

(J) VRMS, Pin 8: Ideally, this should be a DC voltage proportional to the rms value of the line voltage. Since the line waveshape does not change significantly, the average value will do just as well, and a good circuit for the purpose is shown in Fig. 6. This two-pole filter gives excellent attenuation of the various harmonics present, without introducing

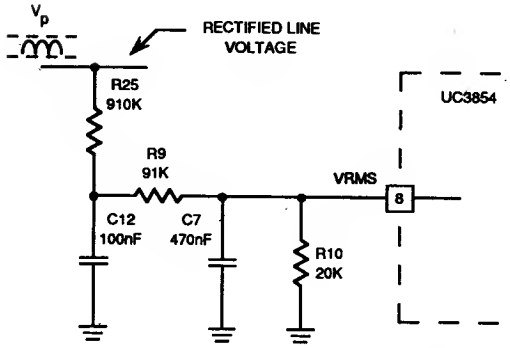

Figure 6. Two-pole filter for the V_{rms} input has a response of -34dB at DC, -67dB at 120Hz, and -79dB at 240Hz.

excessive delay in the DC output. This results in low output distortion and good transient response. The voltage applied to Pin 8 should be kept in the range from 1V to 5V. The values given in the circuit will meet this requirement for an input range from 75Vrms to 275Vrms.

Note that for each 1% of second harmonic ripple at Pin 8 there will be a contribution of 1% to the third harmonic content of the line current. This effect is

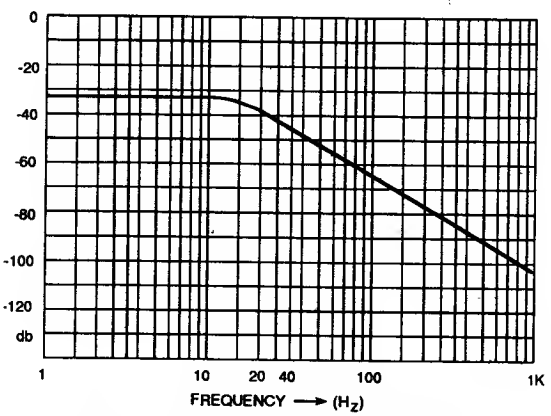

Figure 6A. Frequency response of the 2-pole RC filter of Figure 6.

additive with the contribution due to second harmonic ripple in Vo discussed below,

K) V SENSE, Pins 7 and 11: Except during soft-start, the non-inverting input to the voltage error amplifier is internally biased at 7.5V. The 50nA input bias current makes it possible to use high value resistors in the required biasing network, a valuable feature in view of the high voltages involved.

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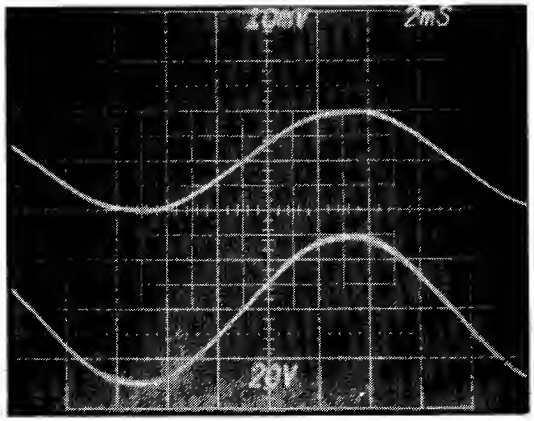
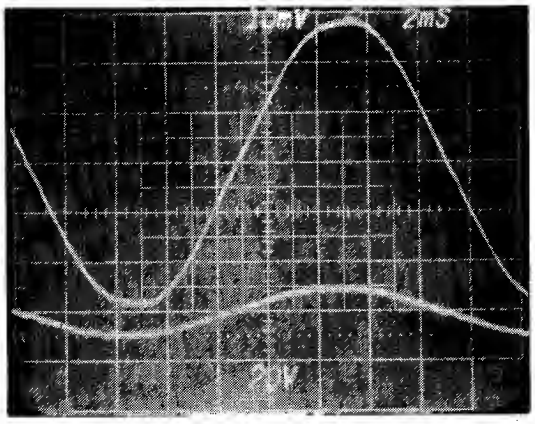


Top Trace: Line Voltage, $85V_{rms}$.
Bottom Trace: Line current, 2A per division.



Top Trace: Line Voltage, $250V_{rms}$.
Bottom Trace: Line current, 2A per division.

Figure 9. Line voltage and current waveforms obtained with the circuit of Figure 8.

(L) PK LIM, Pin 2: This comparator has an input threshold of zero volts. If its input (Pin 2) is driven below ground, the comparator instantly stops the PWM action, with the PWM drive (Pin 16) held low. The components R_4 and R_5 (1.6K and 10K respectively), shown in the complete schematic of Fig. 8, will provide peak limiting at about 4.8A. Capacitor C_3 can be added for noise filtering.

(M) SS (Soft Start), Pin 13: It has already been mentioned that in a circuit utilizing the boost topology, the output voltage cannot be less than the peak line voltage. In such a system, the soft start feature can only be effective in the output voltage range above that value. It is mainly with buck and flyback converter applications that the SS feature becomes fully operational.

POWERING THE UC3854

The UC3854 can be powered with a simple circuit such as the one shown in Fig. 8. Start-up power is supplied through resistor R_{22} and transistor Q_2. Since the maximum start-up current is only 2mA, the power dissipated in the resistor is only about 2.6 watts. After start-up, the secondary winding on the boost inductor begins to transfer energy through the full-wave rectifier bridge D_6, to supply the 20mA maximum current needed to sustain operation.

A 250W APPLICATION

Fig. 8 shows the complete diagram of a high efficiency power supply capable of delivering 250 watts with a power factor in excess of 0.999 and less than 3% harmonic distortion. The input current is limited at approximately 4A, which means that the inductor L_1 must be designed to handle that current. The rectifier D_2 must have very short recovery time rating to handle the high PWM frequency of 100KHz. Note the Schottky diode added from Pin 16 to ground, a precaution that is sometimes necessary to prevent conduction in the chip's substrate diode. Inrush current protection is included by the addition of a thermistor in series with the power line. See Fig. 9 for voltage and current waveforms obtained with the circuit of Fig. 8.

REFERENCES:

(1) Lloyd Dixon, Jr. , "High Power Factor Preregulators for Off-Line Power Supplies", Unitrode Power Supply Seminar Handbook, SEM-600A, 1988.

(2) R. Mammano and R. Neidorff, "Improving Input Power Factor - A New Active Controller Simplifies the Task", Proceedings of the 19th International PCIM Conference, 1989.

(3) Unitrode Power Supply Seminar Handbook for 1990, (in preparation).

The amplifier can be set up to operate at full DC gain, if tight regulation of the output voltage is desired, but at the cost of somewhat slower dynamics (recovery from sudden input voltage or load changes). For the intended application of the

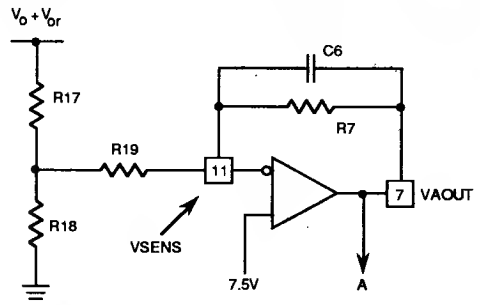


Figure 7. Voltage sensing circuit. The output voltage at Pin 7 is limited to the range from 1V at no load, to 5.6V at full load.

UC3854 as a preregulator, with high power factor as the primary concern, it is best to configure this section as shown in Fig. 7.

The transfer function of the voltage amplifier feedback circuit must be carefully suited to the characteristics of the remaining components of the feedback loop if the given distortion specifications and loop dynamics requirements are to be met. The amount of distortion in the line current depends on the amount of second harmonic ripple introduced into the multiplier by the Vrms signal and by the error amplifier output. The latter's contribution amounts to 0.5% third harmonic distortion in line current for each 1% second harmonic present at Pin 7, calculated in terms of the nominal 4V voltage swing at Pin 7 with $K_m = -1$.

This allows us to calculate the maximum ripple voltage that can be tolerated at Pin 7, as in the following example.

EXAMPLE:

Assume $P_o = 250W$, $V_o = 385V$; then $I_o = 0.625A$.

The 100KHz average current delivered through the boost rectifier to the capacitor and load has a frequency of 120Hz, and an average value of 0.625A at full power. It swings between zero and 1.25A, and we can calculate the ripple voltage V_{or} present in the capacitor voltage V_o:

a) $$V_{or} = \frac{0.625}{2\pi \cdot 120 \cdot C_o} \quad \text{volts peak}$$

Assuming that C_o was chosen at about $2\mu F$ per watt (see above), we have,

$C_o = 450\mu F$, and
$V_{or} = 1.84Vpk$.

Vo is attenuated from 385V to 7.5V, the amplifier's reference voltage, by divider R_{17} and R_{18}: V_{or} will necessarily be reduced by the same factor:

b) $$V_{or} = \frac{1.84 \cdot 7.5}{385} = 0.036V$$

With the multiplier set up properly, a 4V change (from 1V to 5V) in the voltage amplifier output changes the line current from zero to full load. A ripple voltage V_{or} at the amplifier's output, equal to 2.5% of 4V (0.1V), will contribute 1.25% third harmonic distortion to the line current. Then, the product $R_{19} \cdot C_6$ must be such that with an input of 0.036V at 120Hz, the output is 0.1V. In other words, the gain at 120Hz must be;

c) $G_{120} = \frac{0.1}{0.036} = 2.8$ V/V @ 120Hz, with $K_m = -1$.

NOTE: A few advance samples of the UC3854, manufactured in 1989, had a K_m value of about -6. Those devices required a gain G_{120} equal to 1/6 the value calculated above.
The integrator constant is:

13) $$R_{19} \cdot C_6 = \frac{1}{2\pi \cdot 120 \cdot G_{120}} \text{ seconds, or}$$

d) $$R_{19} \cdot C_6 = \frac{1}{2\pi \cdot 120 \cdot 2.8} = 470\mu s.$$

The reciprocal of the integrator constant $R_{19} \cdot C_6$ is the frequency (in rad/s) at which the gain is one. Any combination of values of R_{19} and C_6 whose product is equal to $370\mu s$ will provide the required gain of 3.2 at 120Hz.

Note that this result was determined based on distortion requirements alone, and that we have not yet considered R_7 which will have to be added in shunt with C_6. Without this resistor, the voltage feedback loop will surely be unstable, since there are two -90 degree contributions; one from the output capacitor, and another from the voltage amplifier

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(with R_{19} and C6 only). By adding the resistor R_7 to the feedback path, we can make sure that the net phase lag at unity gain crossover is at least 45 degrees less than 180, thus guaranteeing stability. For 45 degrees of phase margin, the best value for this resistor is that which will place a pole in the voltage control open loop response at the unity-gain frequency f_c, given by Eq. 14:

$$14)\quad f_c = \frac{1}{2\pi} \cdot \sqrt{\frac{P_o \cdot V_{ref}}{V_o^2 \cdot V_a \cdot C_o \cdot R_{19} \cdot C_6}} \quad \text{Hz}$$

P_o = output power, watts
V_{ref} = reference voltage
V_o = DC output voltage
V_a = output range of voltage amplifier, volts
C_o = bulk capacitor, farads

For P_o=250W, V_{ref}=7.5V, V_a=4V, V_o=400V, C_o =500µF, R_{19}=10K, and C_6=47nF (for $R_{19} \cdot C_6$=470µs), we get f_c = 20 Hz.

We can now find a value for R_7:

$$15)\quad R_7 = \frac{1}{2\pi \cdot f_c \cdot C_6} \quad \text{ohms.}$$

For the example above, R7=174K.

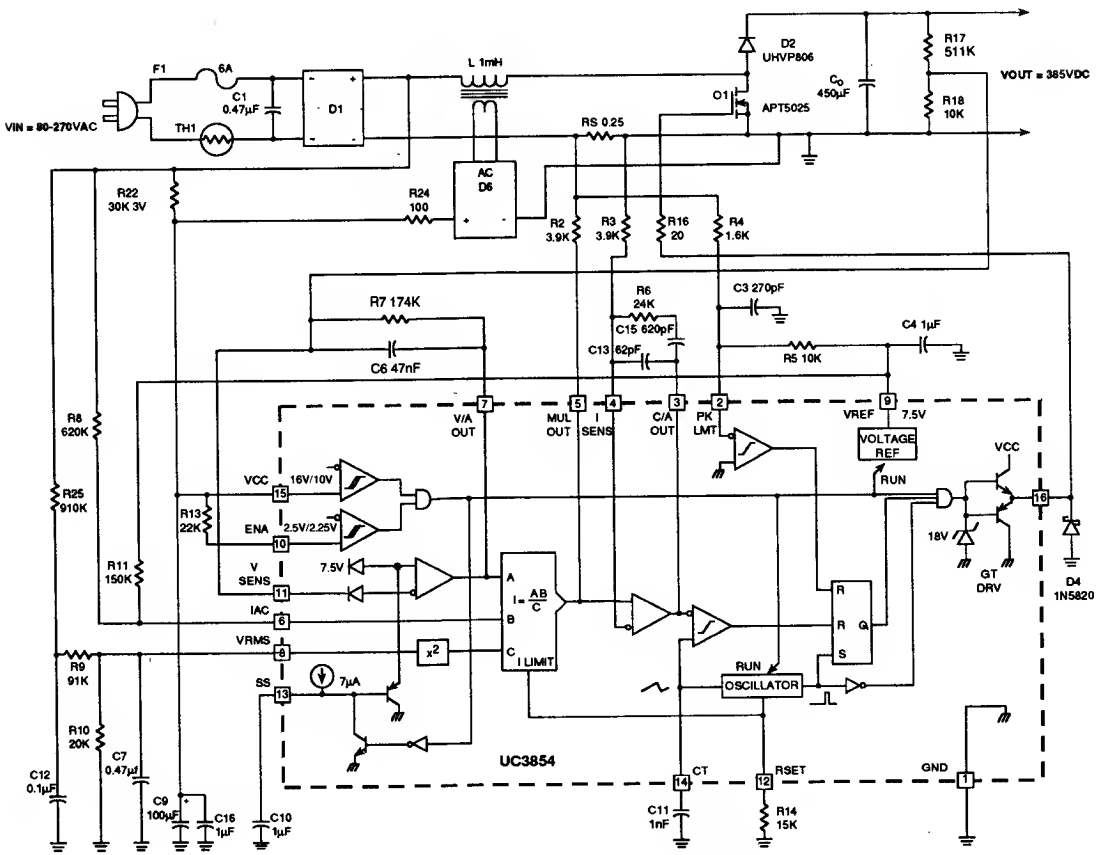


Figure 8. Complete schematic of 250W high power factor preregulator.

Design Note

A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

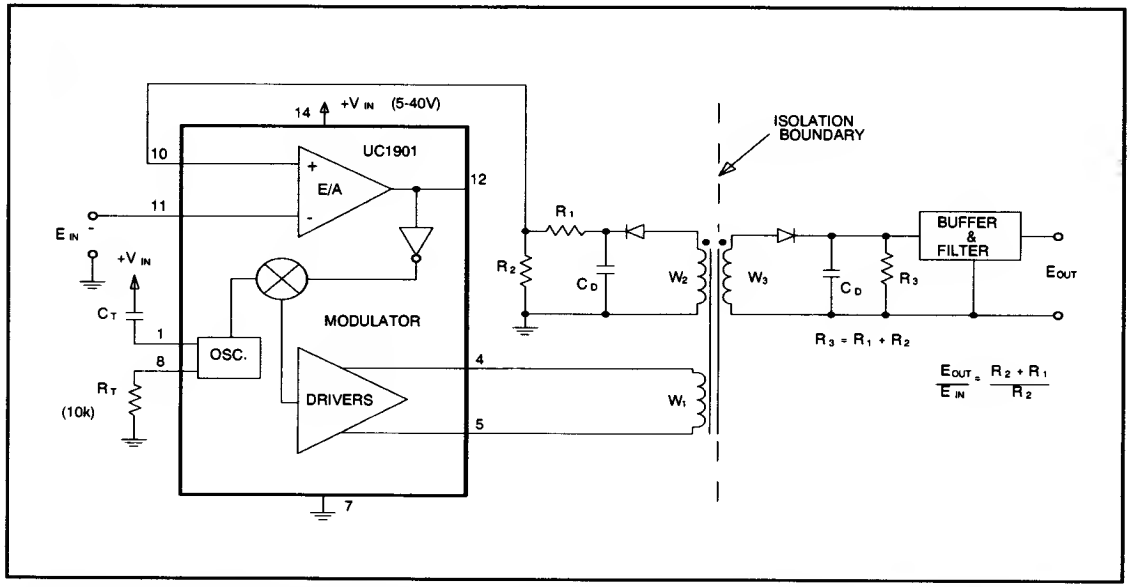
The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal, AC, transfer functions can be established across the isolation boundary.

The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W_2 and W_3) on a small signal transformer. The demodulated signal from winding W_2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W_3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

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Design Note

UC3842A
LOW COST START-UP AND FAULT PROTECTION CIRCUIT

This circuit optimizes control circuit performance to include:

- **Low Start-up Current, Less Than 0.5 ma**
- **MOSFET Compatible Undervoltage Lockout Thresholds 16V Turn-on, 10V Turn-off**
- **Programmable Restart Delay HICCUP Fault Protection**
- **Auxiliary 5V Precision Reference**
- **Overvoltage/OvertemperatureProtection**

CIRCUIT DESCRIPTION AND OPERATION:

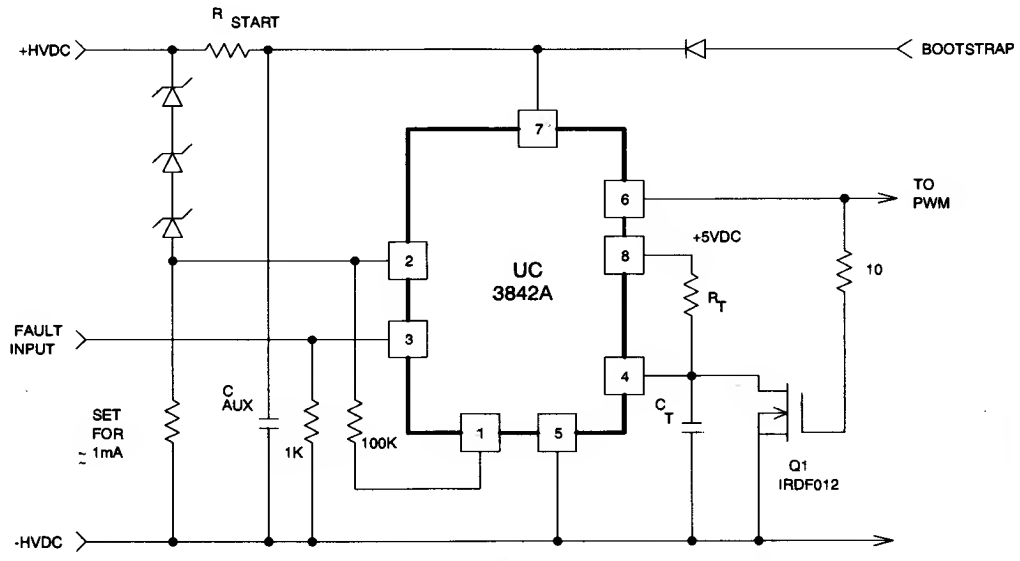
The UC3842A Controller is featured in this design ***NOT*** as the power supply control IC, but in a supervisory function to assist the principal PWM. It will be utilized to facilitate a low current start-up of less than 0.5 milliamp from the high voltage bulk supply. Additionally, the UC3842A features 16 volt turn-on and 10 volt turn-off thresholds, ideally suited for power mosfet gate drive circuits. The 1 amp output of the UC3842A is used to switch the auxiliary supply voltage to the principal PWM controller, a UC3825 or UC3846 for example.

The oscillator of the UC3842A is configured to generate a constant off time, corresponding to the desired restart delay interval. At the beginning of its operation, the UV initiates a clock cycle and the PWM output at pin 6 goes high. This is fed to transistor Q_1 which pulls the R_t/C_t input at pin 4 low, thus "freezing" the oscillator, while keeping the PWM output high. Once a valid fault (greater than 1 volt) is received at the current sense input (pin 3), the output at pin 6 will go low. Transistor Q_1 is then turned off, and the oscillator generates an off period, or delay as programmed by the R_t/C_t components. This procedure will repeat as often as dictated by the fault conditions, but significantly reduces the average short circuit currents and power dissipation.

The UC3842A's current sense node is used as the fault input, and can be configured to provide numerous safeguards. Primary overvoltage protection is accomplished by using a simple resistor divider network or series string of zener diodes to the high voltage rail. Overtemperature protection is possible by including the UC3730 Precision Thermal Monitor IC, or a variable impedance thermistor. In a simple configuration, the fault circuit is designed to deliver a 1 volt input to pin 3 of the UC3842A when a fault response is necessary. The error amplifier can also be biased to accept lower amplitudes of valid fault inputs at the current sense input. A precision five volt auxiliary supply is made available at the IC's reference output, pin 8 and can supply 20 milliamps maximum.

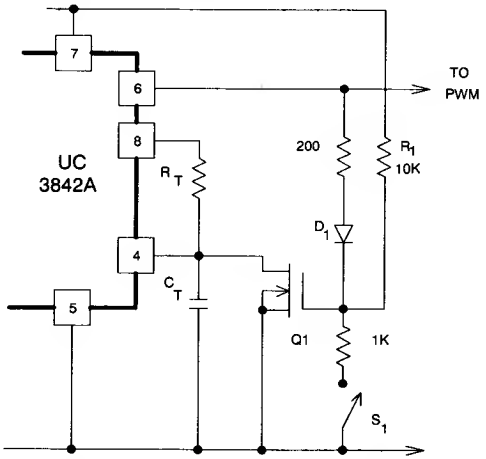
UC3842A Supervisory Function Circuits

LOW COST START-UP and FAULT PROTECTION Circuit

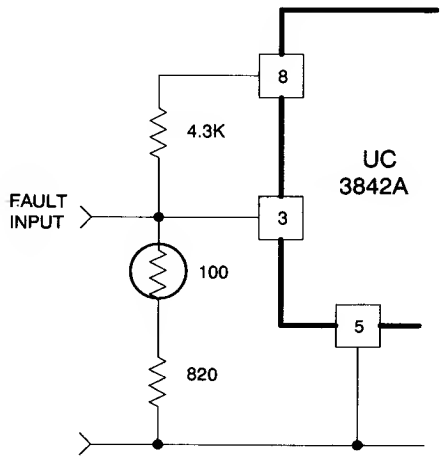


Design Note

COMBINED LATCH/RESET/HICCUP FUNCTIONS
General Circuit



OVER-TEMPERATURE PROTECTION
using 50 to 100Ω thermocouples



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Design Note

UC1842/UC1842A FAMILY
SUMMARY OF FUNCTIONAL DIFFERENCES

The industry standard series of UC1842/43/44/45 devices has been improved for higher frequency, off-line power supplies. This new "A" series of controllers, UC1842A/43A/44A/45A, feature three major advantages over their predecessors as shown in the summary below.

Start Up Current

	UC1842/45	UC1842A/45A
Typical (T_J=25°C)	0.5ma	0.3ma
Maximum (T_J=25°C)	1.0ma	0.5ma

Oscillator Discharge Current

	UC1842/45			UC1842A/45A		
	MIN	TYP	MAX	MIN	TYP	MAX
At T_J=25°C (ma)	7	10	13	7.8	8.3	8.8
Overtemp. Range	6	—	14	7.5	—	8.8

Output Saturation

	UC1842/45	UC1842/45A
During UVLO	1V @ 0.2ma	1V @ 10ma

The reduced start-up current is of particular concern in offline supplies where the IC is "powered-up" from the high voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Lowering this by 50% in the "A" version family will reduce the resistors power loss by the same percentage.

Precision operation at high frequencies with an accurate maximum duty cycle can now be obtained with the "A" family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or deadtime.

Another significant improvement has been made in the output section, specifically to the lower totem-pole transistor's operation during undervoltage lockout. The "A" series of devices prevent the power MOSFETs from parasitically turning-on at powerup due to the "Miller" effect. This new technique allows the IC to sink higher currents at lower saturation voltages than it's predecessors.

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UC3840/UC3841/UC3851 PWM CONTROLLERS SUMMARY OF FUNCTIONS AND DIFFERENCES

The UC3840/UC3841 and UC3851 PWM controllers incorporate numerous protection features for switch mode power supplies. The list includes programmable undervoltage lockout thresholds, programmable current limit thresholds, overvoltage protection, soft-start and external stop/reset capability. While these controllers are similar in concept, there are subtle differences amongst them in the operation of the error latch circuitry, specifically, the external stop and reset inputs. The UC3841 and UC3851 ICs feature an improved circuit design which simplifies the interface to the internal protection circuitry. A summary of the functions and modes of operation is listed below.

EXTERNAL STOP

	UC3840	UC3841/51
Low (<0.8V)	Stop	Defeat E/L Operation
High (>2.4V)	Normal	Stop
Open	Normal	Normal
Cap. to GND During Power-up	Not Recommended	Delay E/L Operation at ~ 13msec/μF

E/L= Error Latch

RESET

	UC3840	UC3841/51
High (>3.2V)	Latch	Latch
Low (<2.8V)	Requires UV Cycle To Reset	Reset

SOFT START

	UC3840	UC3841/51
After UV or RESET	Unlatched	Latched (Vss≤0.40V)

The UC3851 controller incorporates two additional features, a toggle flip-flop for an accurate 50% maximum duty cycle clamp, and a 1 amp peak totem-pole output for driving power MOSFETs. Maximum duty cycles and output configurations for each device is shown below.

MAXIMUM DUTY CYCLE (T_J = 25°C)

	UC3840/41	UC3851
R_T = 20K, C_T = 1nF	0-95%	0-46%

PWM OUTPUT

	UC3840/41	UC3851
1A (PK)	Open Collector Active Low	Totem Pole Active High

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Design Note

UC3842A FAMILY
FREQUENCY FOLDBACK TECHNIQUE PROVIDES PROTECTION

Excessive power dissipation in switching devices can occur during start-up and overload conditions in many switchmode power supplies. Many sophisticated PWM controllers provide the means for protection against these conditions; however, simple low-cost controllers will require additional circuitry. The circuit described below utilizes only one additional resistor and transistor to enhance the performance of the UC3842A family of controllers.

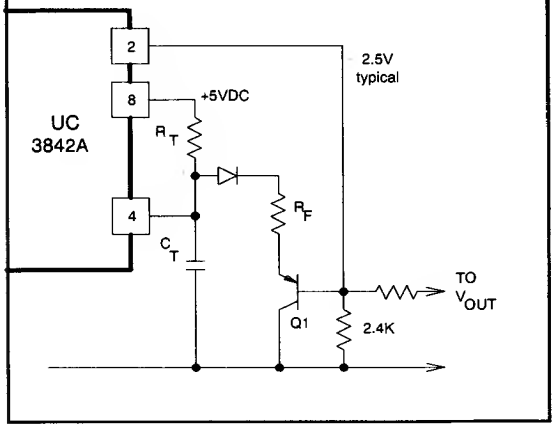
The power supply output voltage is fed to the error amplifier inverting input (pin 2) at a 2.5 volt amplitude under normal operating conditions. During start-up or overload, however, this voltage can drop to zero. The circuit shown uses this feedback voltage to divert normal charging current from the IC's timing capacitor to ground whenever the feedback voltage is below the 2.5 volt nominal. A linear three-to-one reduction of oscillator frequency is obtainable for most applications. This technique lengthens the potential maximum on-time and reduces the programmed deadtime. In many circuits, however, the peak current limit threshold is reached early in the cycle under these overload conditions, and this is not a problem. For most applications, the foldback resistor value (R_F) should equal that of the timing resistor (R_T)

EXAMPLE:

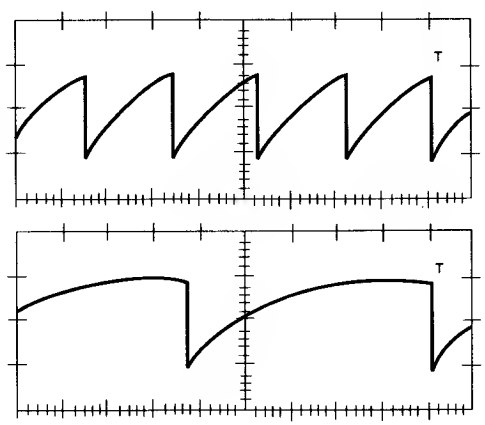
100 kHz operation, R_T = 15K, C_T = 1 nF, R_F = 15K, Q_1 = 2N2907A

OPERATING MODE	NORMAL	OVERLOAD
$V_{E/A}$ - (pin 2)	2.50V	0.00V
Oscillator Freq.	105 kHz	36 kHz

FREQUENCY FOLDBACK TECHNIQUE
Circuit



OSCILLATOR FREQUENCY



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Design Note

PROGRAMMABLE ELECTRONIC CIRCUIT BREAKER

The design of a programmable electronic circuit breaker is shown below which utilizes the UC3843A control IC to facilitate a high speed turn-off following an overcurrent condition. This low cost, industry standard IC contains the required protection features and drive capability in a single 8 pin device.

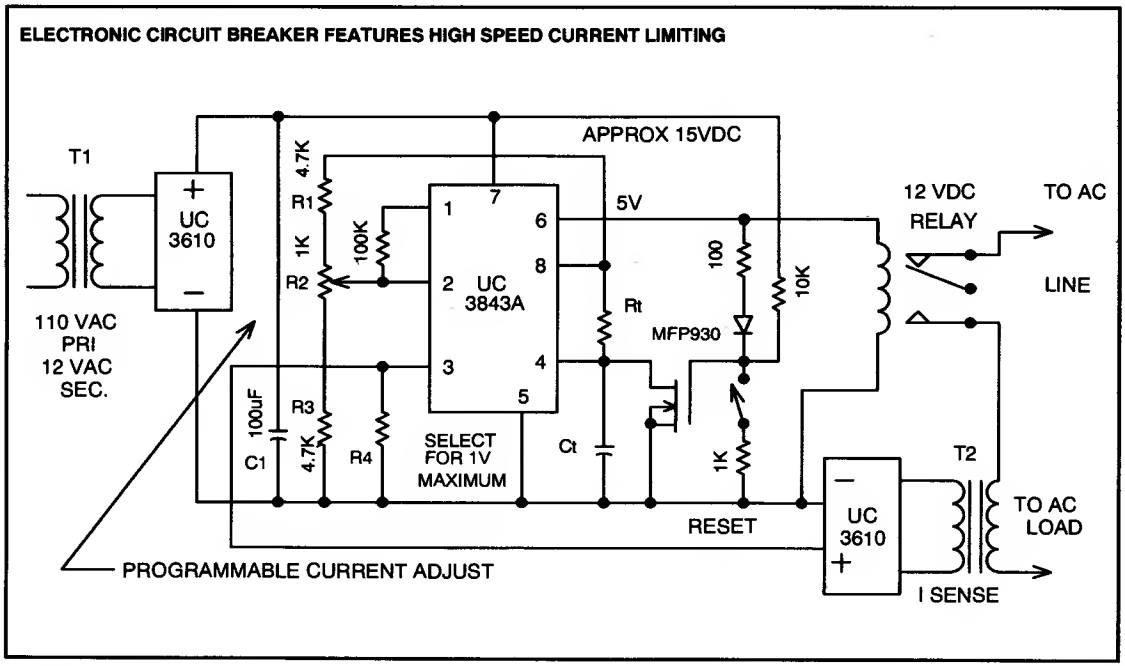
CIRCUIT OPERATION

Power to the controller is provided by a simple, low cost 60Hz transformer from the AC line which delivers 12 VAC at the secondary. The output current is determined primarily by the relay used with an additional 10 milliamps, or so, drawn by the IC. Undervoltage lockout prevents any operation until 10 VDC is obtained across capacitor C1, when the UC3843A will turn on. The PWM output at pin 6 goes high which drives the relay ON and switches the load across its respective power source. The load current is sensed by the current transformer T2, multiplied by its truns ration(N) and develops a voltage across the sense resistor R4. This resistor is scaled to delivery 1 volt maximum at the full load current and is one input to the PWM comparator.

While the output at pin six is high transistor Q1 is also turned ON which disables the ICs oscillator, locking the output high until toggles by the PWM. A 10K resistor (R5) to the supply voltage (pin 7) supplies bias to Q1 after the output has gone low, providing a latched OFF condition. This can easily be reset by pulling Q1's gate low through 1K ohms to ground as shown.

SCHEMATIC DIAGRAM

ELECTRONIC CIRCUIT BREAKER FEATURES HIGH SPEED CURRENT LIMITING



The other input to the PWM comparator is represented by the voltage at pin 1, the error amplifier output which can be adjusted by resistor R2. Internally, this voltage is reduced by two diode drops then attenuated to one-third its amplitude. The PWM circuitry compares this voltage with that of the current sense input at pin 3. When the current sense input exceeds the threshold set by resistor R2, the comparator is tripped and the ouptput at pin 6 is latched OFF.

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CURRENT MODE CONTROLLED QUASI-RESONANT ZERO VOLTAGE SWITCHING POWER CONVERSION

Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise switch ON time, an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

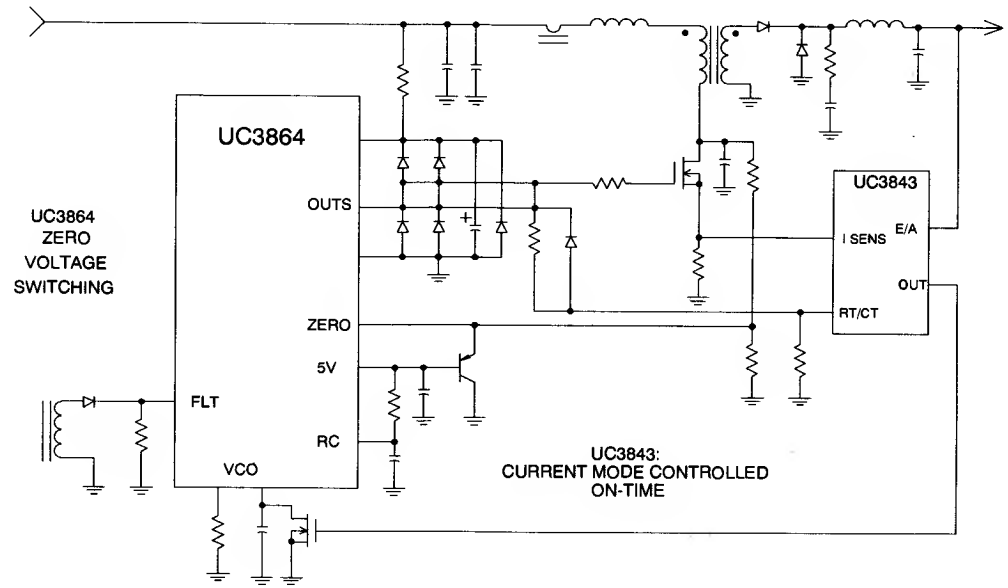
PRINCIPLES OF OPERATION

Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator (VCO) to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry in their standard configuration. When the resonant capacitor voltage crosses zero, the UC3884 output goes high. This turns ON transistor Q1 and recycles the UC3843A which initiates the next current mode controlled period. The UC3864 error amplifier and VCO are not used, however the fault protection circuitry will still respond to an overcurrent fault.

CURRENT MODE CONTROLLED ZVS FORWARD CONVERTER

VARIABLE FREQUENCY OPERATION



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OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES

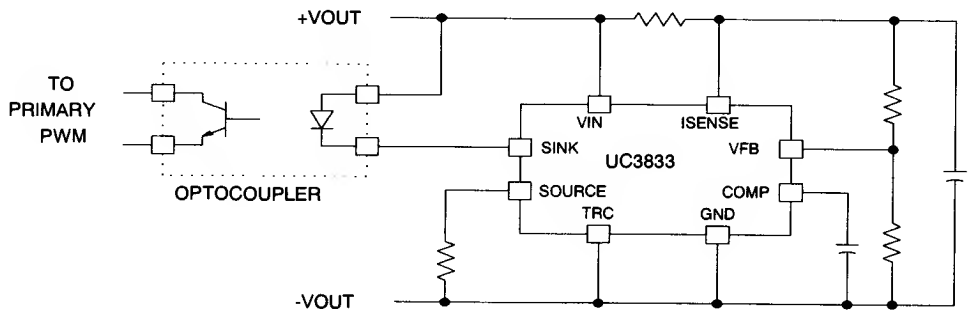
The use of optocouplers in the feedback path of switchmode power supplies is probably one of the most common practices in the industry. Benefits of this method include low component cost, high voltage isolation and simplicity of design and implementation. Although adequate for many existing designs, the need for additional loop gain bandwidth occurs as switching frequencies are pushed towards the megahertz region.

One of the most popular ways to drive an optocoupler utilizes a TL431 Adjustable Shunt Regulator. It is configured on the output side of the power supply to modulate the optocoupler's photo diode current as a function of the power supply output voltage. Across its isolation boundary, the optocoupler transistor is connected to the PWM controller's error amplifier on the primary side of the power supply. Variations in the output voltage are optically transferred back to the error amplifier and control loop for correction. Providing additional features like over current protection or external shutdown require extra optocouplers and drive mechanisms, thus increasing the circuit complexity.

A linear regulator control IC, such as the UC3832, UC3833 or UC3836 can be substituted for the '431 while providing numerous additional features besides regulating the output. Overcurrent limiting and fault protection can be combined with the error voltage to drive the optocoupler and override it when necessary. Handshaking with external control logic, such as shutdown and sequencing is greatly simplified since the control IC is referred to the same ground. The most obvious benefit, however, is the introduction of the supplementary error amplifier in the feedback loop with programmable compensation.

Depending on the specific application, current limiting can be tailored to accommodate a programmable foldback characteristic, constant current or complete overcurrent shutdown. The UC3832 and UC3833 provide an addition level of versitility by offering a programmable duration event timer in the current limit circuitry. An adjustable trip threshold to accommodate varying load demands can be facilitated with the UC3832. For additional information, please consult application note U -116 and the respective device data sheets.

UC3833 LINEAR CONTROL IC DRIVES OPTOCOUPLED FEEDBACK



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